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A 14-bit 100-MS/s Digitally Calibrated Binary-Weighted Current-Steering CMOS DAC without Calibration ADC

Yusuke Ikeda, Matthias Frey, and Akira Matsuzawa
Department of Physical Electronics, Tokyo Institute of Technology
2-12-1-S3-27 Ookayama, Meguro-ku, Tokyo 152-8552 Japan
Tel/Fax: +81-3-5734-3764, E-mail: matsu@ssc.pe.titech.ac.jp

***Abstract*—A 14-bit digitally calibrated digital-to-analog converter (DAC) is presented. This DAC uses a simple current comparator for the current measurement during calibration instead of a high-resolution ADC. Therefore, compared to a calibration scheme utilizing a high-resolution ADC, a faster calibration cycle is possible with smaller additional circuits. To reduce the additional area for calibration and error compensation, the lowest 8-bit DAC is used for both error correction and for normal operation; the additional DACs required for calibration are only of 3-bit and of 7-bit resolution. Nevertheless, a large calibration range is attained. Full 14-bit resolution is achieved on a small chip-area (0.72 mm^2). The measurement results show that the spurious free dynamic range is 83.4 (46.6) dBc for signals of 6 kHz (30 MHz) at an update rate of 100 MS/s.**

I. Introduction

For telecommunication applications, digital-to-analog converters (DACs) with a resolution of 10–14 bit at a conversion rate of several hundred MS/s are required. To fulfill such challenging specifications, current-steering DACs are widely used at present. The resolution of a current-steering DAC is limited by the mismatch of the elements that compose the DAC's current sources. Therefore, in order to obtain a high resolution, it is necessary to control the mismatch of the elements by enlarging their area. However, by increasing their size the parasitic capacitances, as well as the wiring capacitances, are augmented and the DAC's resulting conversion speed may not satisfy the desired specifications at low power levels. Furthermore, increased area also means increased cost; the area of the current-steering DAC should therefore be kept small. A high speed, high resolution DAC can be achieved by applying a calibration scheme [1–4].

In this paper, a novel digital calibration scheme is proposed that is applied to the binary-weighted part of the DAC. Digital calibration schemes measure the current value of each current source and—by means of digital signal processing—determine an appropriate value that will be added from a calibration DAC. To measure the values of each current source, the use of an accurate high-resolution sigma-delta analog-to-digital converter (ADC) has been proposed [1-3]. This additional sigma-delta ADC enlarges the die-area and therefore increases the cost of the chip. In addition, calibration schemes using a sigma-delta ADC are slow due to high over-sampling ratios that are required to achieve a high resolution. To overcome these disadvantages, another scheme was proposed in [4] using current comparators instead of a high resolution ADC. In addition, this scheme chooses a binary-weighted structure. Binary-weighted DACs (as opposed to thermometer-decoded DACs) are more suitable for digital calibration as there are fewer current sources that need to be measured; this reduces the die-area of the memory and shortens the calibration time. However, a calibration DAC is required at each current source of the MSB array in [4]. This scheme therefore also enlarges the total die area.

The proposed scheme utilizes the LSB-part of the DAC for conversion as well as for calibration. The analog circuitry is only marginally increased as the calibration is mainly done in the digital domain. Consequently, the DAC's total die area is still small; nevertheless, a high resolution is achieved. Shifting the main part of the calibration into the digital domain will become even more advantageous with future processes and for higher resolution DACs.

The paper is structured as follows: after this brief introduction, the calibration algorithm is discussed in detail in Section II. The measurement results are presented in Section III. Finally, the paper ends with some conclusions in Section IV.

II. The DAC's Calibration Scheme

The architecture of the proposed digitally calibrated DAC is shown in Fig. 1. The DAC is segmented into the following parts: "MAINDAC" (consisting of a 6-bit "MSBDAC" and an 8-bit "LSBDAC"), "CALDAC" (3 bit), "SUBDAC" (7 bit), the current mirror array (6 bit), the current comparator, the output stage, and the calibration logic. Each DAC is composed of a current-source array and switches. The MSB array, the CAL array, the SUB array, and the current mirror array each need to have one additional dummy current source, which is of the same current value as each array's lowest current. All current sources and current mirrors are composed of conventional low voltage cascodes.

The output stage is composed of PMOS current sources folding the DAC current and a return-to-zero (RZ) circuit [2].

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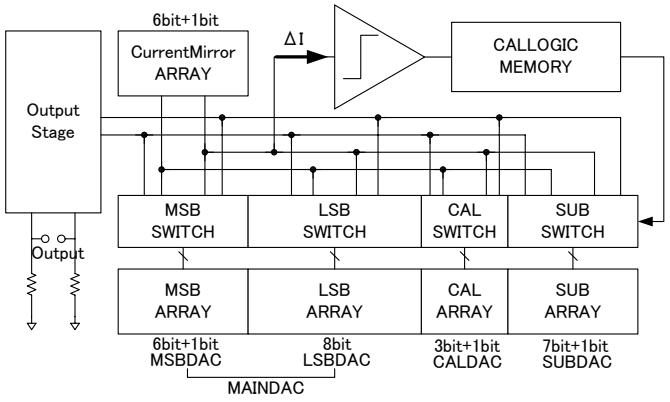


Figure 1. Block diagram of the proposed calibrated DAC.

The MSB array will be self-calibrated. In the proposed self-calibration scheme, the MSB dummy current source (I_{CMSB0}) is calibrated before the 6-bit MSB current sources (I_{MSB0}-I_{MSB5}). The MSB dummy current calibration is called "SUB Calibration", the calibration of the 6-bit MSB currents is called "MSB Calibration". The deviation of the MSB dummy current from its nominal value is δ_0; the deviations from the nominal values for the 6-bit MSB currents are from the lowest value to the highest δ_1, δ_2, δ_3, δ_4, δ_5, and δ_6.

The calibration flow described in Fig. 2 is as follows: the first step in the proposed digital calibration method is to obtain the digitized value of the error current through a successive approximation process using the calibration current sources and a current comparator. The digital value of the error current is then used for the error correction in the digital domain. The calibrated output is composed of currents from the DAC for conversion, as well as of currents from the DAC for calibration.

A. *SUB Calibration*

The MSB dummy current source (I_{CMSB0}) has the same nominal current as the sum of the LSB array and the CAL array (I_{LSBs}). However, due to mismatch, the current sources show different output currents. During "Sub Calibration", the error current of I_{CMSB0}, δ_0, will be determined.

Using the current mirrors and the current comparator, I_{CMSB0} is compared with I_{LSBs}, the sum of the LSB array and the CAL array. The current comparator circuit is depicted in Fig. 3. δ_0 can be obtained as a 6-bit digital value by a 6-step successive approximation process utilizing SUBDAC, the current comparator output and the calibration logic.

The simplified "SUB calibration" circuit is shown in Fig. 4. During calibration the current-sources are measured twice, once with the switches in position A and once in position B. By using two measurement results, δ_0 is obtained independently of the current comparator offset (I_{offset}). δ_0 is then stored in a register. During normal operation, the error current of I_{CMSB0} is canceled out by correctly switching the SUBDAC.

B. *MSB Calibration*

After "SUB Calibration", the 6-bit MSB current source array will be calibrated. At first, the error current of the lowest bit of the MSB currents, δ_1, will be obtained.

The lowest MSB current (I_{MSB0}) is compared with I_{CMSB0} using the current mirrors and the current comparator. Then, SUBDAC operates to cancel out δ_0.

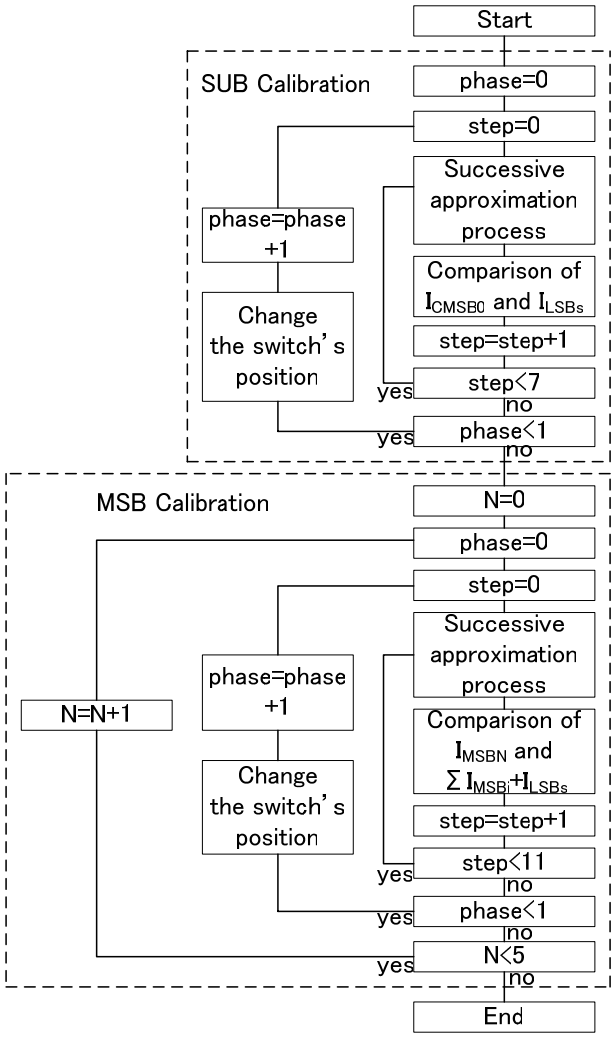


Figure 2. The calibration flow.

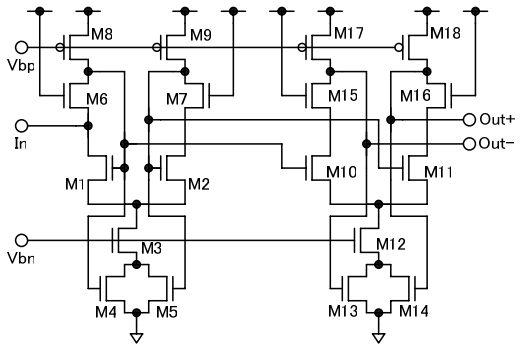


Figure 3. The current comparator.

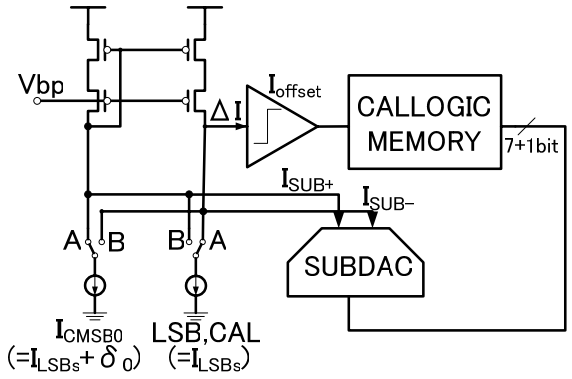


Figure 4. SUB calibration circuit.

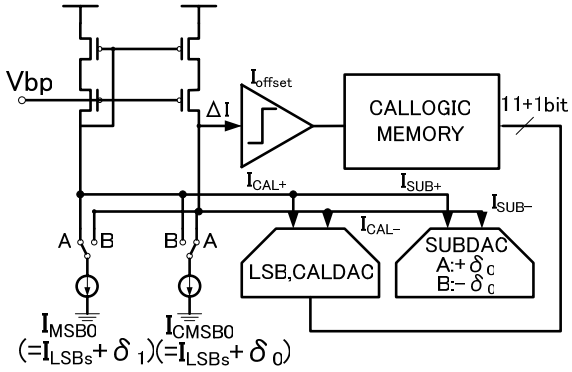


Figure 5. MSB calibration circuit for I_{MSB0}.

δ_1 is obtained as an 11-bit digital value by an 11-step successive approximation process utilizing LSBDAC (8 bit) and CALDAC (3 bit). This process is controlled by the current comparator output as well as the calibration logic. The simplified MSB calibration circuit for I_{MSB0} is shown in Fig. 5.

Same as for the "Sub Calibration", the measurement is done twice, once in phase A and once in phase B.

In the next phase, the error current corresponding to the second lowest MSB (δ_2) will be determined: the second lowest MSB current (I_{MSB1}) is compared with the sum of I_{LSBs} and I_{MSB0}. By using the previously determined error current δ_1, δ_2 is obtained through an 11-step successive approximation process as an 11-bit digital value.

In the same way, the error current of the other MSB current sources can be determined, each with an 11-step successive approximation process and with the previously determined error currents of the lower MSBs.

III. DAC Operation

The architecture for the DAC operation is shown in Fig. 6. All MSB error currents are stored in a register. Other than in a conventional DAC where the 8-bit DAC can produce output currents from 0 to 255 LSB, this converter's 8-bit LSB block ranges from 0 to 511 LSB. This is because the MSB dummy current source is used for the 8-bit LSB conversion. If the MSB array current sources reveal no error, the 8-bit LSB part ranges from 128 LSB to 383 LSB. The MSB array can

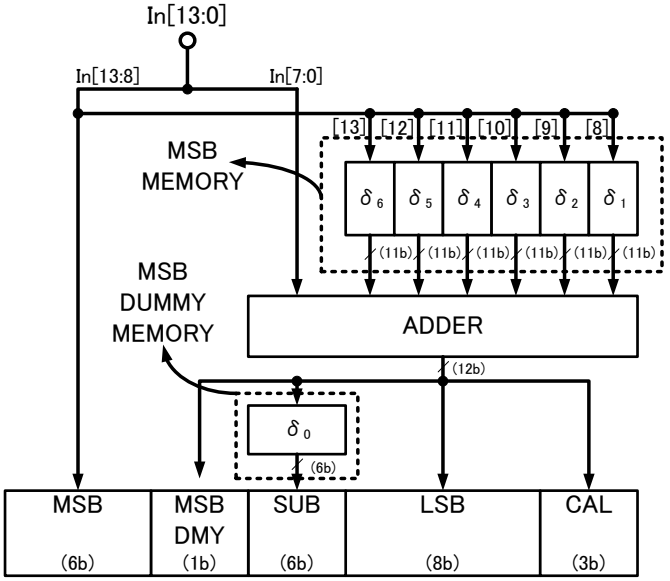


Figure 6. Block diagram of operation during normal conversion.

therefore be calibrated in the large range of -128 LSB to +128 LSB.

The DAC inputs are divided into the 6-bit MSB data and the 8-bit LSB data. The 6-bit MSB data is used as the input to the six MSB switches and to the MSB memory.

The 8-bit LSB data is added to the MSB memory's output and its result controls the MSB dummy switch, the LSB switches, and the CAL switches. Either $+\delta_0$ or $-\delta_0$ is used as the input to the SUB switches, depending on the MSB dummy memory.

In conventional calibration schemes, a large calibration range leading to a smaller MSBDAC area comes at the cost of a large CALDAC area. In this proposed scheme however, the 8-bit LSBDAC is reused for the current correction and the large calibration range of 11 bit is realized by the small CALDAC with a resolution of only 3 bit.

IV. Measurement Results

The proposed self-calibration architecture is realized in a 0.18-µm CMOS technology; the supply-voltage is 1.8 V. The chip's layout is presented in Fig. 7; its active area is only 0.74 mm^2.

Figs. 8 and 9 show the output spectrum at an update rate of 100 MS/s for a 6-kHz input signal before and after calibration, respectively. The SFDR of the DAC is 69.2 dBc before calibration. The linearity is degraded due to mismatch in the current sources of the MSB array. After calibration, the SFDR is increased and becomes 83.4 dBc. The results indicate that the linearity is improved by the proposed digital calibration architecture and 14-bit level is achieved.

Fig. 10 shows the SFDR of the calibrated DAC operating at an update rate of 100 MS/s for various input signal

frequencies. The SFDR of the DAC is 83.4 dBc at 6 kHz and 46.6 dBc at 30 MHz input frequencies. Table I summarizes the measured DAC's characteristics.

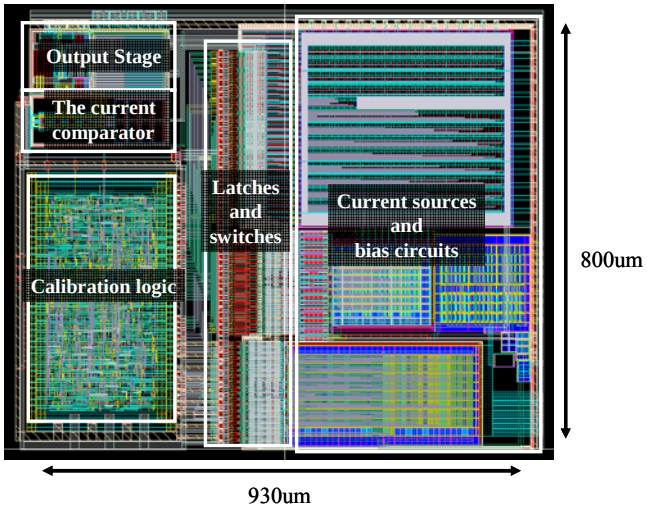


Figure 7. Layout of the DAC.

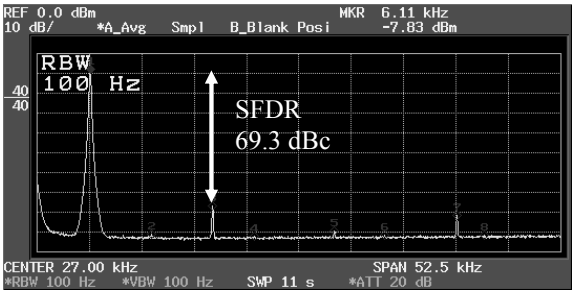


Figure 8. Output spectrum for a 6-kHz input signal before calibration.

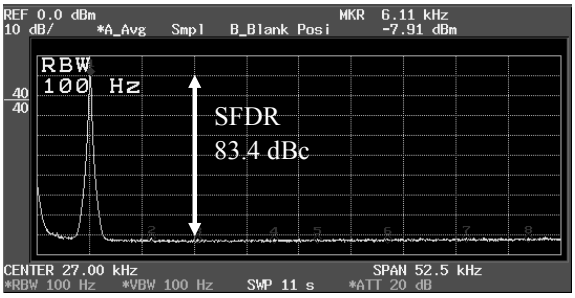
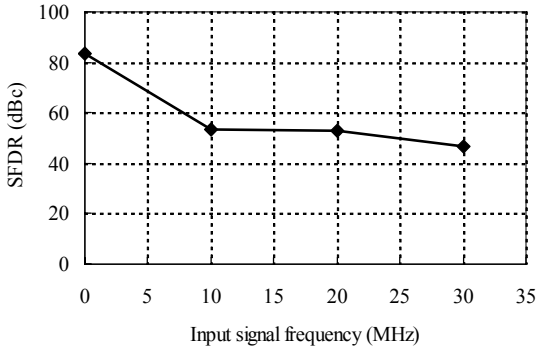


Figure 9. Output spectrum for a 6-kHz input signal after calibration.

V. Conclusion

A new digital calibration scheme for a current-steering DAC has been proposed. This scheme was applied to a binary-weighted DAC that is—due to the minimal number of current-sources—most suitable for a fast digital calibration. Because this scheme uses a single simple current comparator for the current measurement instead of a high-resolution ADC, a fast calibration cycle was attained and the additional circuitry could be kept minimal. Furthermore, using the LSB part of the DAC for both the error correction scheme as well as for the normal conversion, lead to an only minimal increase of die-area. The additional analog circuits required for the digital calibration are only a 6-bit DAC and a 3-bit DAC.



Technology	0.18 um CMOS process
Resolution	14 bit
Sampling Rate	100 MS/s
Full-Scale Current	11.5 mA
Supply Voltage	1.8 V
SFDR (Before Calibration)	69.2 dBc @ fsig=6 kHz
SFDR (After Calibration)	83.4 dBc @ fsig=6 kHz 46.6 dBc @ fsig=30 MHz
Power Dissipation	79.2 mW (analog with output RZ circuit) 21.6 mW (analog w/o output RZ circuit) 5 mW (digital)
Active Area	0.74 mm^2

Figure 10. SFDR at an update rate of 100 MS/s after calibration.

TABLE I. Measured DAC Characteristics

Measurement results have revealed that the proposed digital calibration scheme can be used to achieve 14-bit level linearity. Before calibration, the SFDR of the DAC is 69.2 dBc at an update rate of 100 MS/s for a 6-kHz input signal. After calibration, the SFDR is enhanced to 83.4 dBc.

References

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