A 14-bit 100-MS/s Digitally Calibrated Binary-Weighted Current-Steering CMOS DAC without Calibration ADC

Yusuke Ikeda, Matthias Frey,
and Akira Matsuzawa
Tokyo Institute of Technology, Japan

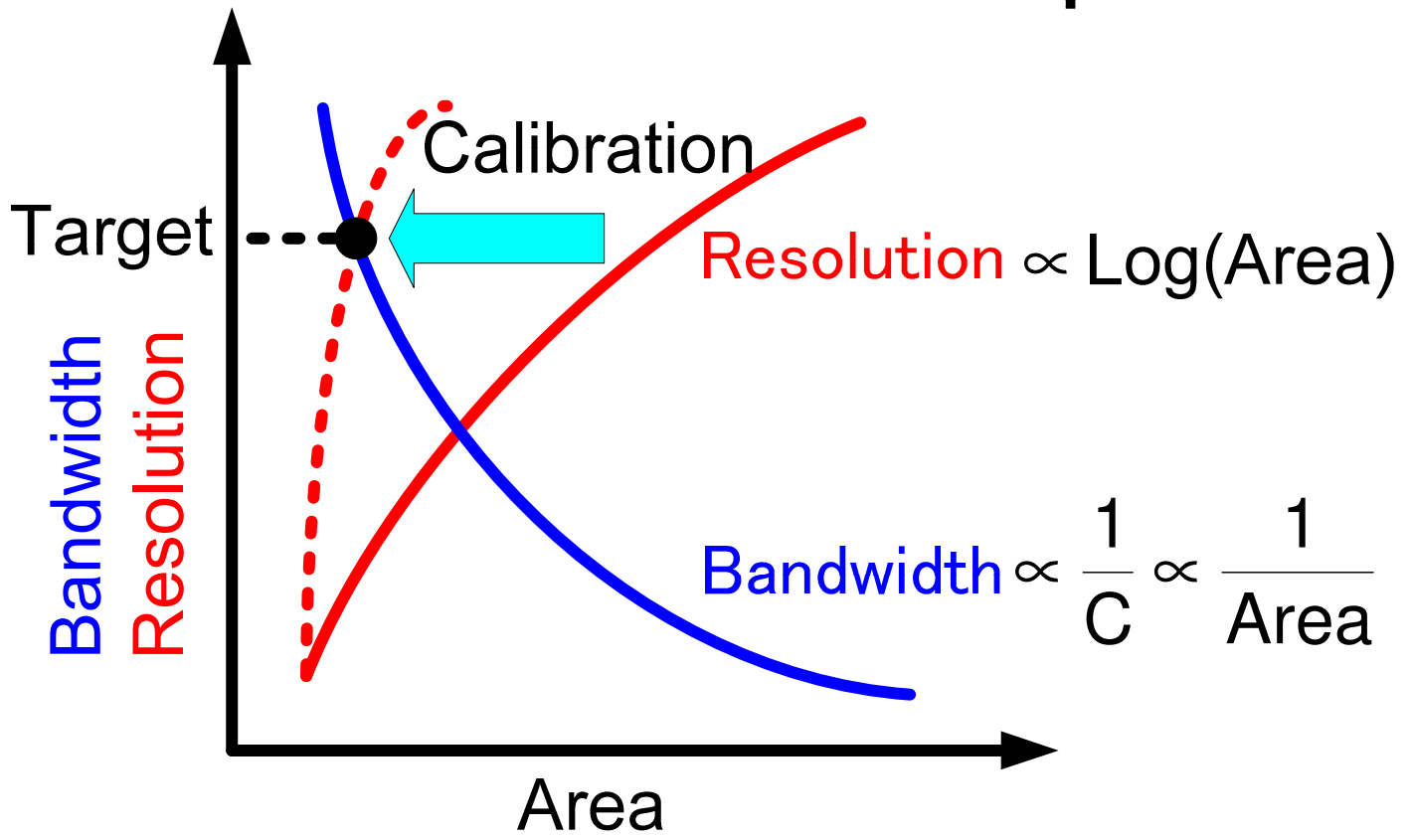
Matsuzawa & Okada Lab.

Outline

- Motivation
- The Calibration Scheme
- Measurement Results
- Conclusions

Motivation

The relation between the area and the performance

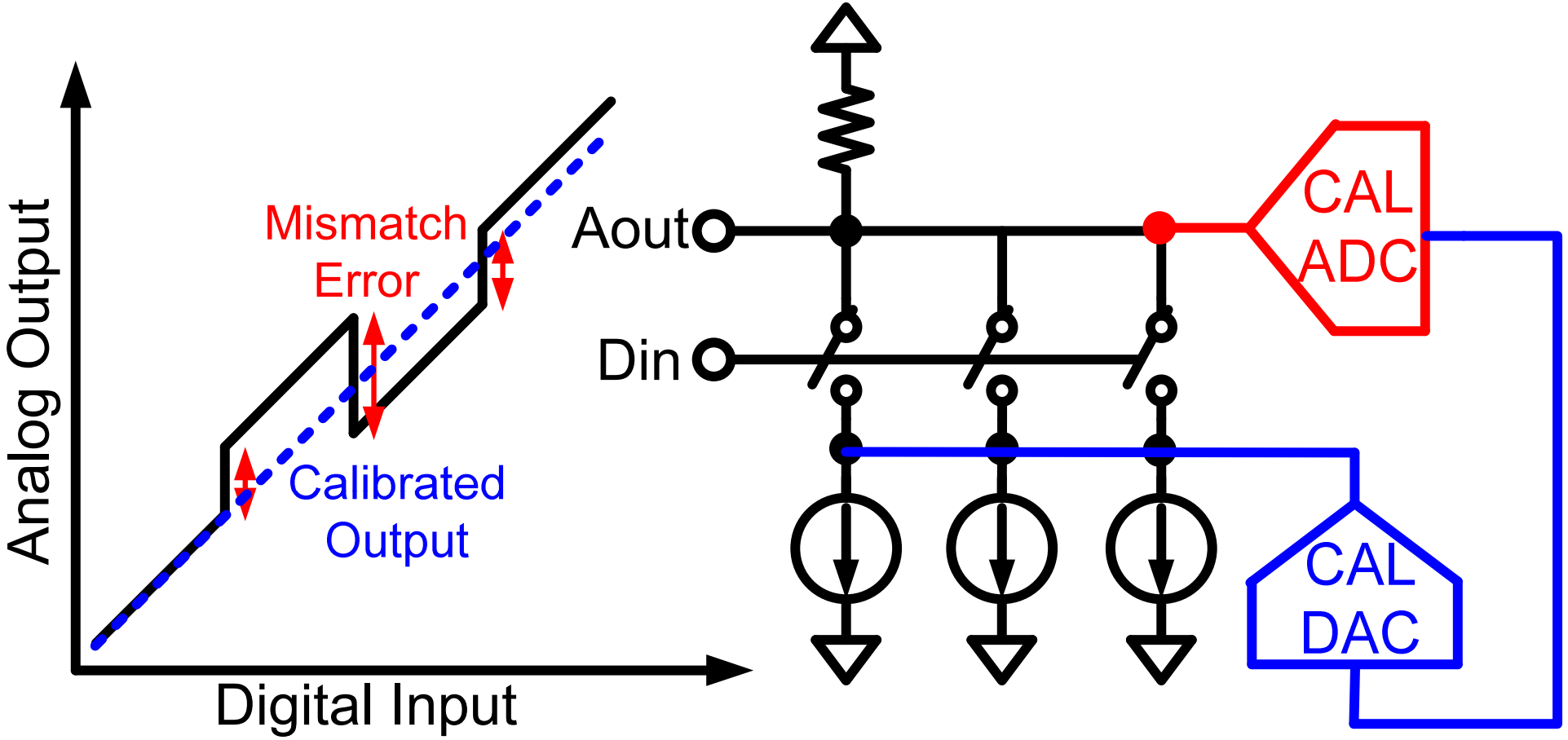


- To realize a high speed and high resolution DAC, it is necessary to utilize the calibration technique.
- Keep the total area small.

Outline

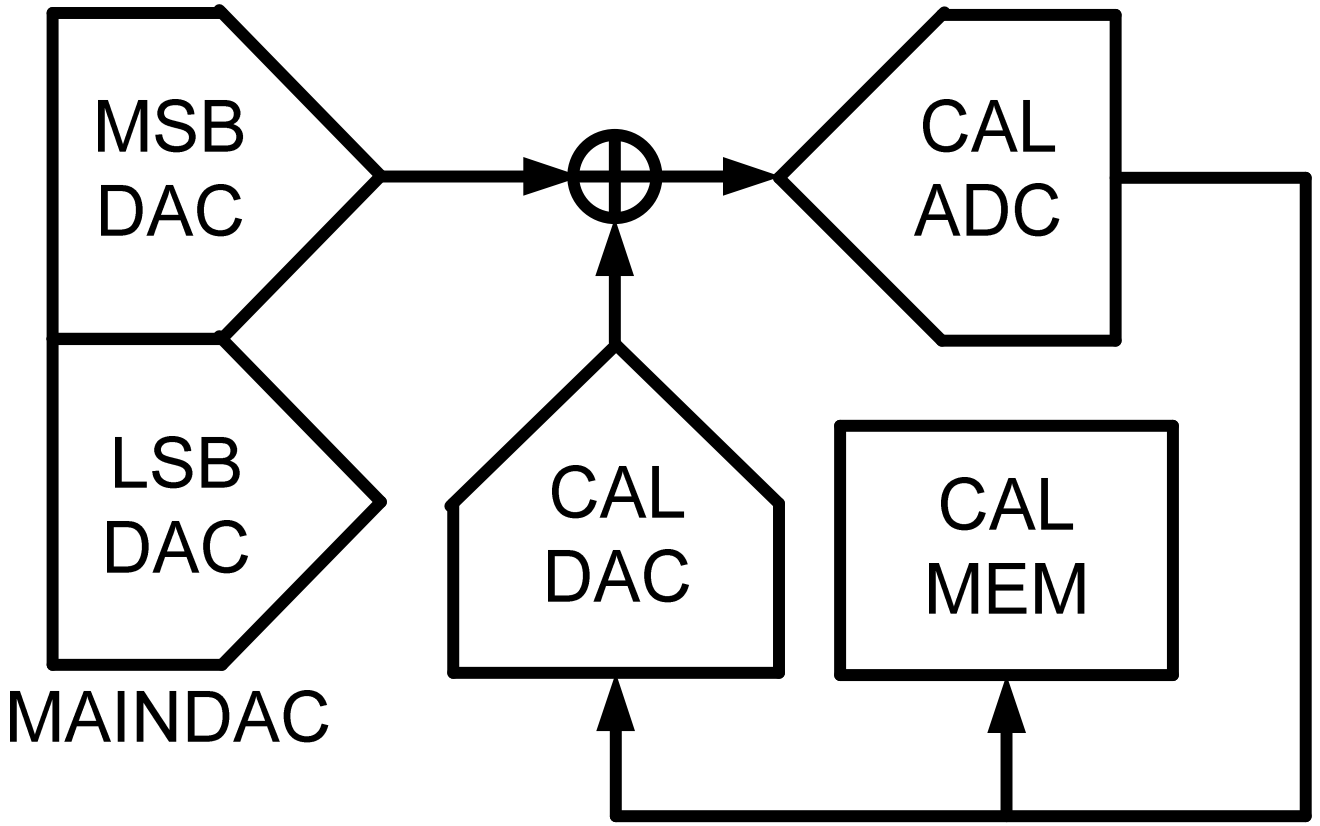
- Motivation
- **The Calibration Scheme**
- Measurement Results
- Conclusions

The CS DAC function



1. The CS DAC linearity is limited by current source mismatch.
2. The mismatch is measured by CALADC.
3. CALDAC corrects the error currents.

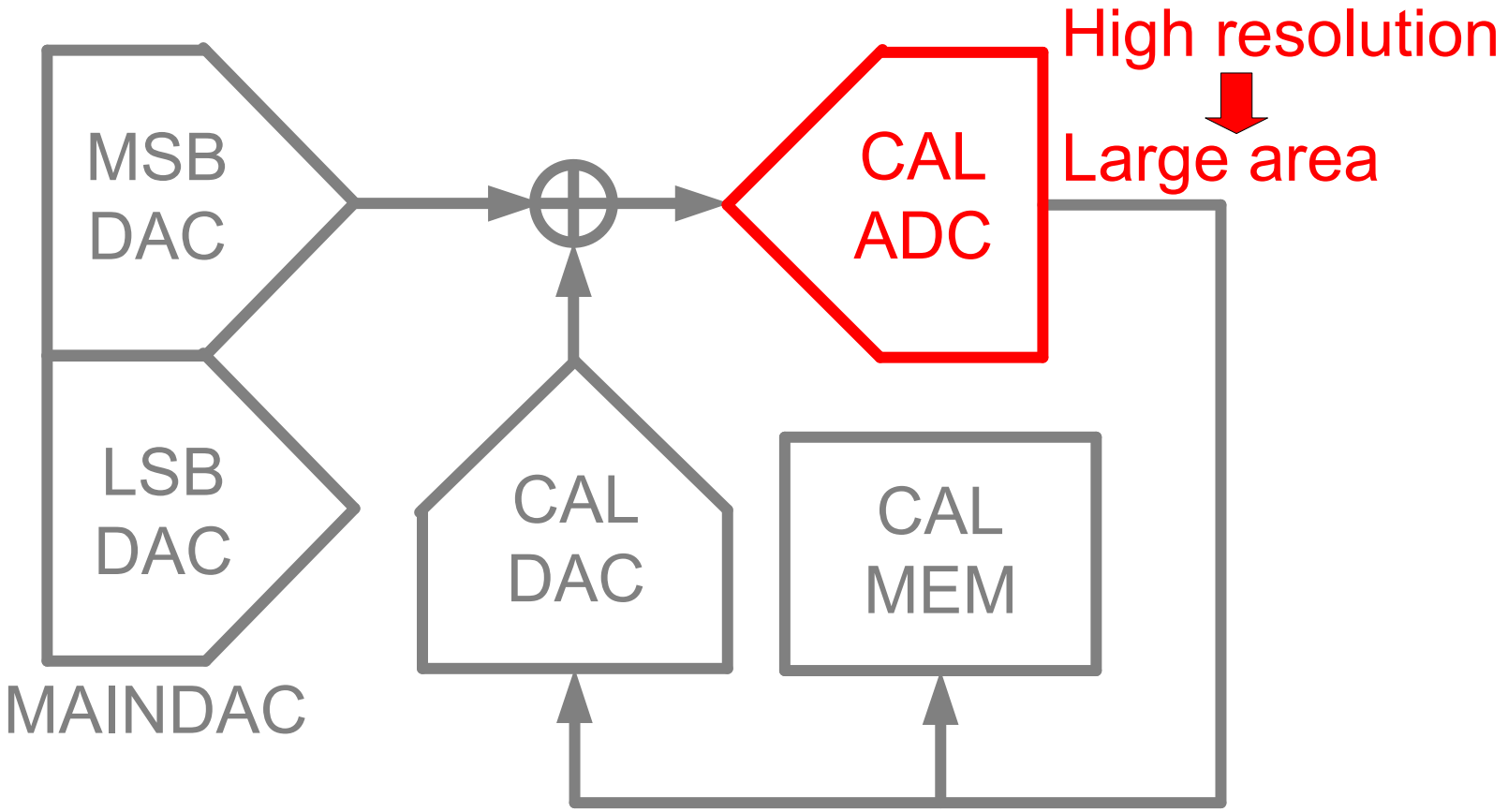
Conventional calibration



1. Mismatch currents of MSBDAC are measured by CALADC.
2. The error currents are stored in CALMEM.
3. CALDAC corrects the error current.

This scheme has 3 problems.

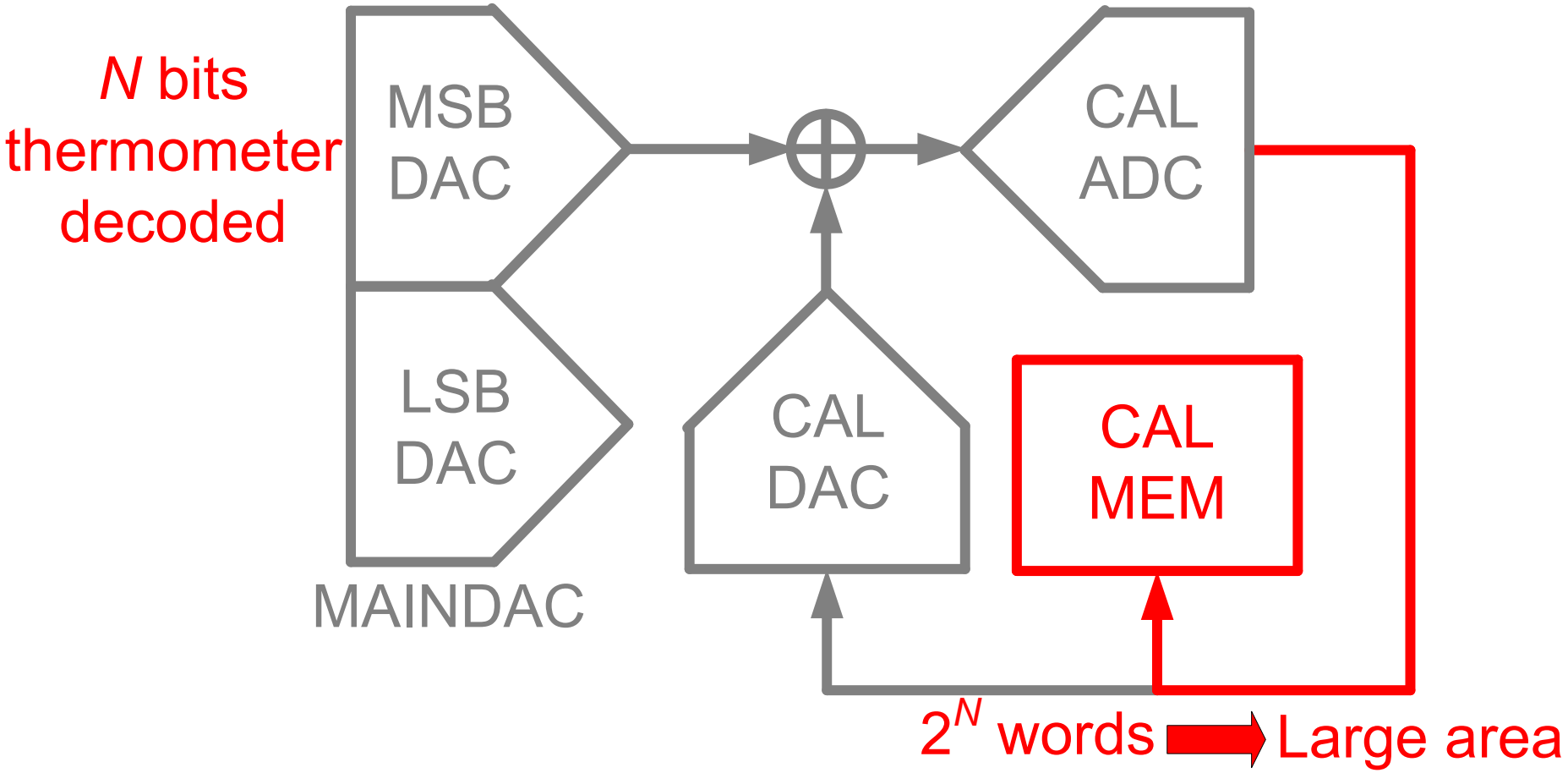
The problem of CALADC



- CALADC needs a high resolution, such as 16 bits

1. Complexity
2. Long calibration time
3. Large area

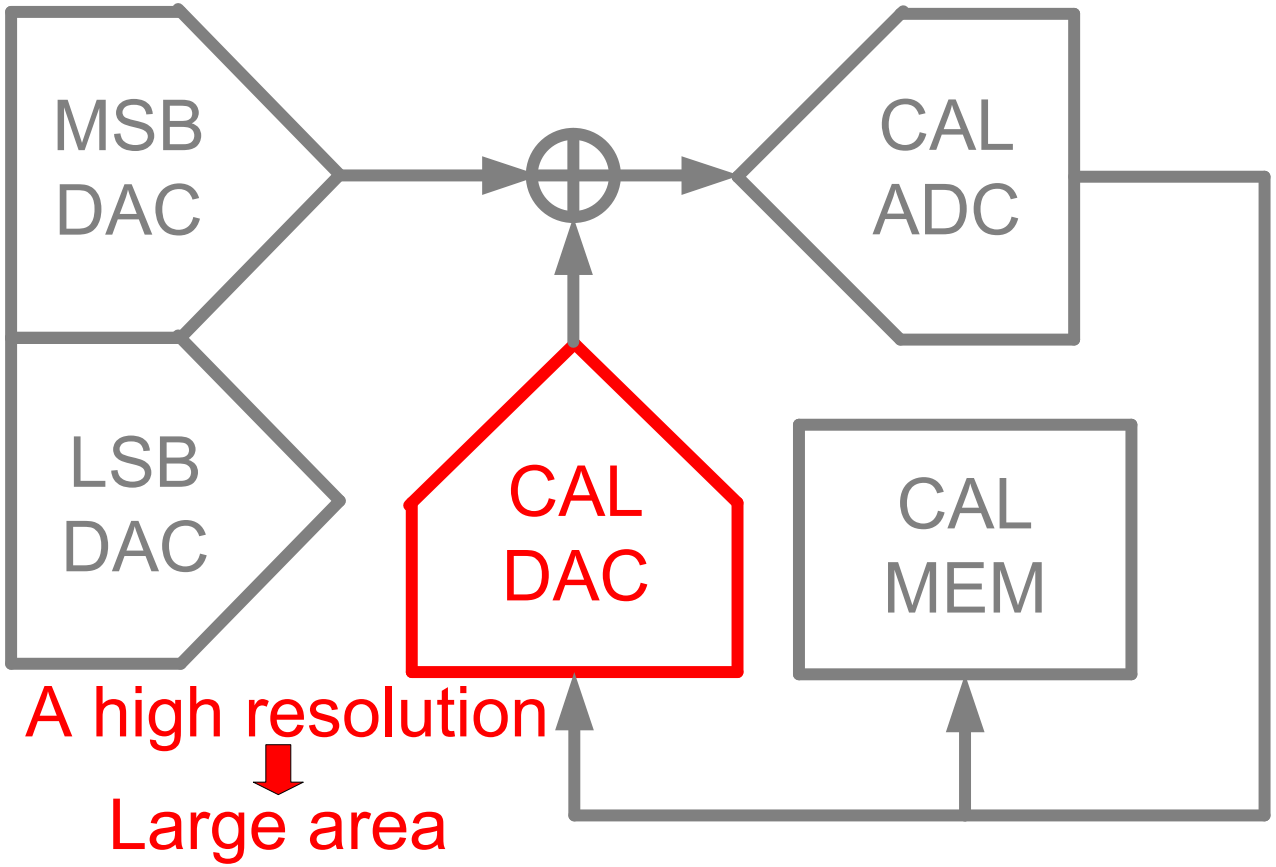
The problem of CALMEM



- A lot of calibration memory, 2^N words are required.

1. Slow operation speed
2. Large area

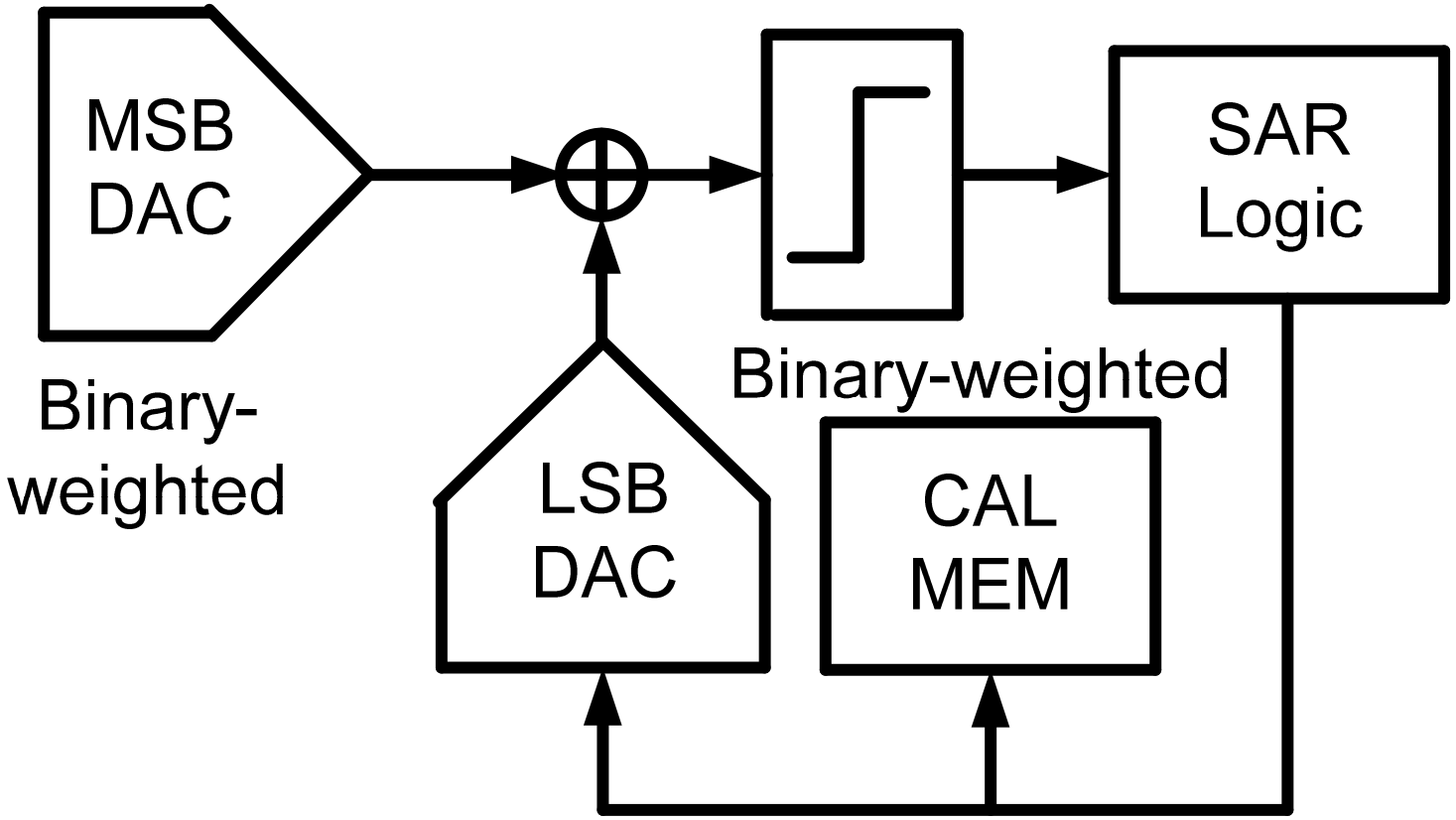
The problem of CALDAC



- If we keep MAINDAC small, the mismatch becomes large.
- CALDAC needs a high resolution, such as 10 bits.

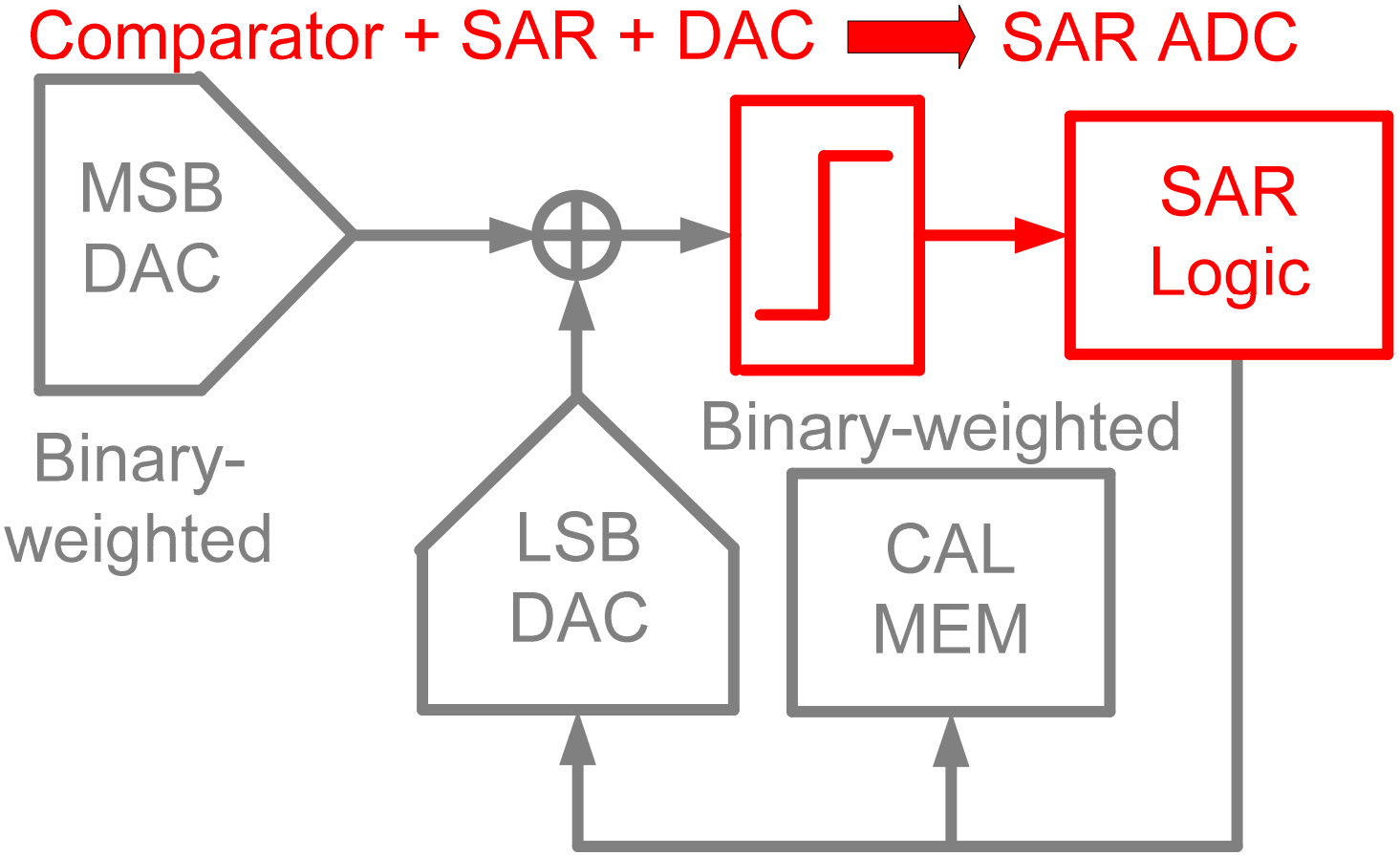
Large area

The proposed calibration



1. Mismatch currents are measured by the current comparator.
2. The error currents are stored in CALMEM, a lower capacity.
3. LSBDAC, in the part of MAINDAC corrects the error current.

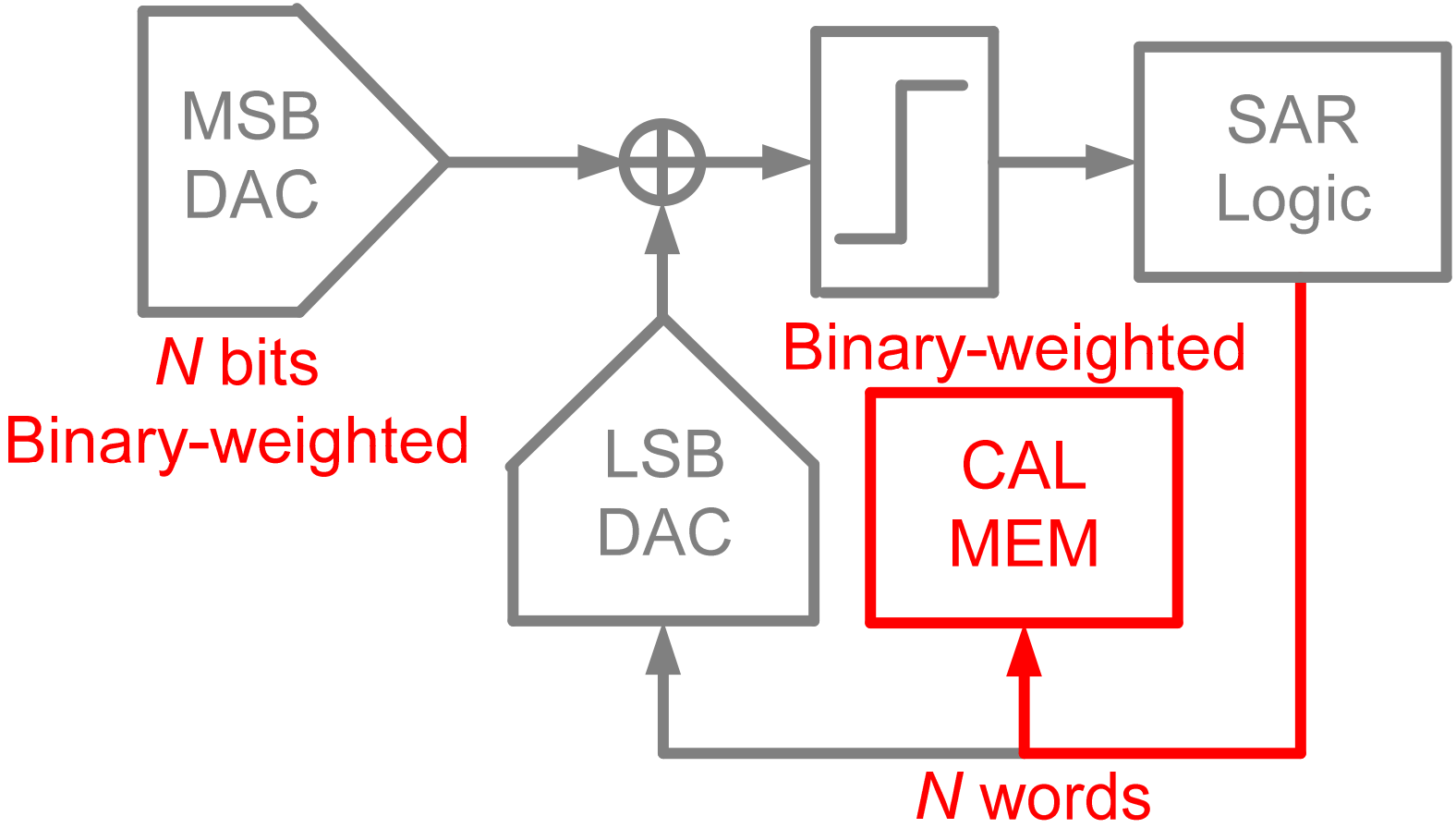
The proposed CALADC



- By using a current comparator and SAR logic, the error currents can be measured like in a SAR ADC

1. Simplicity
2. Short calibration time
3. Small area

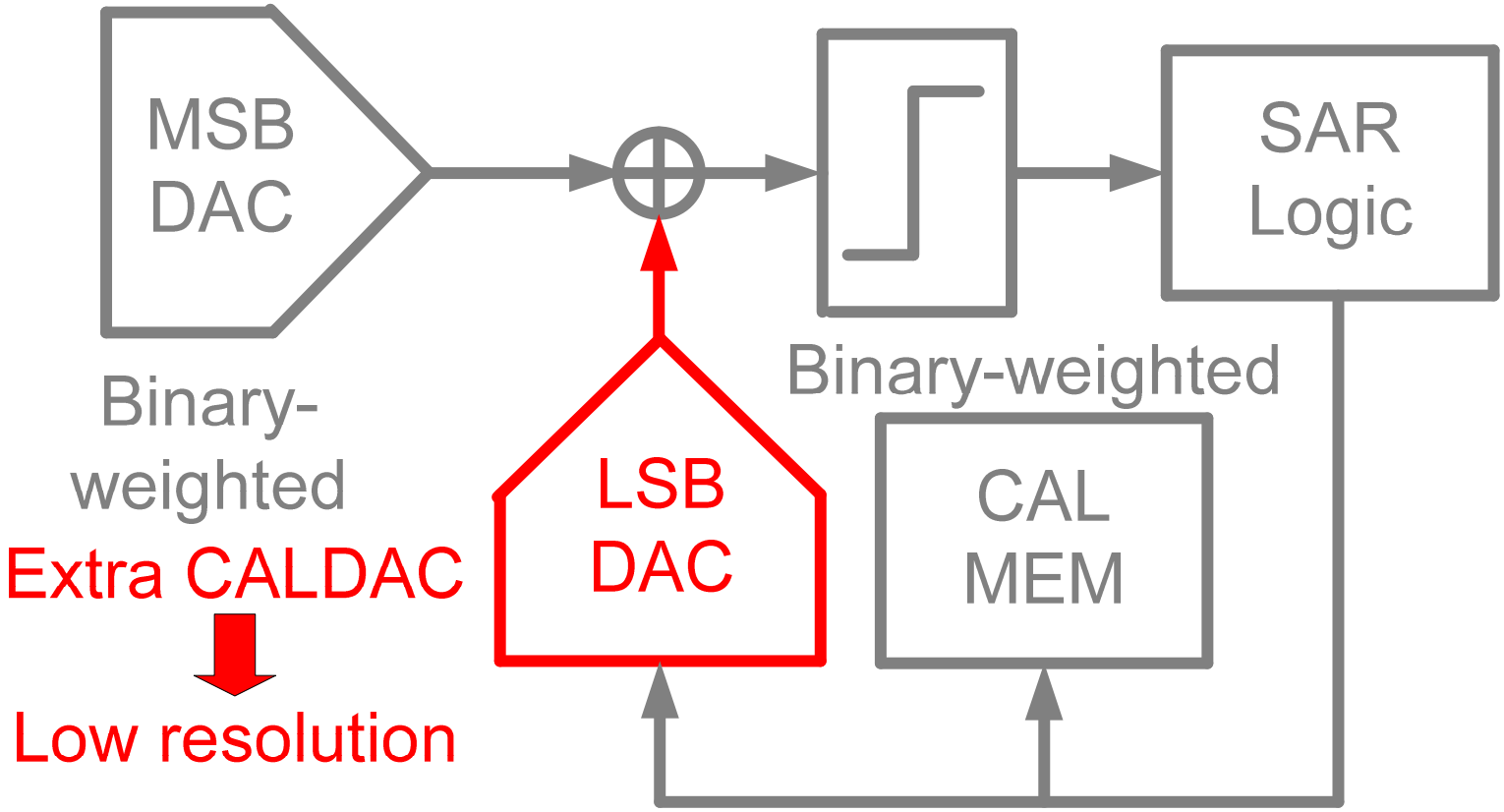
The proposed CALMEM



- N current sources instead of 2^N current sources
- CALMEM allows a lower capacity, N words instead of 2^N words

1. Fast operation speed
2. Small area

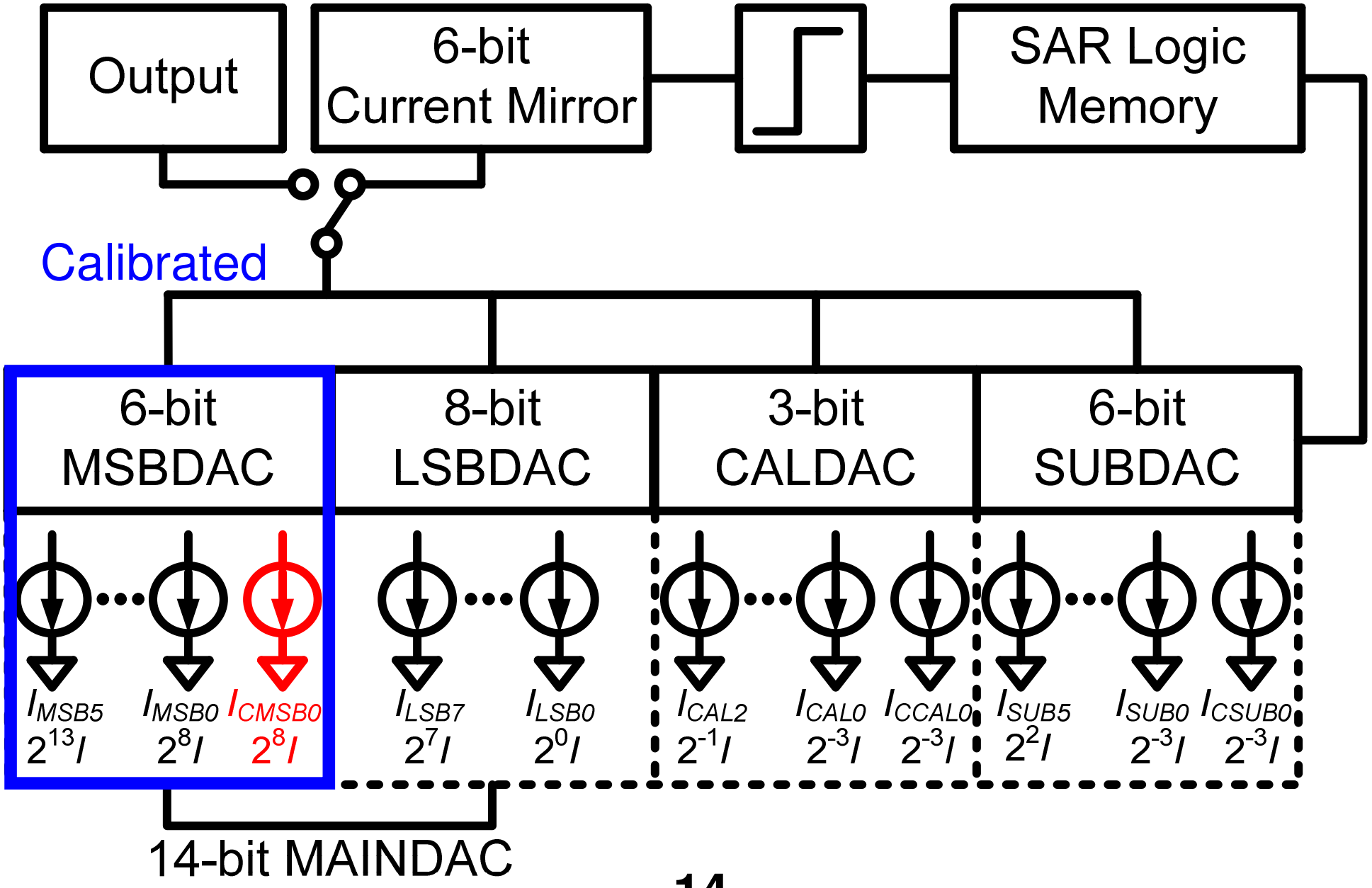
The proposed CALDAC



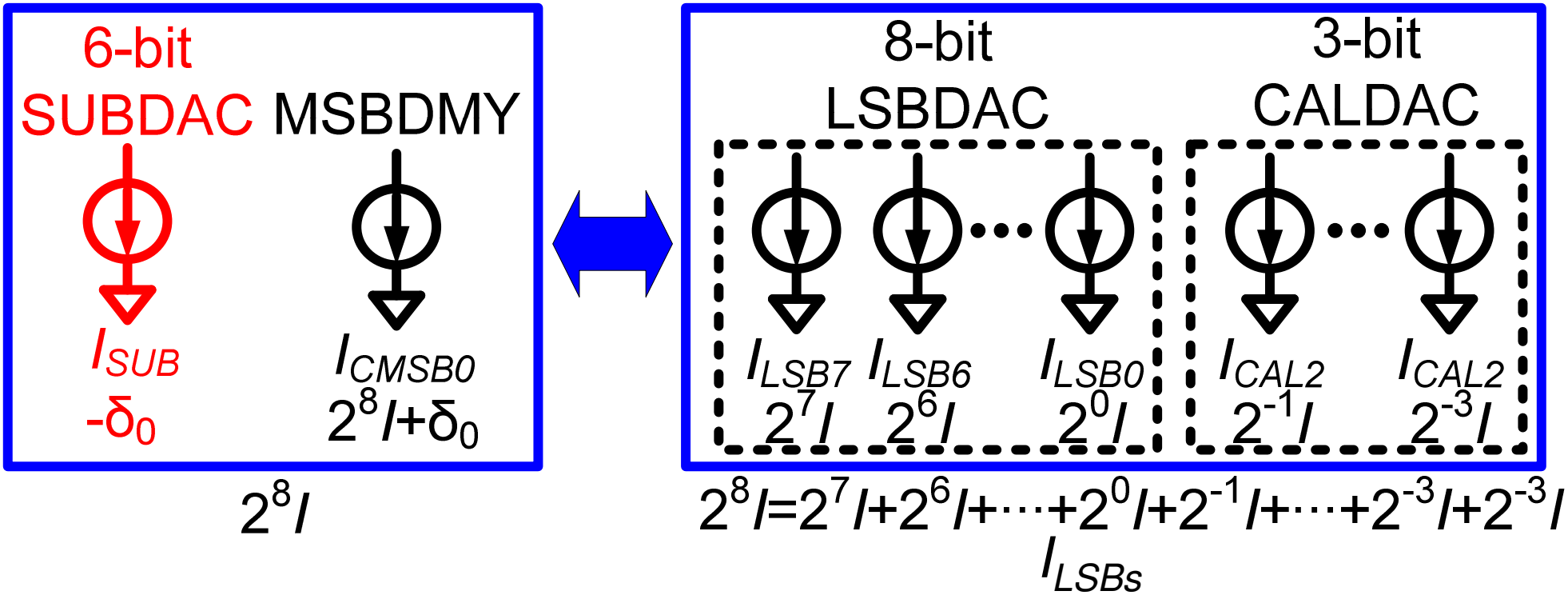
- The error currents of MSBDAC are corrected by LSBDAC, in the part of MAINDAC
- LSBDAC has a high resolution, such as 8bits

1. Extra CALDAC allows a low resolution
2. Small area

The proposed DAC

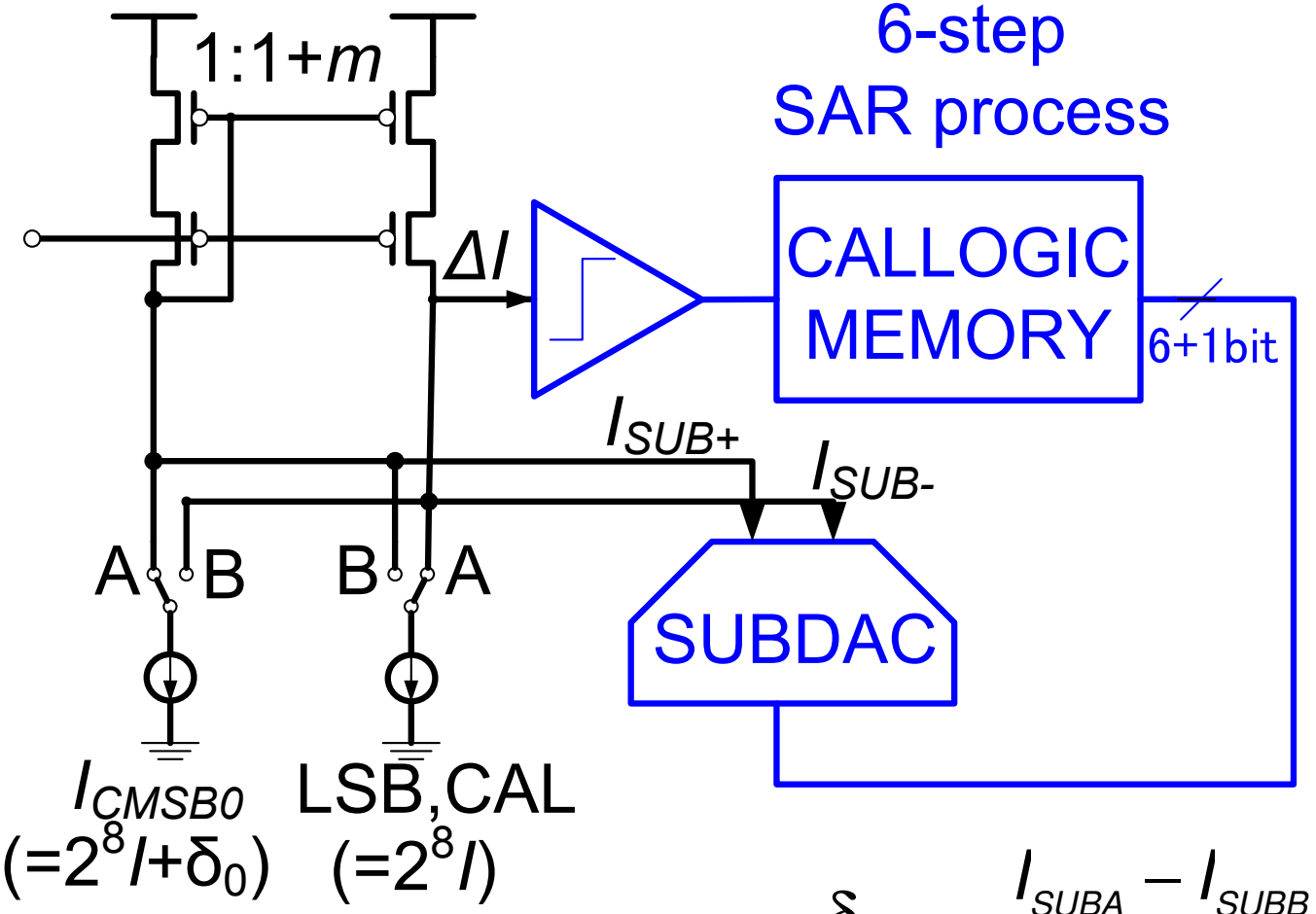


MSB dummy calibration



- Comparing MSB dummy current(I_{CMSB0}) with the sum of the LSBDAC and CALDAC current (I_{LSBs})
- SUBDAC is controlled to cancel out the error current, δ_0
- δ_0 is obtained as a 6-bit digital value.

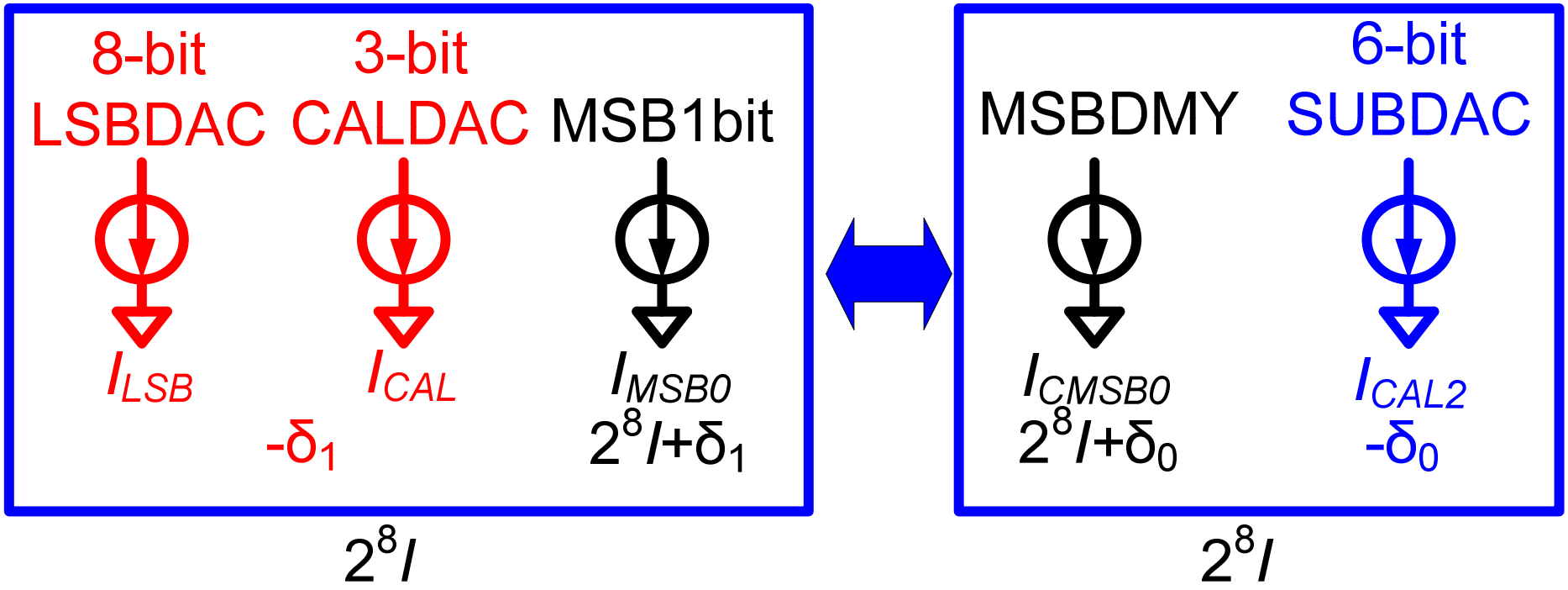
MSB dummy calibration



$$\delta_0 = -\frac{I_{SUBA} - I_{SUBB}}{2}$$

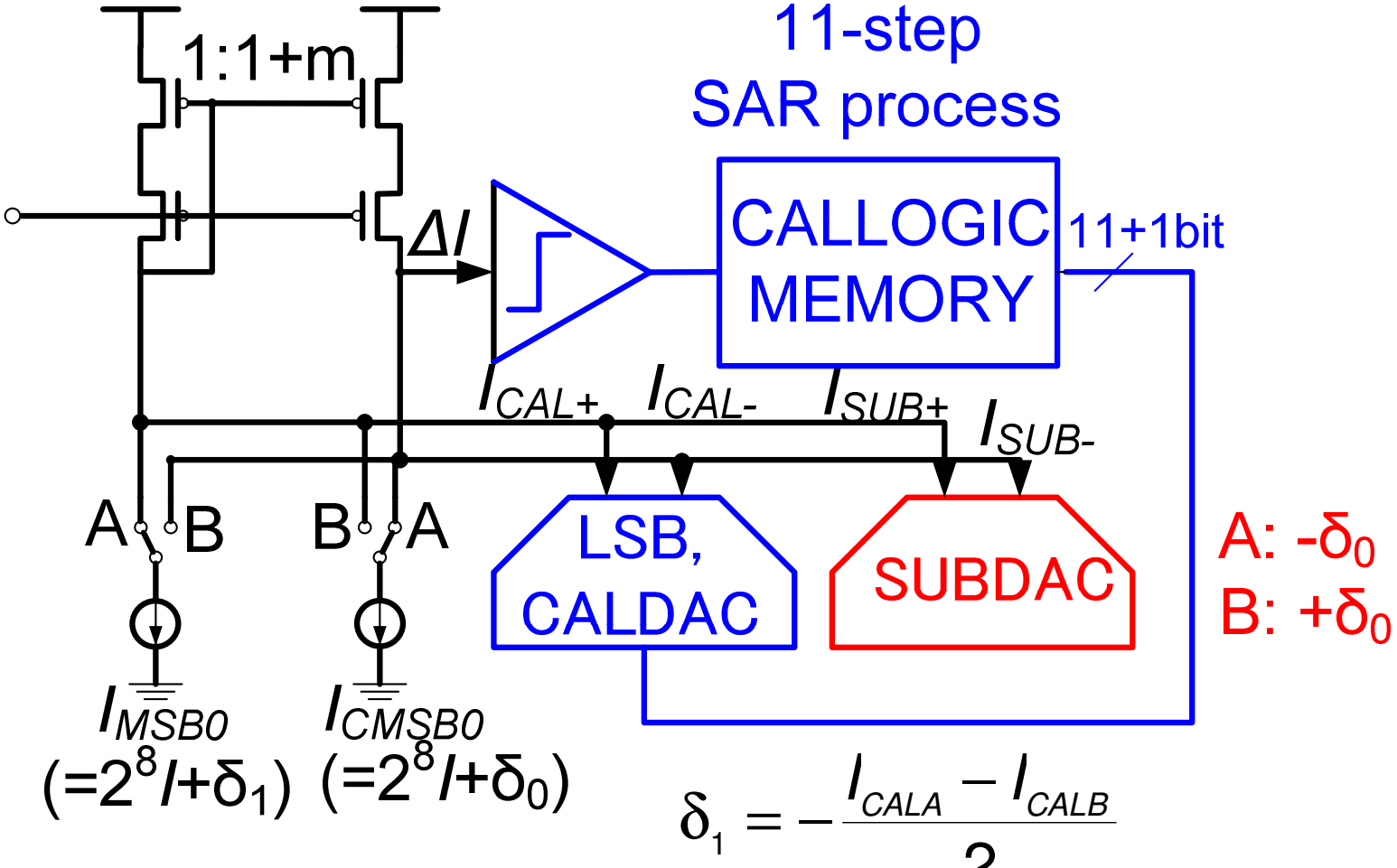
- Comparing I_{CMSB0} with the total current, I_{LSBs}.
- Current mirror mismatch and comparator offset are canceled by changing the switch position.

MSB calibration



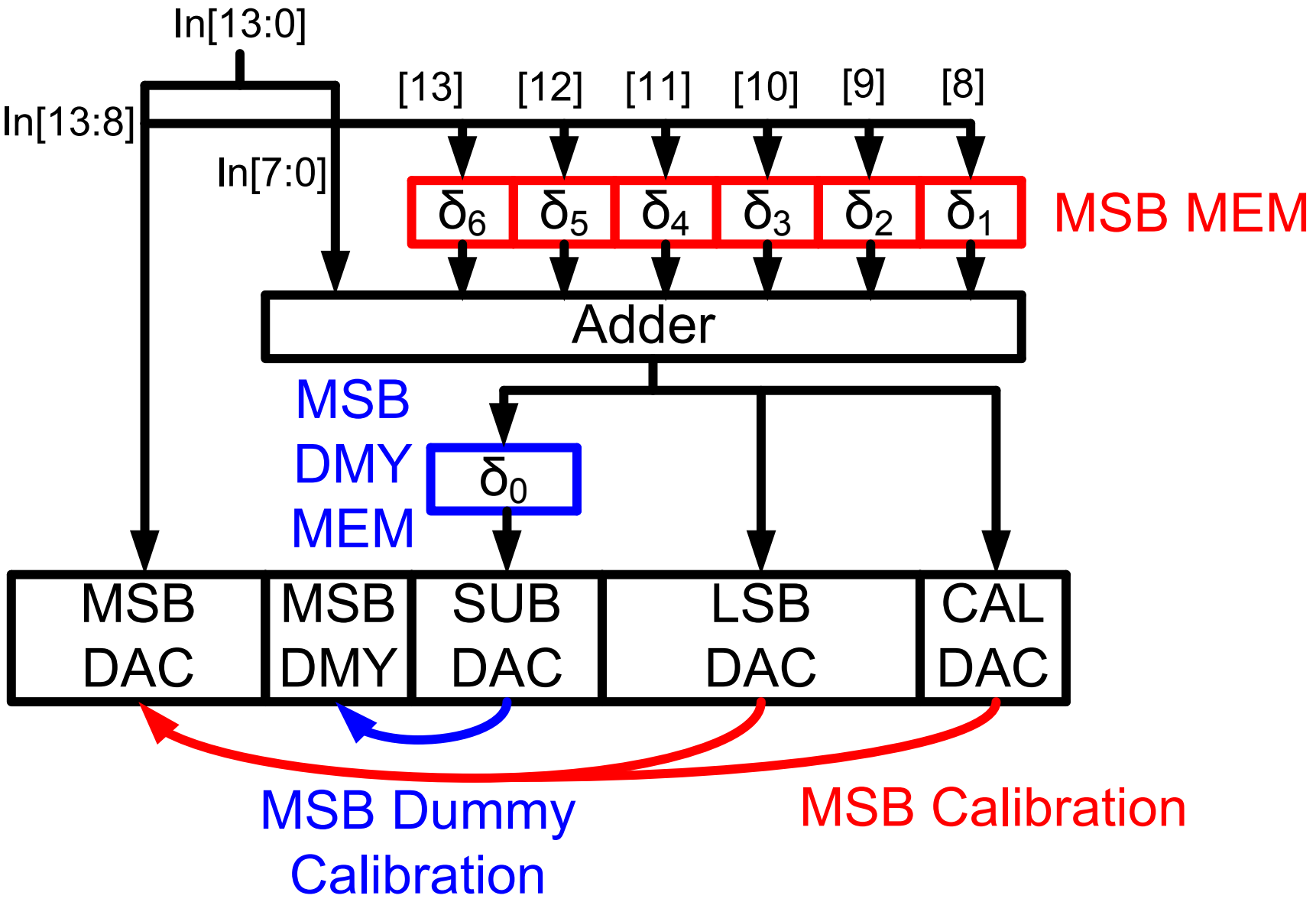
- Comparing the lowest MSBDAC current (I_{MSB0}) with the MSB dummy current (I_{CMSB0}) calibrated by SUBDAC.
- LSB, CALDAC are controlled to cancel out the error current, δ_1
- δ_1 is obtained as an 11 bit digital value.

MSB calibration



- Comparing I_{MSB0} with I_{CMSB0} calibrated by SUBDAC
- Current mirror mismatch and comparator offset are canceled by changing the switch position.

The conversion operation



The comparison with others

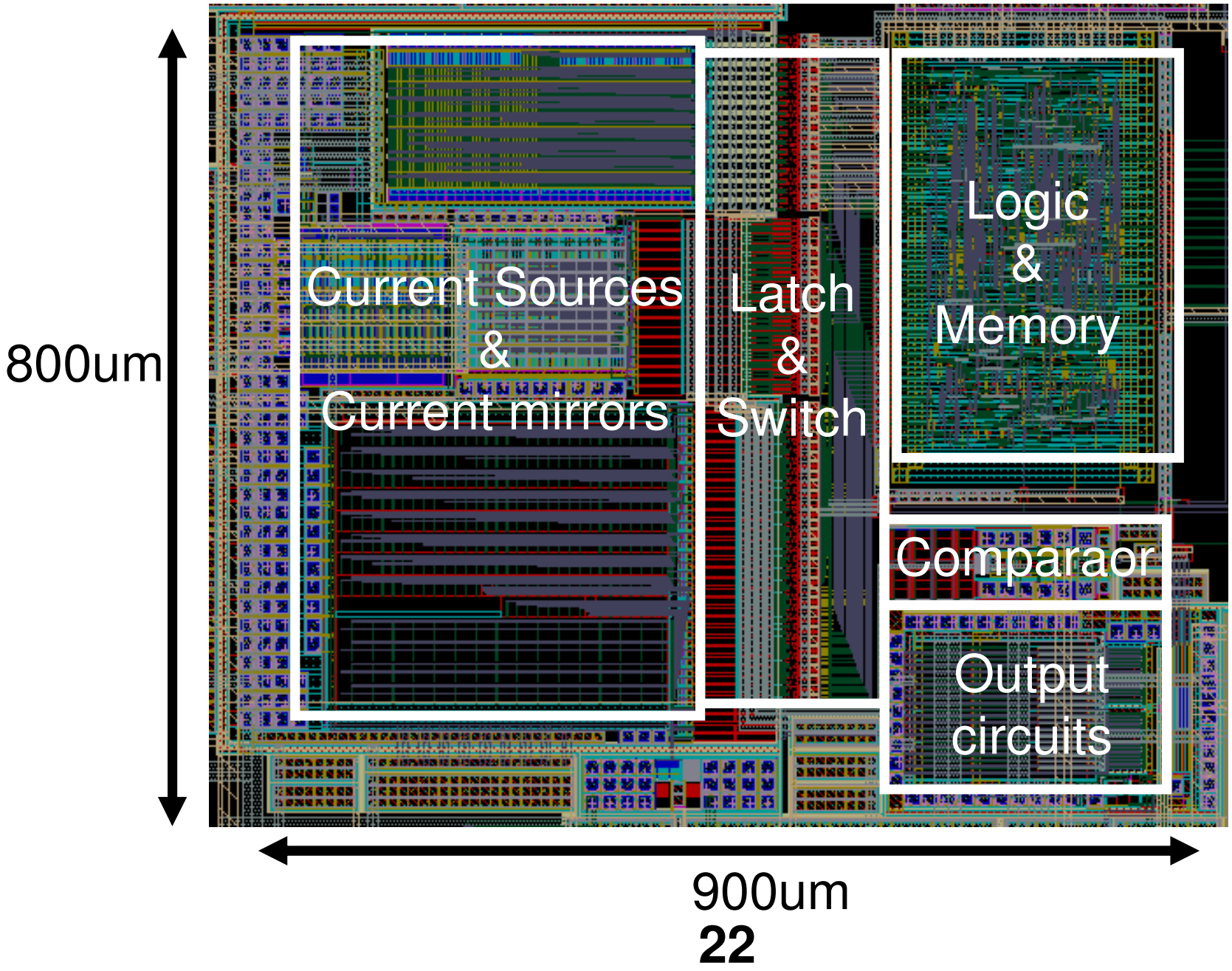
14-bit digital calibration scheme

Conference	CALADC	CALDAC	MemoryBit	CALBit	Area
VLSI'06	On Chip ΣΔADC	8bDAC ×16	8×16	4	2.88mm^2
ISSCC'03	Off Chip ΣΔADC	8bDAC +6bDAC	8×63	6	*0.1mm^2
ISSCC'01	On Chip ΣΔADC	12bitDAC	12×15	4	11.8mm^2
JSSCC'01	Current Comp.	6bDAC ×4	6×4	4	1mm^2
This Work	**Current Comp.**	**6bDAC +3bDAC**	**11×6**	**6**	**0.74mm^2**

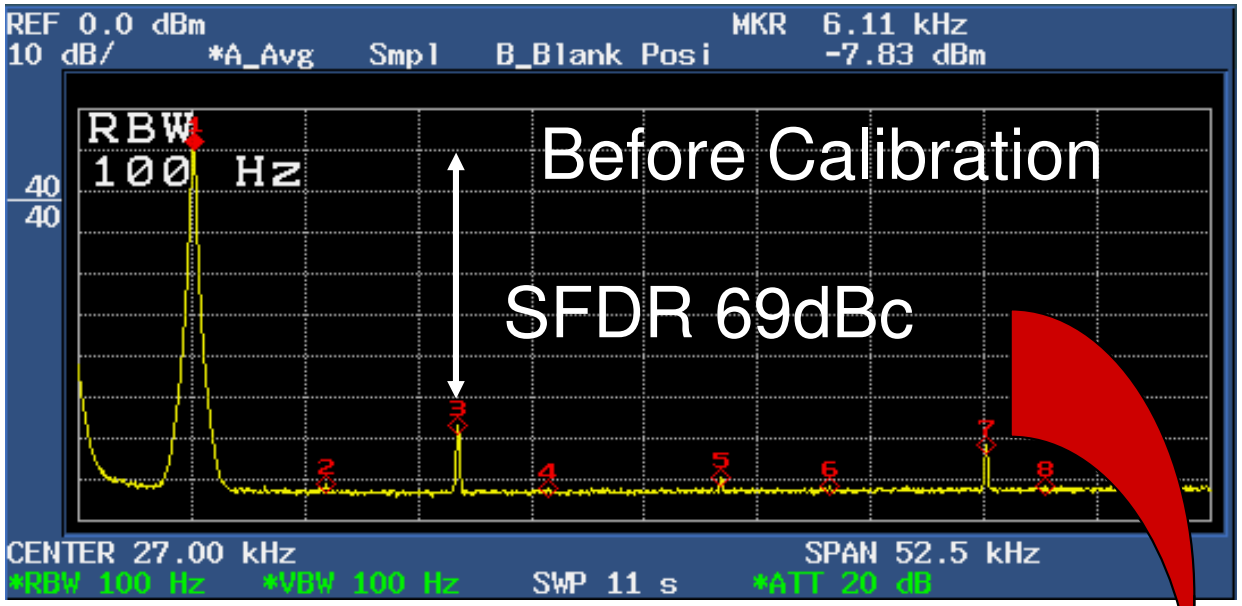
Outline

- Motivation
- The Calibration Scheme
- **Measurement Results**
- Conclusions

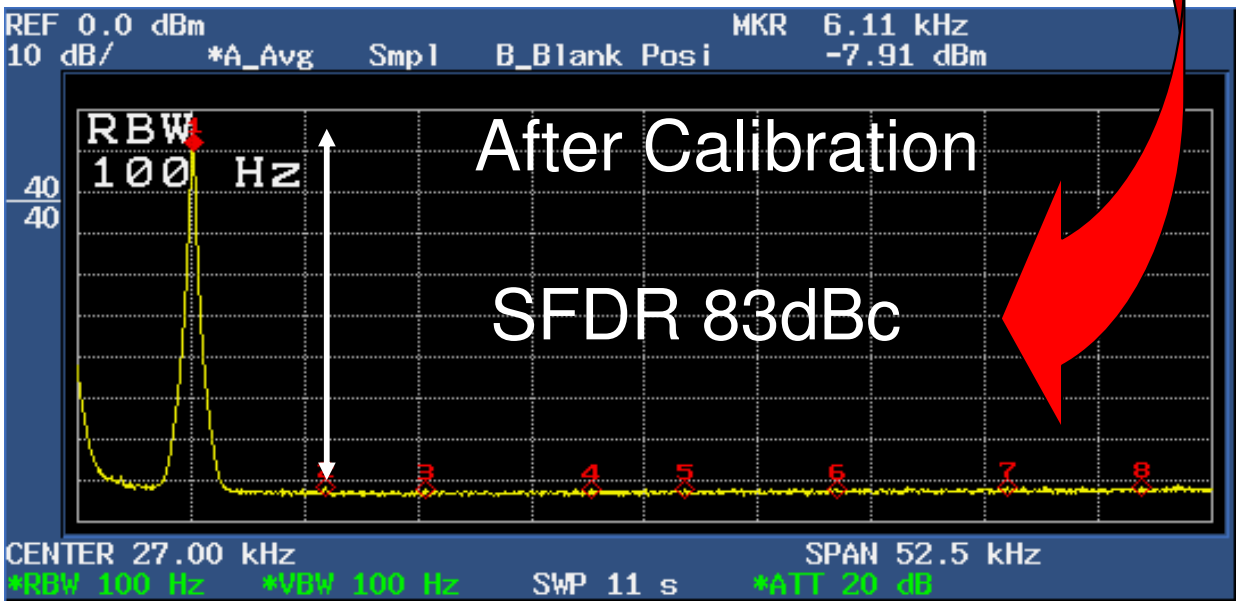
Layout (0.18um CMOS)



The Measurement Results

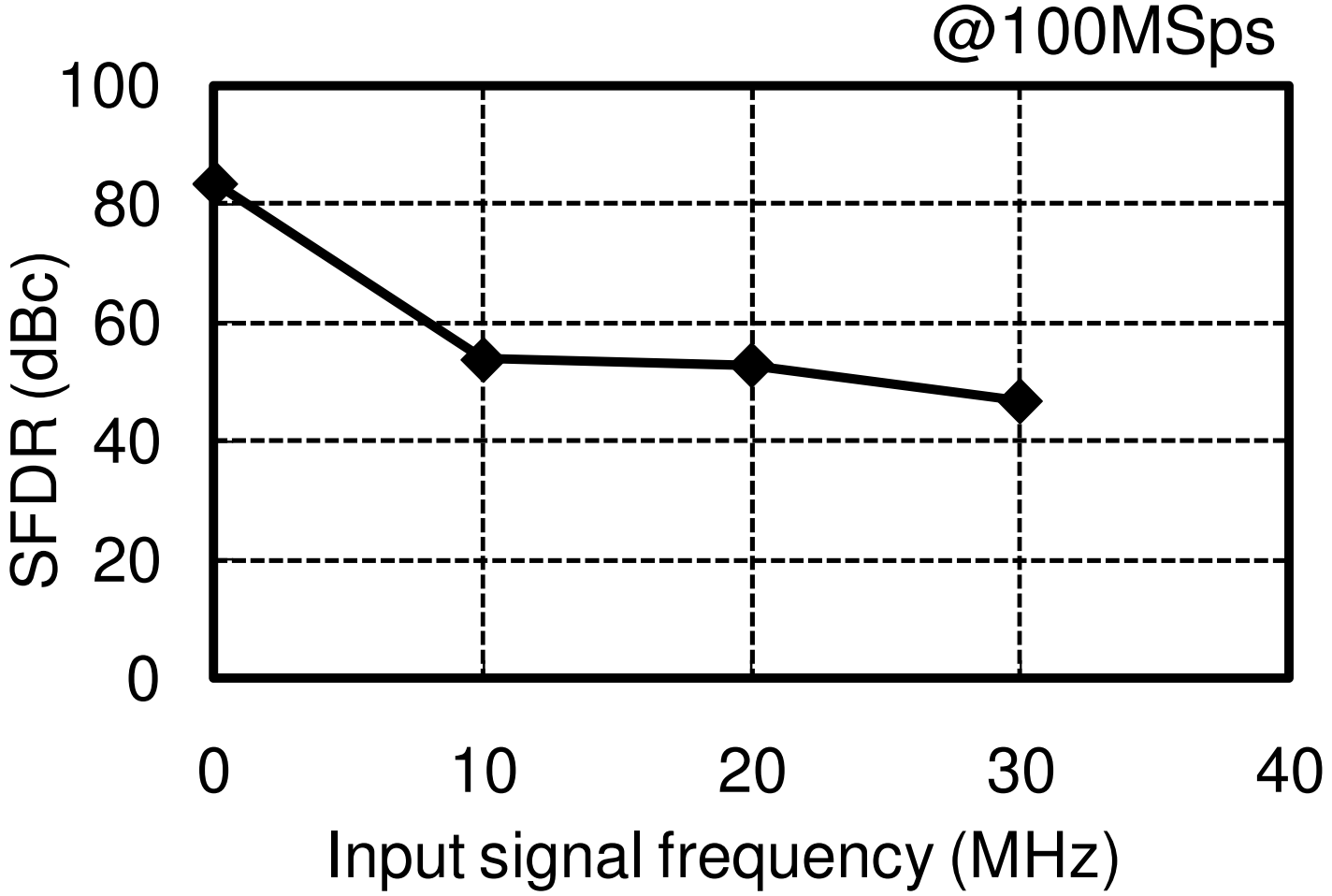


@100MSps
6kHz Signal



SFDR
14dBUP

The Measurement Results



- For high frequencies, SFDR degrades.
  It can be improved by return-to-zero circuits

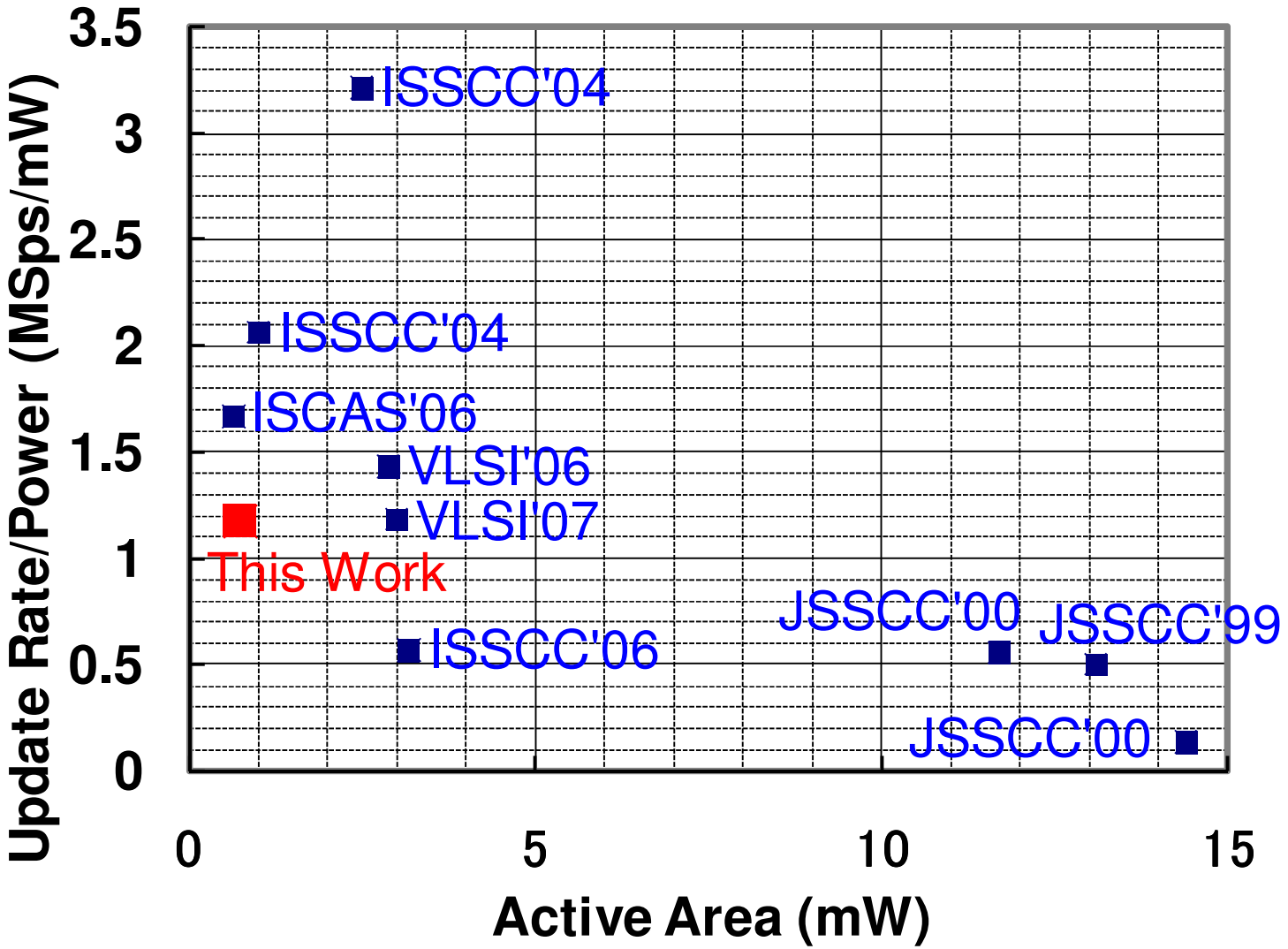
The Performance Summary

Tecnology	0.18 um CMOS
Resolution	14 bit
Update Rate	100 MSps
Full-Scale Current	11.5 mA
Supply Voltage	1.8 V
SFDR (Before Calibration)	69.2 dBc @fsig=6kHz
SFDR (After Calibration)	83.4 dBc @fsig=6kHz 46.6 dBc @fsig=30MHz
Power Consumption	79.2 mW (analog) 5 mW (digital)
Active Area	0.74 mm^2

Outline

- Motivation
- The Calibration Scheme
- Measurement Results
- **Conclusions**

The Comparison with other DACs



Conclusions

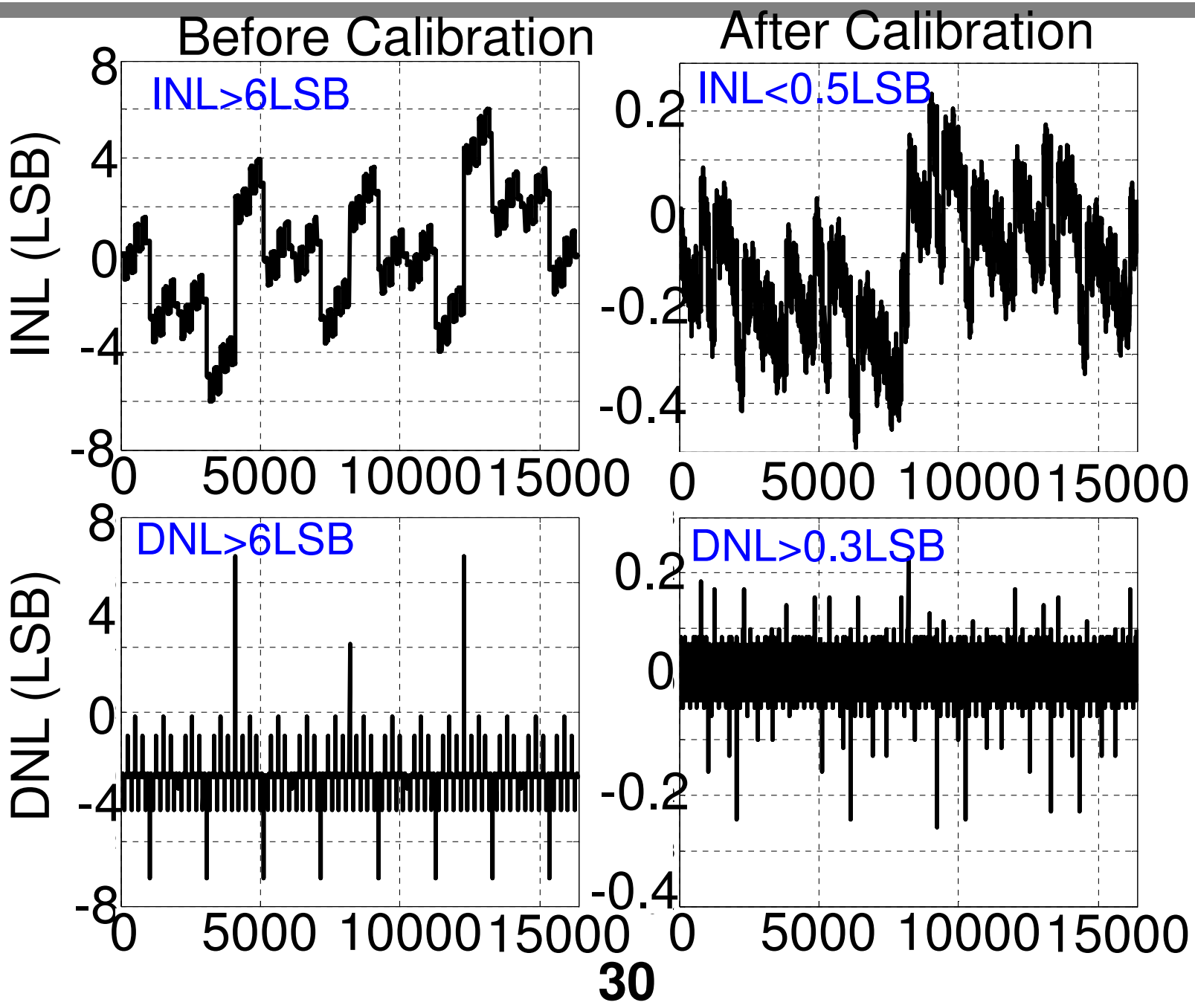
- **A new digital calibration scheme for a current-steering DAC has been proposed.**
- **By using a current comparator and the LSB part of the DAC for error correction, the additional circuits are kept minimal.**
- **Before calibration, the SFDR is 69.2 dBc. After calibration, the SFDR is greatly improved to 83.4 dBc.**

Thank you
for your interest

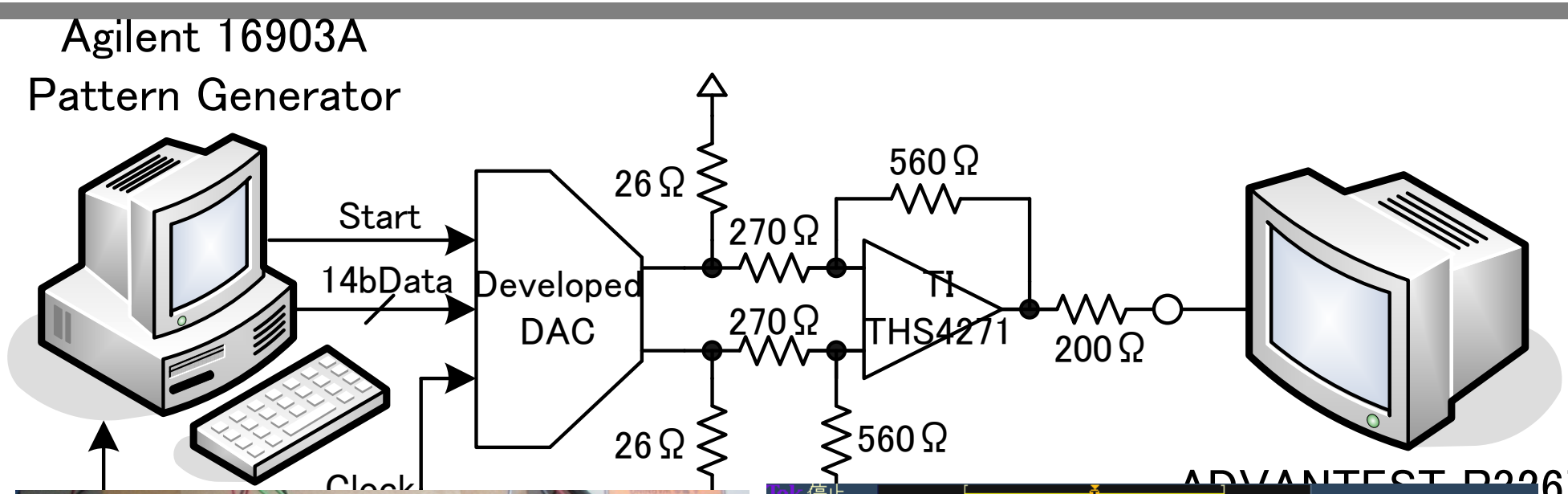
Yusuke Ikeda,
Yusuke.ikeda311@gmail.com

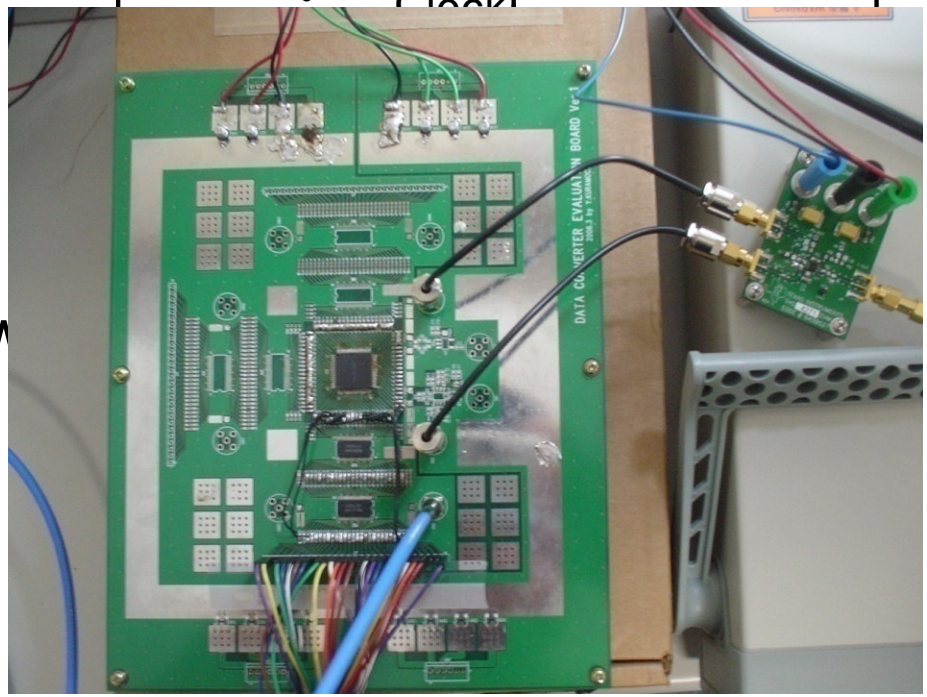
Matsuzawa
& Okada Lab.

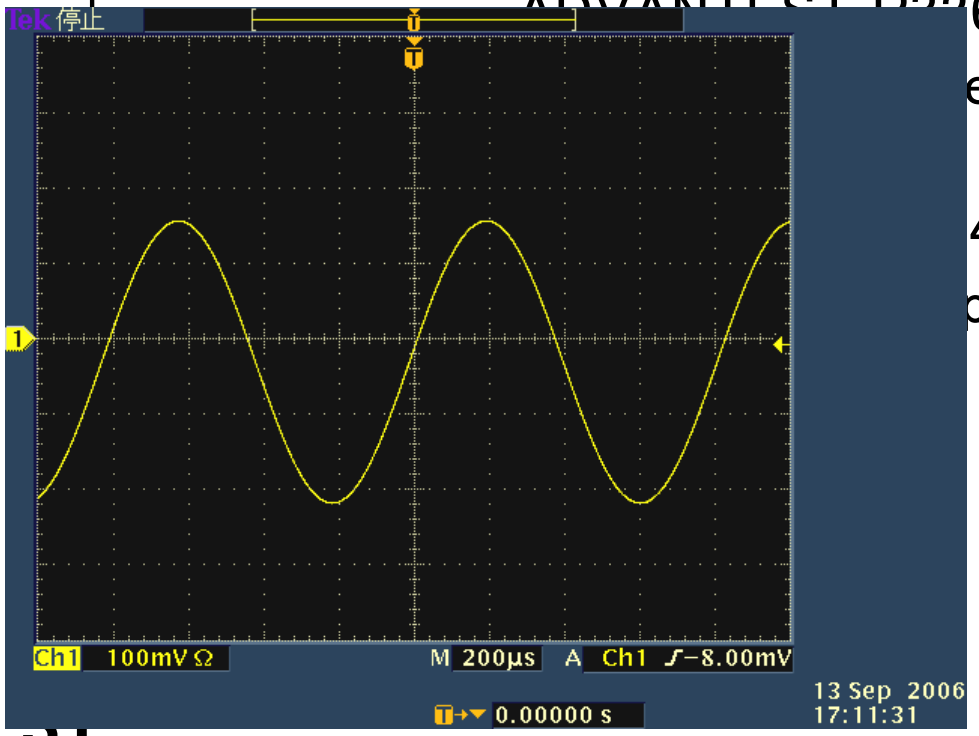
The Simulation Results



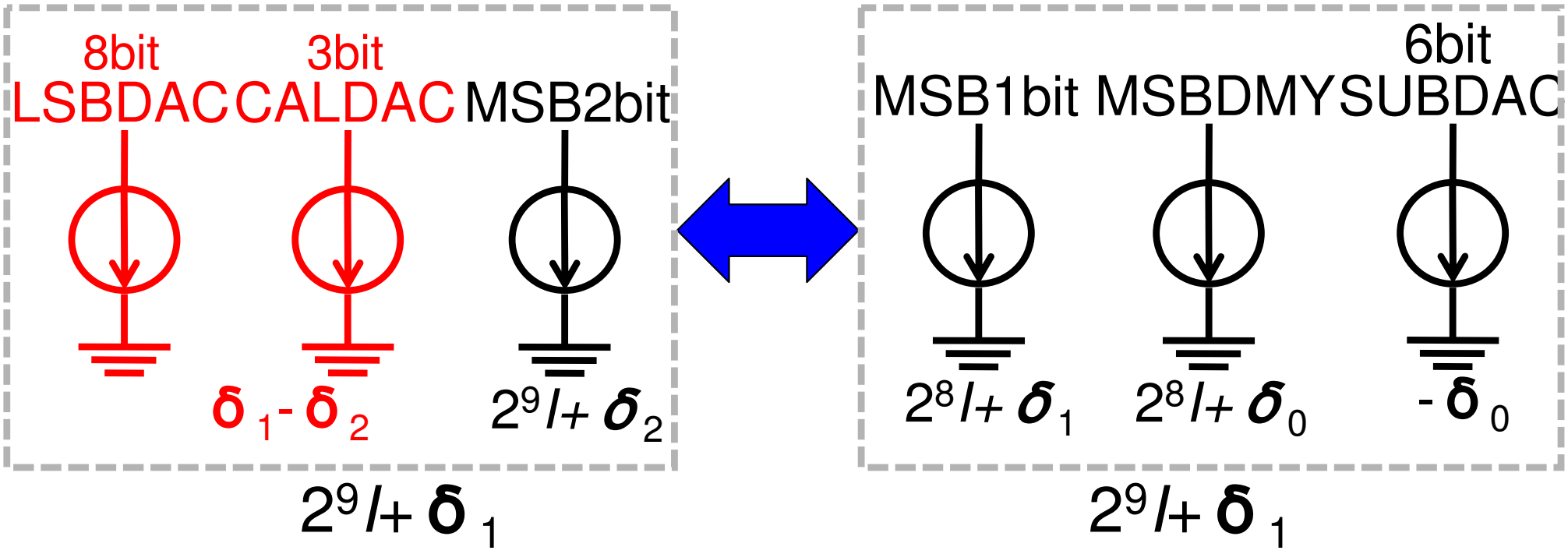
The Measurement Circuit



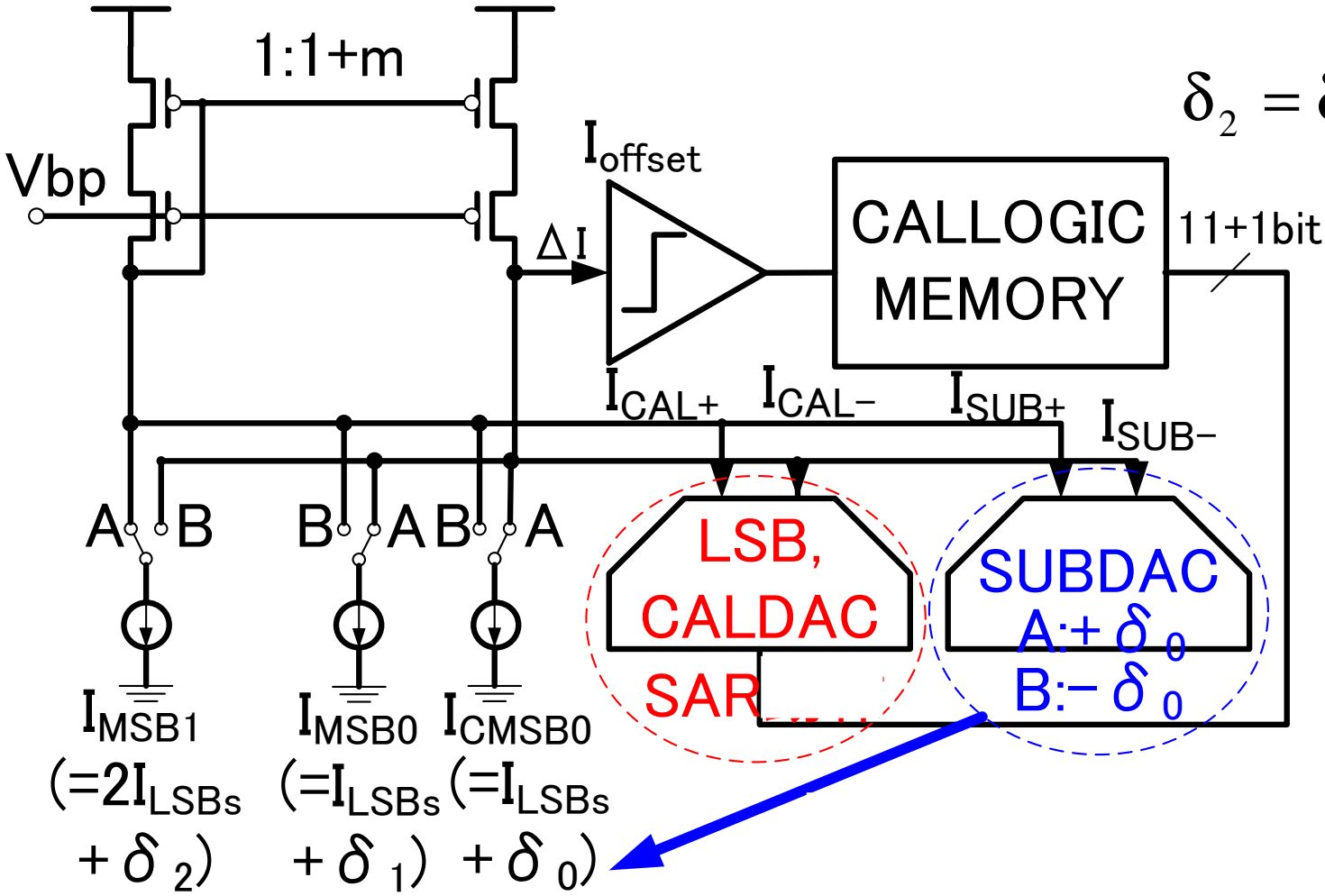




MSB Calibration 2



MSB Calibration



$$\delta_2 = \delta_1 - \frac{I_{CALA} - I_{CALB}}{2}$$

$$\delta_{N+1} = \sum_{i=1}^{N} \delta_i - \frac{I_{CALA} - I_{CALB}}{2}$$