Dynamic Reconfigurable Si CMOS VCO Using a Transmission-Line Resonator with PMOS-Bias and PMOS-Crosscouple Topology

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ABSTRACT

This paper proposes a low-phase noise CMOS VCO for more than 10 GHz oscillation, which utilizes a PMOS-bias and PMOS-crosscouple topology. PMOS transistors have lower $1/f$ noise while they have larger gate capacitance. In this work, a transmission-line resonator is employed to enhance the high-frequency operation. The VCO is fabricated by a 180 nm Si CMOS process. A phase noise is -112.6 dBc/Hz, and frequency tuning range is 11.8 GHz–12. 4GHz. Power consumption is 8.6 mW. Figure of Merit is -184.9 dBc/Hz.

I. INTRODUCTION

A Voltage controlled oscillator (VCO) is an essential building block in an analog RF front-end of wireless communication. As gate length of CMOS transistors gets shrunk, Si CMOS VCO can obtain higher-frequency oscillation. However, there are several obstacles to realize CMOS RF circuits while the low fabrication cost of CMOS chips is quite attractive. For example, lower f_{T} and $f_{\max}$, larger $1/f$ noise, lower breakdown-voltage, and larger process fluctuation are unavoidable problems in CMOS transistors. In particular, larger $1/f$ noise and process fluctuation are serious problems for high-frequency VCOs, *e.g.*, more than 10 GHz, which cause process variation in oscillating frequency and degradation in phase-noise characteristics. To compensate such the variation and the fluctuation, the reconfigurability of VCO is an indispensable requirement. As one of the solutions, we propose a reconfigurable RF circuit technology [1], which is realized by the dynamic reconfiguration due to digital control circuits. Very wide-tuning CMOS VCOs using the reconfigurable technique, *e.g.*, 0.98 GHz to 6.6GHz [2] and 0.49 GHz to 6.5GHz [3], have been reported. However, reconfigurable CMOS VCOs oscillating at more than 10 GHz have not been reported so far, because on-chip spiral inductors have low self-resonance frequency. PMOS transistors have better noise characteristics while PMOS transistors have larger parasitic capacitance. In recent CMOS processes, PMOS transistors have 4 times larger input capacitance than NMOS transistors at the same g_{m} condition. In this paper, we propose and analyze a PMOS-bias and PMOS-crosscouple VCO using a transmission-line resonator. The capacitance in transmission-line resonators is distributed, and the resonators have higher resonance frequencies. The PMOS topology contributes to improve phase-noise performance, and the transmission-line resonator realizes higher oscillating frequencies. In this paper, we demonstrate that the proposed VCO can perform superior characteristics from 10 GHz to 20 GHz.

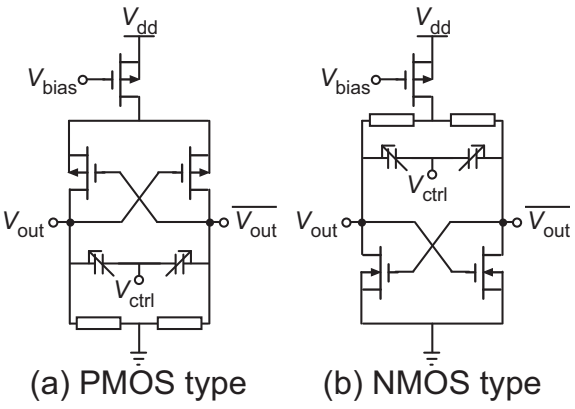

Fig. 1. Circuit schematics of VCO cores.

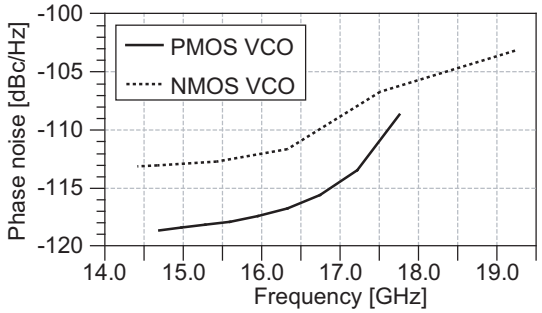

Fig. 2. Difference of phase noise between PMOS-type and NMOS-type VCOs.

II. CIRCUIT DESIGN OF VCO

As the oscillation frequency increases, phase noise also increases. It is important issue for more than 10 GHz VCO to have low phase noise. In this section, low phase noise VCO topologies are disscussed.

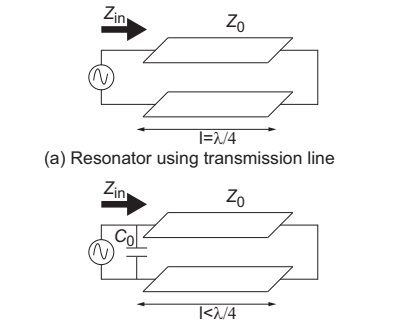

Fig. 3. Resonators.

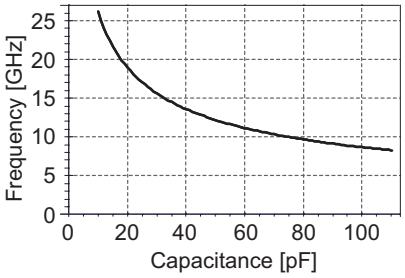

Fig. 4. Frequency characteristic calculated with ideal capacitance and transmission line.

A PMOS transistor is used as a current source in the VCOs because 1/f noise of PMOS transistors are smaller than that of NMOS's. The PMOS-crosscouple VCO as shown in Fig. 1(a), which oscillates at several GHz, has smaller phase noise than NMOS's in Fig. 1(b). However, there are trade-offs between PMOS-crosscouple and NMOS-crosscouple in more than 10 GHz VCOs. Because of channel mobility difference, $g_{\rm m}$ of NMOS transistors is 4 times larger than that of PMOS's. As the oscillation frequency increases, phase noise also increases and $g_{\rm m}$ decreases. To maintain oscillation, gate width of transistor and current flow are increased. Increase of parasitic capacitance along with gate width increase makes oscillation frequency lower, and increase of current flow degrades phase noise. Consequently, PMOS-crosscouple does not always have lower phase noise than NMOS at more than 10 GHz.

As shown in Fig. 2, phase noise characteristics of PMOS-crosscouple and NMOS-crosscouple are compared by using simulation results at more than 10 GHz. At less than 16 GHz, PMOS-crosscouple has lower phase noise than NMOS-crosscouple. At more than 16 GHz, phase noise increase rate of PMOS-crosscouple is larger than that of NMOS's, and both will be almost the same at 18 GHz. Moreover, PMOS type does not oscillate at more than 18 GHz in simulation. PMOS-bias and PMOS-crosscouple topology has lower phase noise than that of NMOS's at 12 GHz from simulation results. So, a PMOS-bias and PMOS-crosscouple topology 12 GHz VCO is demonstrated in this work.

In millimeter-wave VCOs, transmission lines are used as resonators as shown in Fig. 3(a). The capacitance in transmission-line resonators is distributed, and the resonators have higher resonance frequencies than on-chip spiral inductors.

Input impedance $Z_{\rm in}$ is calculated as follows.

$$\begin{aligned} Z_{\rm in} &= Z_0 \frac{Z_{\rm L} + jZ_0 \tan\beta l}{Z_0 + jZ_{\rm L} \tan\beta l}, \\ &= jZ_0 \tan\beta l = jZ_0 \frac{\sin\beta l}{\cos\beta l}, \end{aligned} \tag{1}$$

where Z_0 is characteristic impedance of transmission line, $Z_{\rm L}$ is load impedance, β is wave number, and l is line length. Here, $Z_{\rm L}$ is zero because it is shorted. At the resonance frequency, the denominator of Eq. (1) equals to zero. The resonance frequency with ideal transmission line is calculated as follows.

$$\cos\beta l = 0 \tag{2}$$

$$l = \frac{\lambda}{4} \tag{3}$$

However, wave length is several centimeters at more than 10 GHz, and line length l of several millimeters is required. Long transmission lines have large parasitic resistance, which degrades quality factor of resonators. In this work, transmission line and capacitance are used in the resonator of VCO as shown in Fig. 3(b).

Input impedance $Z_{\rm in}$ is calculated as follows.

$$\begin{aligned} Z_{\rm in} &= jZ_0 \tan\beta l /\!\!/ \frac{1}{j\omega C_0}, \\ &= \frac{jZ_0 \tan\beta l \times \frac{1}{j\omega C_0}}{jZ_0 \tan\beta l + \frac{1}{j\omega C_0}}, \\ &= \frac{jZ_0 \sin\beta l}{\cos\beta l - \omega C_0 Z_0 \sin\beta l}, \end{aligned} \tag{4}$$

where C_0 is capacitance added to the open side of transmission line. At the resonance frequency, the denominator of Eq. (4) equals to zero. Resonance frequency with ideal transmission line and capacitance is calculated as follows.

$$\begin{aligned} \cos\beta l - \omega C_0 Z_0 \sin\beta l &= 0 \\ -\sin(\beta l - \pi/2) &= \omega C_0 Z_0 \cos(\beta l - \pi/2) \\ -(\beta l - \pi/2) &\fallingdotseq \omega C_0 Z_0 \qquad (\because \beta l - \pi/2 \ll 1) \end{aligned}$$

$$l \fallingdotseq \frac{\lambda}{4} - C_0 Z_0 v \quad (\because \beta = \frac{2\pi}{\lambda} = \frac{\omega}{v}) \tag{5}$$

From Eq. (5), the resonance frequency is decreased by C_0, which is confirmed by a simulation using 500 μm ideal transmission line and ideal capacitance. Fig. 4 shows the simulation results. Fig. 1(a) shows circuit schematic of VCO. The transmission line has coplanar wave guide structure, and a NMOS varactor is used as C_0 to tune oscillation frequency. Fig. 5 shows circuit schematic of the output IO buffer. The output power of VCO is low, so a stacked PMOS common-source amplifier is used.

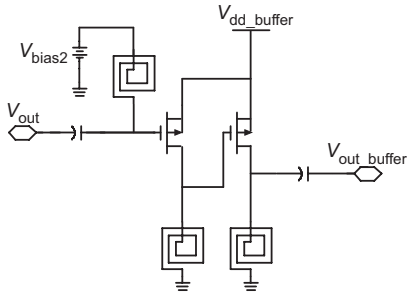

Fig. 5. Circuit schematic of IO buffer.

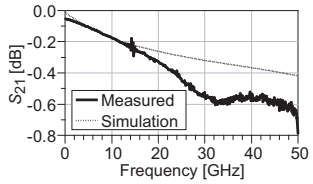

Fig. 6. Magnitude of S_{21}.

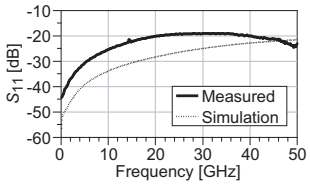

Fig. 7. Magnitude of S_{11}.

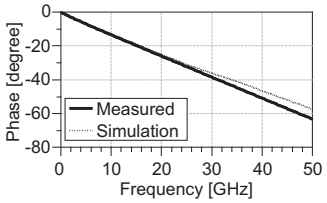

Fig. 8. Phase of S_{21}.

III. Experimental results

The proposed VCO is fabricated by using a 180 nm Si CMOS process with 6 aluminum layers. The configurations of the transmission line are the coplanar wave guide, 500 μm of length, 5 μm of width, 5 μm of gap, and characteristic impedance is 50 Ω.

A. Transmission Line

Electrical length of transmission line is greatly affected by parasitic capacitances and resistivity of Si substrate. Simulation of transmission line is performed by the electromagnetic simulator HFSS (Ansoft Co., Ltd.). To characterize transmission lines, a TEG of transmission line is fabricated and measured.

Parasitics of RF pads are de-embedded by using measured open and short patterns. Figs. 6, 7, and 8 show magnitude of S_{21} and S_{11}, and phase of S_{21}, respectively. As shown in Fig. 6, both of S_{21} are similar to each other at less than 15 GHz. As shown in Fig. 7, the measured S_{11} is almost 8 dB larger than that of simulation. As shown in Fig. 8, the measured phase of S_{21} agree with to the simulation results at less than 25 GHz.

B. VCO

Fig. 9 shows a chip micrograph of the fabricated VCO. Fig. 10 shows oscillation frequency, and Fig. 11 shows phase noise. Simulation results are obtained by using EDA (Agilent ADS), and the measured results of transmission line is used in this simulation. The VCO is measured by using a signal source analyzer (Agilent E5052A) and a 1/2 frequency divider (NEL MOD08).

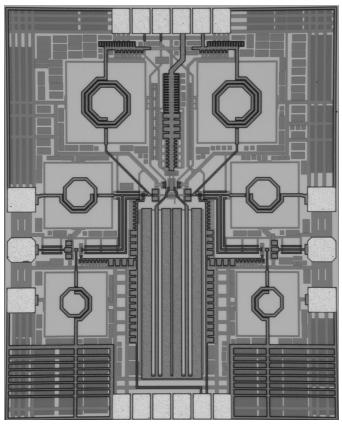

Fig. 9. Microphotograph of the proposed VCO.

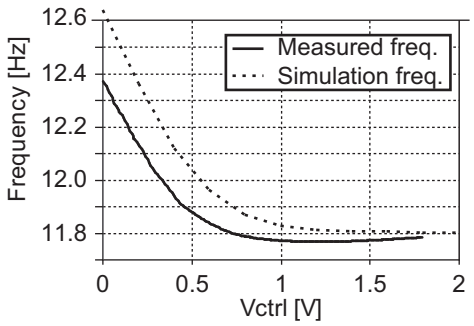

Fig. 10. Oscillation frequency.

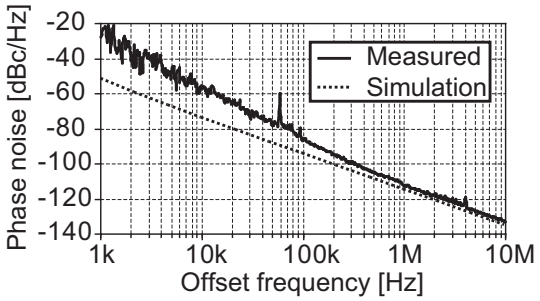

Fig. 11. Phase noise.

Measured frequency tuning range is 11.8 GHz to 12.4 GHz. On the other hand, simulated oscillation frequency range is from 11.8 GHz to 12.6 GHz. Measured phase noise is -112.6 dBc/Hz at a 1 MHz offset for an 11.8 GHz carrier frequency. Power consumption is 8.6 mW. Figure of Merit of VCO is -184.9 dBc/Hz, which is calculated by the following equation.

$$FoM = L\{f_{\rm offset}\} - 20\log\left(\frac{f_0}{f_{\rm offset}}\right) + 10\log\left(\frac{P_{\rm DC}}{1{\rm mW}}\right), \quad (6)$$

TABLE I

VCO PERFORMANCE COMPARISON.

Reference	Topology	Frequency	P_{out} [dBm]	Phase Noise [dBc/Hz]	f_{offset} [MHz]	P_{DC} [mW]	Technology	FoM
[4]	Injection locked	39.2–40.3	−8	−108.7	1	6.0	0.18 μm Si CMOS	−192.9
[5]	LCVCO	10.18–11.37		−118.7	1	11.8	0.18 μm Si CMOS	−188.6
This Work	TLVCO	11.8–12.4	−7.5	−112.6	1	8.6	0.18 μm Si CMOS	−184.9
[5]	LCVCO	19.84–22.01		−111.7	1	40.3	0.18 μm Si CMOS	−182.0
[6]	NMOS LCVCO	19.9		−111.0	1	32.0	0.18 μm Si CMOS	−181.9
[7]	LCVCO	11.2		−106.0	1	4.8	0.13 μm Si CMOS	−180.2
[8]	Distributed Oscillator	40		−99.0	1	27.0	0.18 μm Si CMOS	−176.7
[5]	LCVCO	39.33–43.67		−102.0	1	115.9	0.18 μm Si CMOS	−173.7
[9]	balanced VCO	21.9–22.33	−0.3	−108.2	1	140.0	InGaP/GaAs HBT	−173.6
[10]	Colpitts	23–24.4	–	−94.0	1	22.0	0.25 μm SiGe BiCMOS	−168.1
[11]	Varactorless VCO	23.2–29.4		−96.2	3	36.5	0.13 μm Si CMOS	−159.4
[12]	Distributed Oscillator	11.03–11.19	–	−84.0	1	9.0	0.35 μm Si Bipolar	−155.4

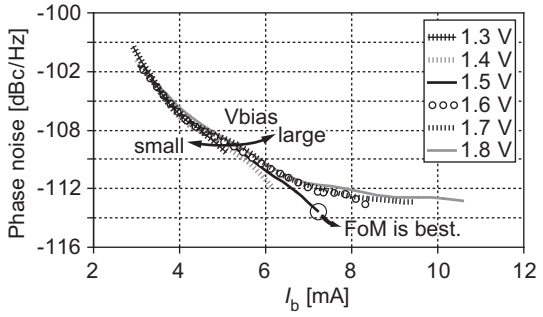

Fig. 12. Optimization of phase noise.

where f_0 is carrier frequency, $f_{\rm offset}$ is offset frequency, $L\{f_{\rm offset}\}$ is phase noise at $f_{\rm offset}$, and $P_{\rm DC}$ is power consumption. Table I summarizes the measurement results of this work and previous work. Fig. 12 shows phase noise as a function of bias current $I_{\rm b}$, and $V_{\rm dd}$ is varied from 1.3 V to 1.8 V. In general, fabricated VCOs have performance variation caused by the PVT variation, which is a serious problem, especially, in CMOS chips. Thus, the reconfigurability is very important in such the situation. The VCO presented in this paper has a reconfigurable bias port controled by a digital control circuit, and can be optimized to improve phase noise characteristics as shown in Fig. 12.

IV. CONCLUSION

This paper proposes a PMOS-bias and PMOS-crosscouple VCO using a transmission-line resonator toward a dynamic reconfigurable RF circuits. PMOS-crosscouple has lower $1/f$ noise than NMOS's for VCOs while PMOS transistors have 4 times larger gate capacitance. To realize low-noise VCOs at more than 10 GHz, a transmission-line resonator is employed and incorporated with a PMOS cross-couple pair, which has higher resonance frequency due to the distributed capacitance. It has been demonstrated that the VCO has 184 dBc/Hz of FoM.

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