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Dynamic Reconfigurable Si CMOS VCO Using a Transmission-Line Resonator with PMOS-Bias and PMOS-Crosscouple Topology

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Matsuzawa & Okada Lab.

1. Outline

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(1) Background

(2) Circuit topology of VCO

(3) Experimental results

(4) Conclusion

2. Background

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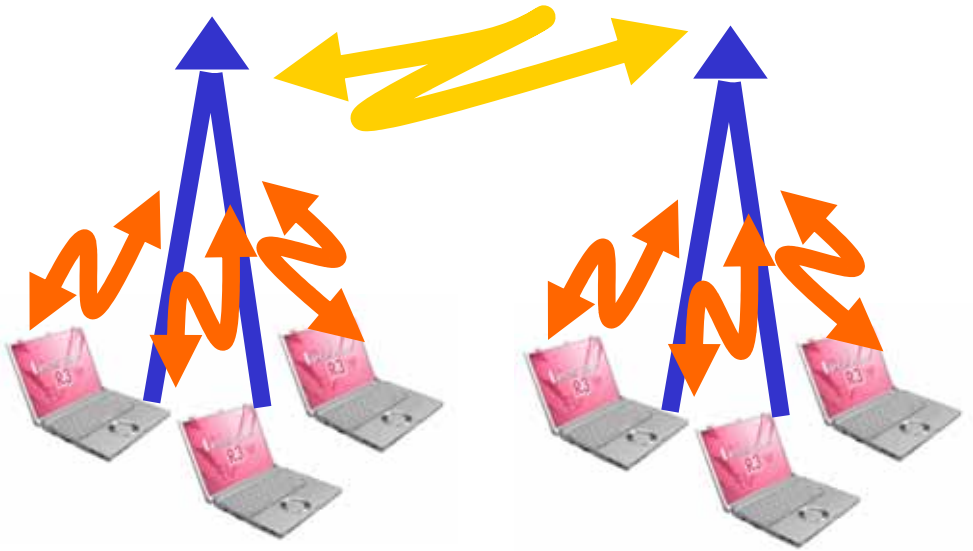
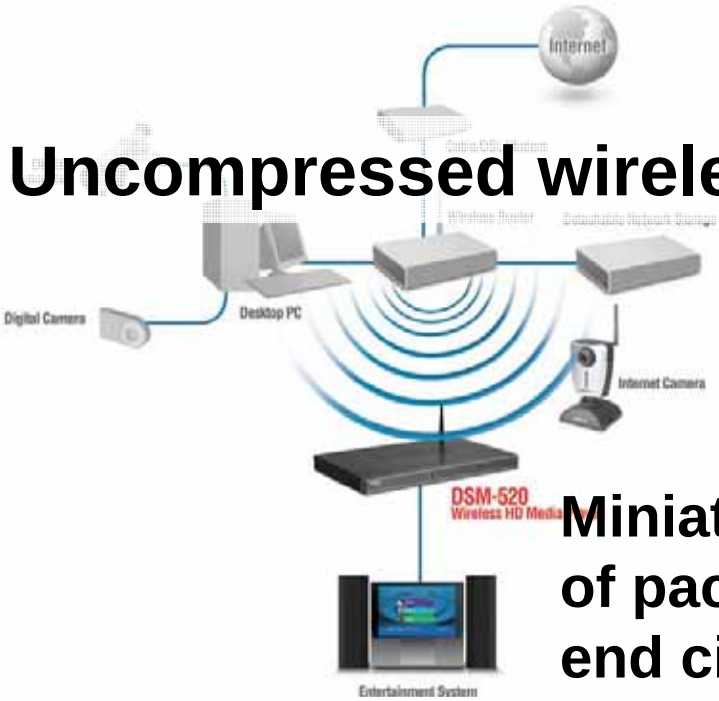
Road-to-vehicle and vehicle-to-vehicle communication

BS-to-BS communication



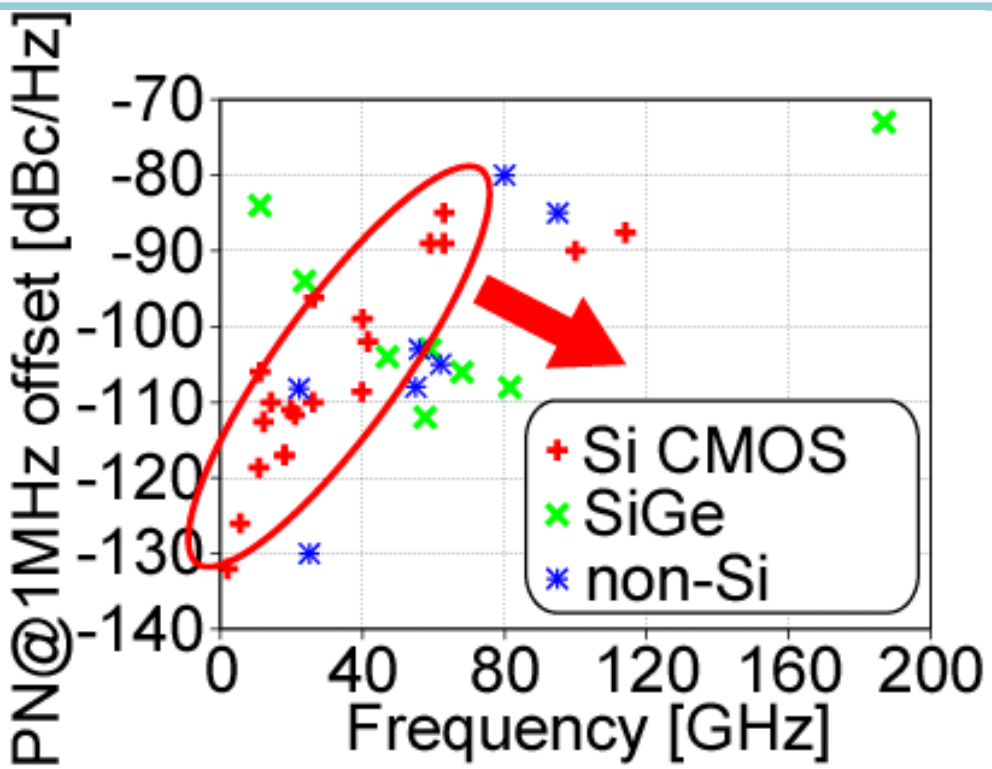
Uncompressed wireless HD transmission

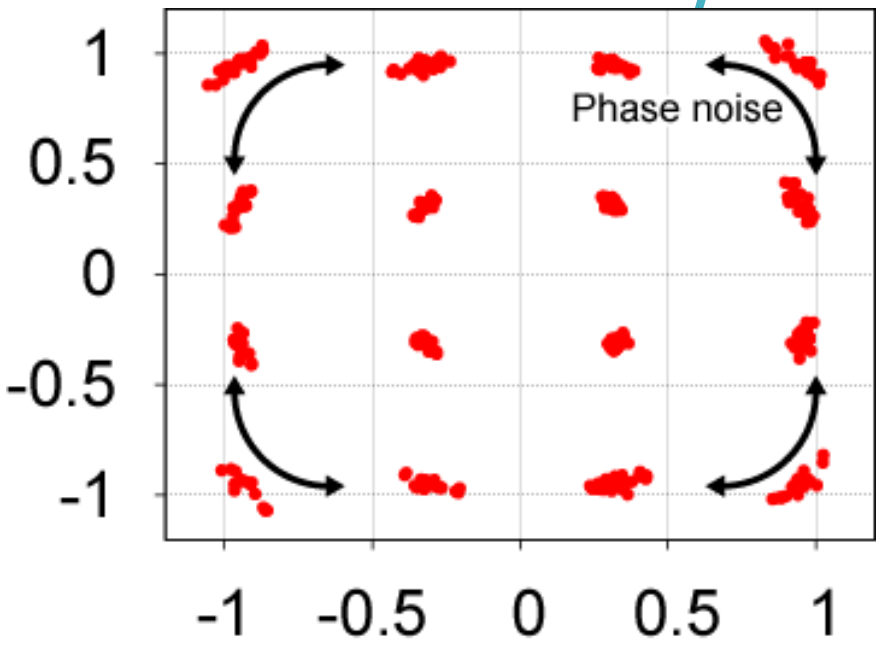


Miniaturization of Si CMOS process and improvement of packaging technology realize lower cost RF front-end circuits for millimeter wave application.

http://www.dlink.com/products/resource.asp?pid=438&rid=1635&sec=1

3. Motivation





Constellation is mismatched by phase noise degradation

VCOs using Si CMOS process have larger phase noise as compared with non-Si or SiGe.

4. Issues

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To realize low-phase-noise VCO at higher frequencies,

Topology:

NMOS-, PMOS-, or CMOS- cross-couple

NMOS-, PMOS-, or No- current source

LC or Transmission-line resonator

5. Purpose of this work

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- The PMOS cross-couple topology has lower phase-noise characteristic.
- It is a little difficult to use at more than 20GHz frequencies because gate capacitance degrades quality factor of resonator.
- As our conclusion, PMOS-cross-couple and PMOS current source topology is better for low-phase-noise VCO at around 10GHz.

6. Inductor or transmission line for resonator

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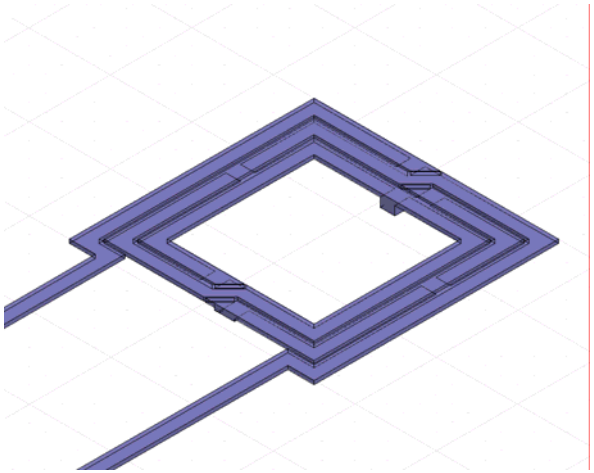
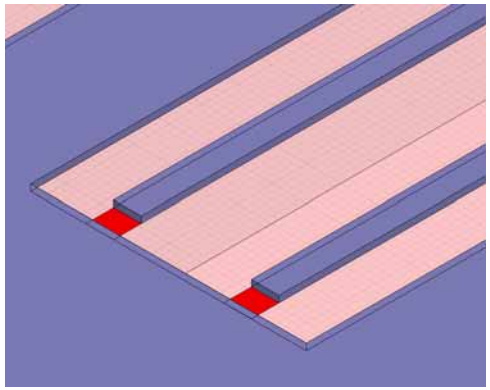
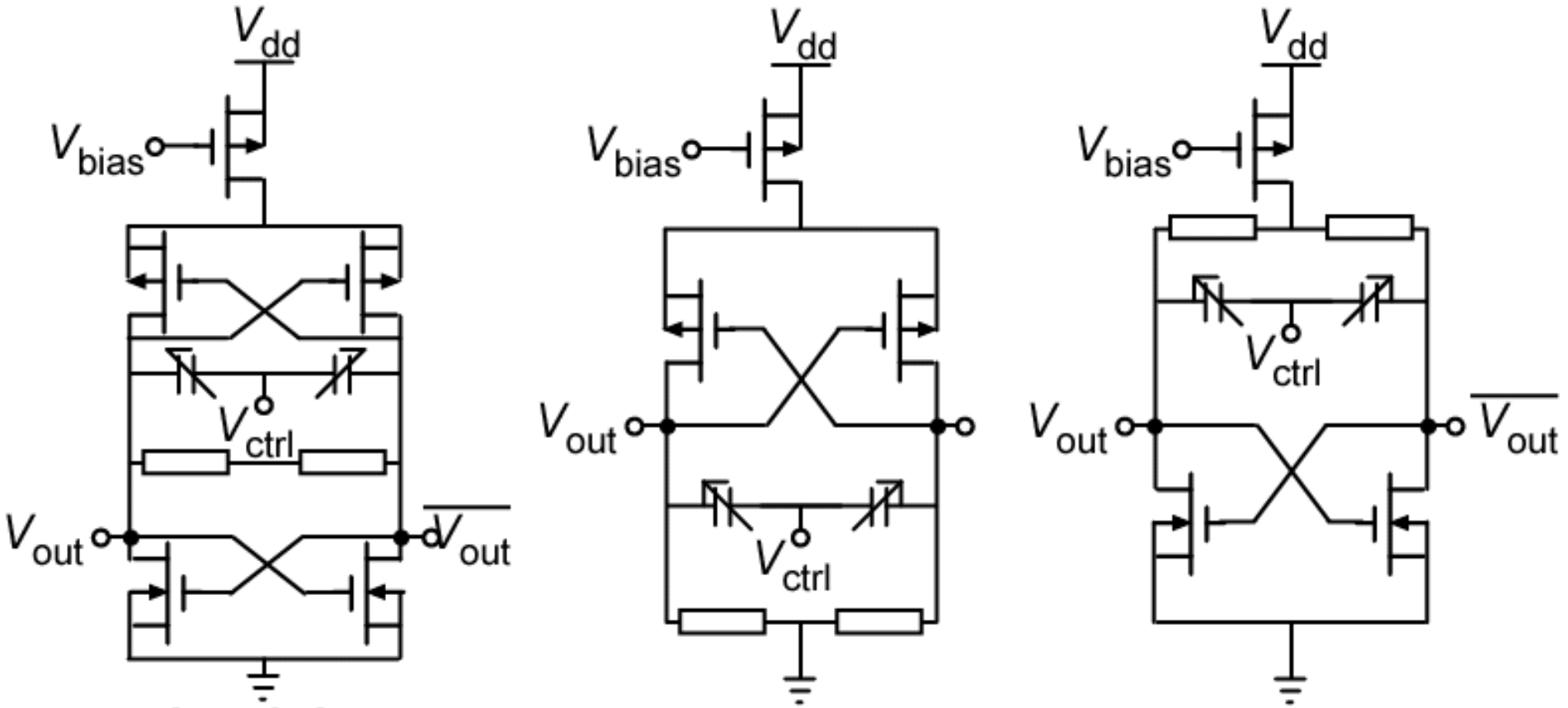
For high qualify factor resonator,





	Inductor	Transmission line
Inductance per unit length ∝1/(line loss)	large	small
Coupling with Si substrate ∝substrate loss	large	small
Distribution of parasitic capacitance	Lumped	Distributed
Frequency range for high quality factor	~20GHz	10GHz~

7. Simulation condition



- Length of Transmission Line used as resonator are 0.5mm~1mm
- Bias currents are optimized depending on W/L.
- Oscillation frequency is equalized by using MIM capacitors.

8. Trade-offs between VCO topologies

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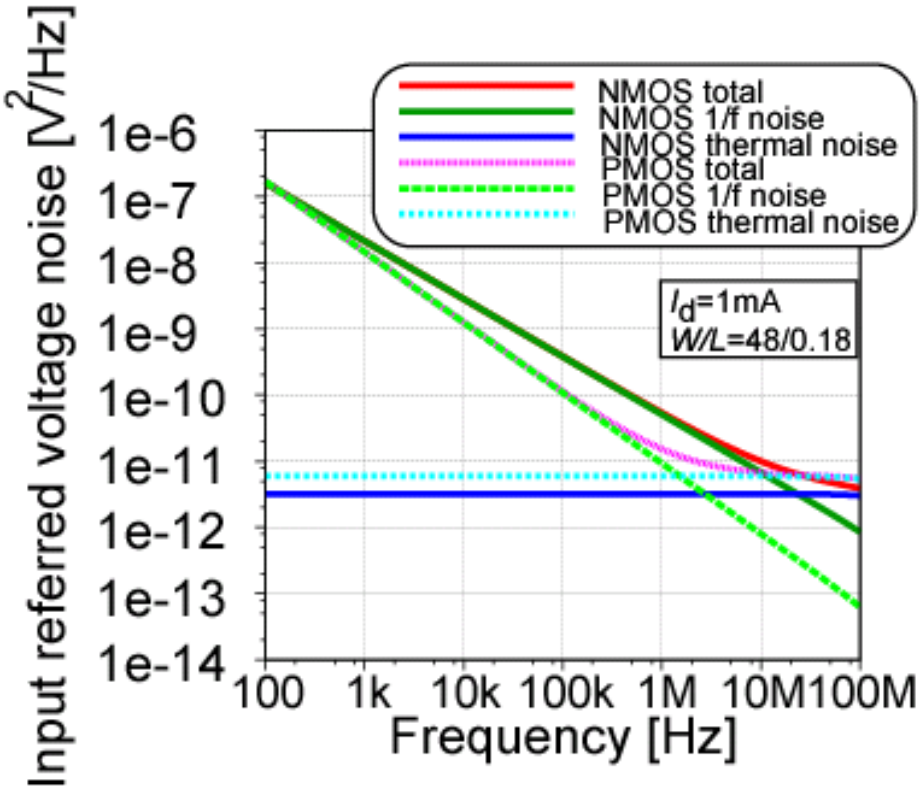
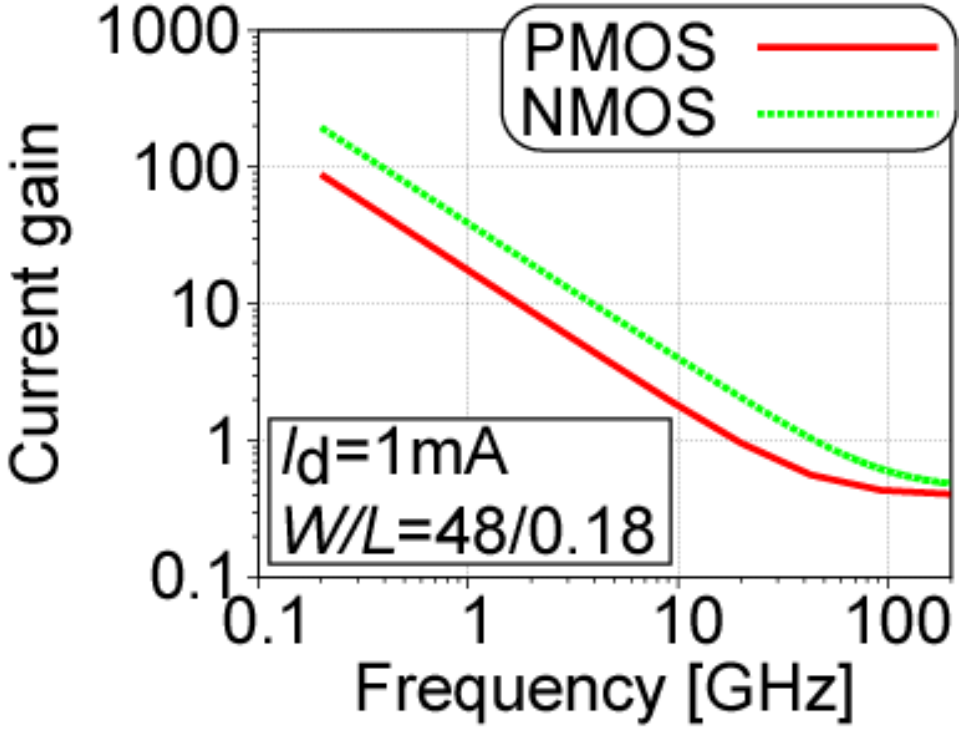
Cross-couple type	CMOS	PMOS	NMOS
Signal swing	$(V_{dd}-2V_{eff})$	$2x(V_{dd}-2V_{eff})$	$(V_{dd}-2V_{eff})$
1/*f* noise source (noise generation)	medium	low	high
1/*f* noise sensitivity (gain flatness)	low	high	high
Total noise	medium	medium	high
Total phase noise (S/N)	medium	low	high
g_m per unit tail current and unit C_{gs}	medium	low	high
Tail current @max. voltage swing	medium	high	low
Cut-off frequency	medium	low	high

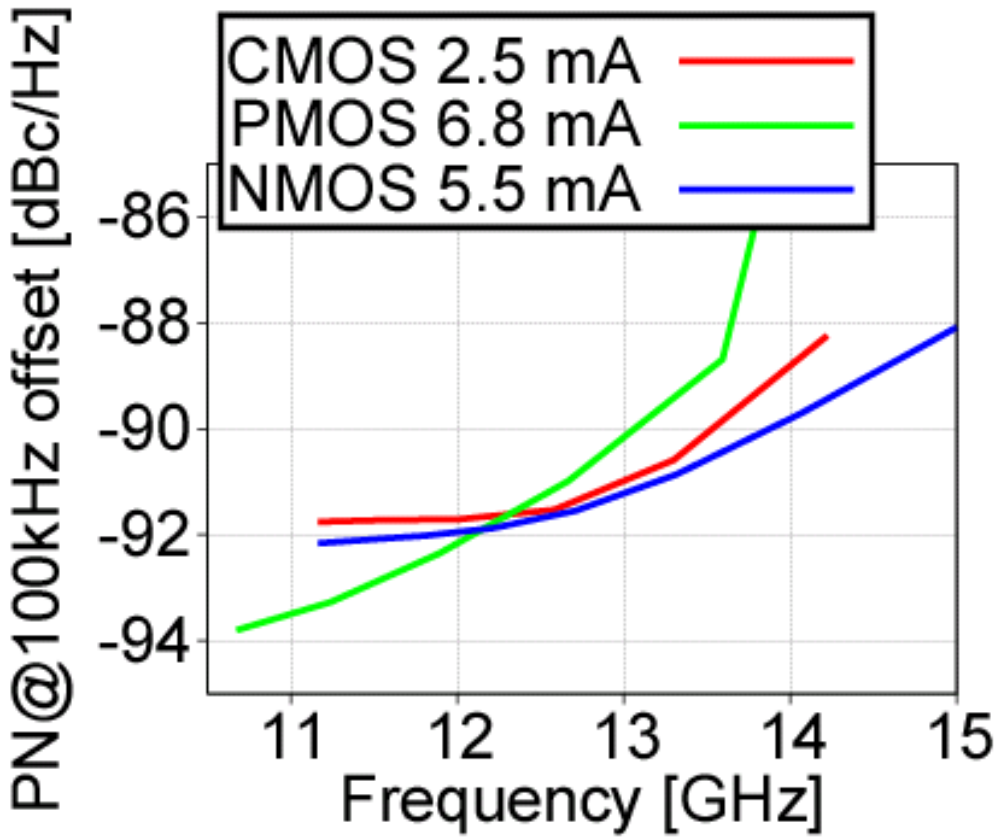
9. Trade-offs between PMOS and NMOS





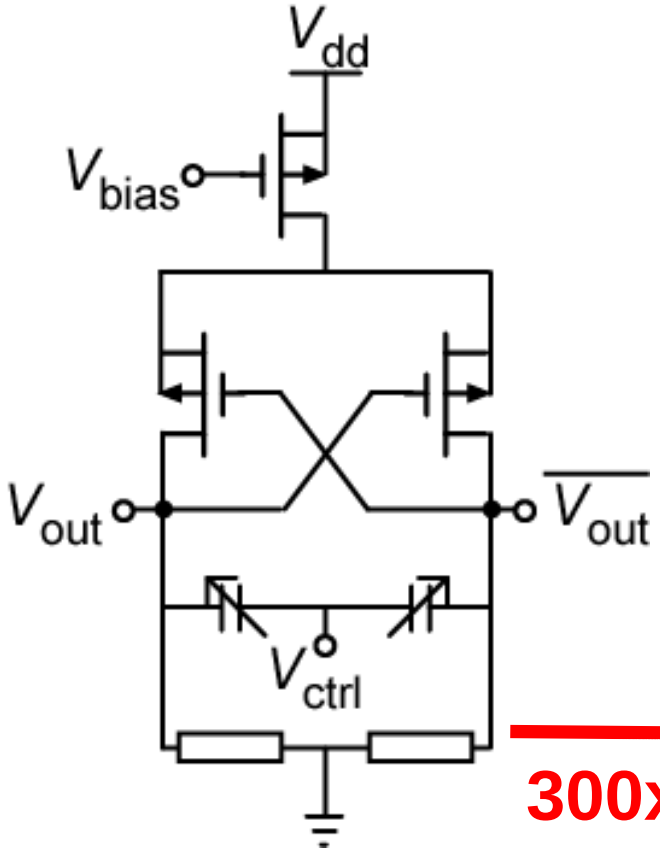
- At less than 10MHz, PMOS-type MOS has 5 times smaller 1/f noise than NMOS.
- PMOS has lower g_m and larger parasitic capacitances.

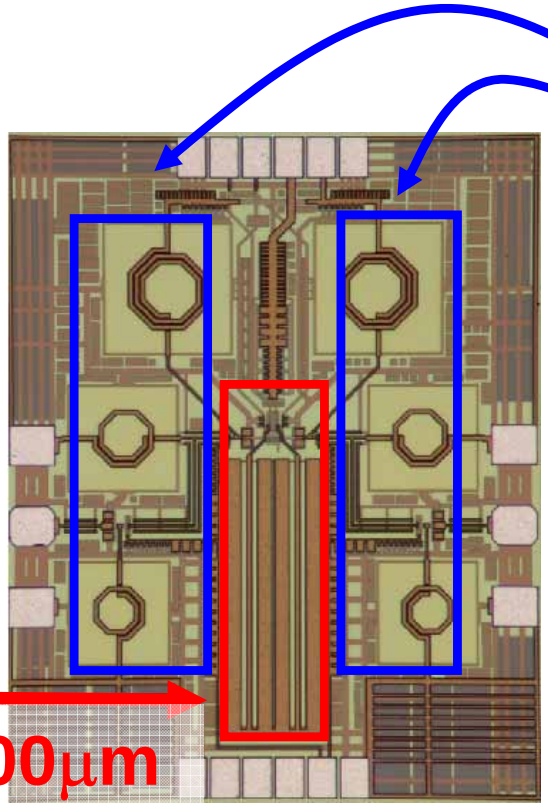
10. PMOS and NMOS cross-couple

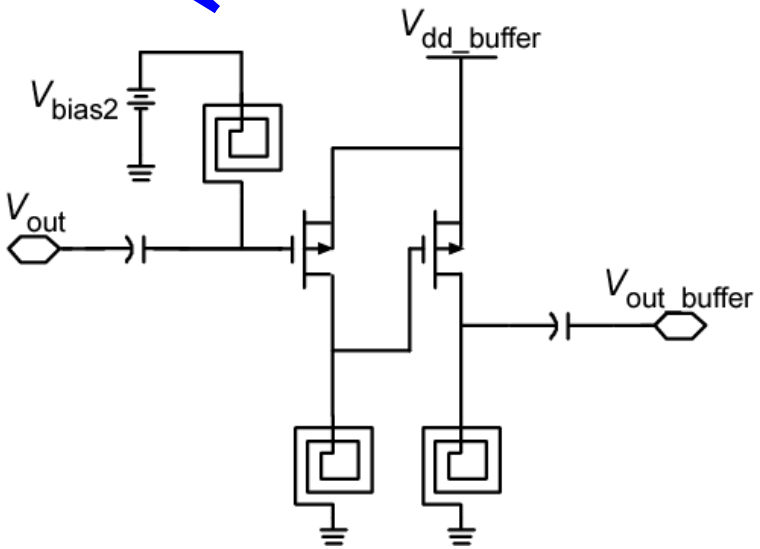


•Phase noise of PMOS cross-coupe is smaller at less than 12.5GHz

11. Microwave-band VCO







VCO Core

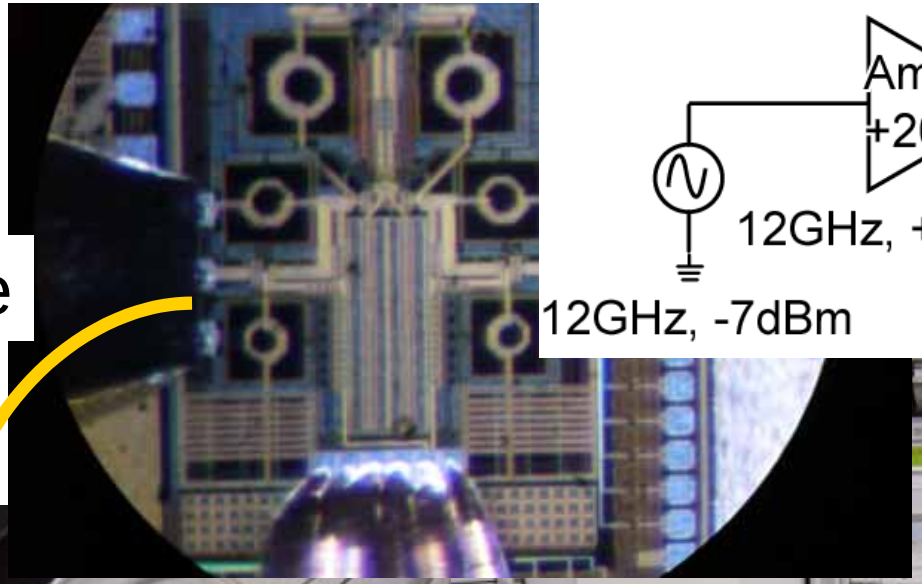
Chip photo

IO buffer

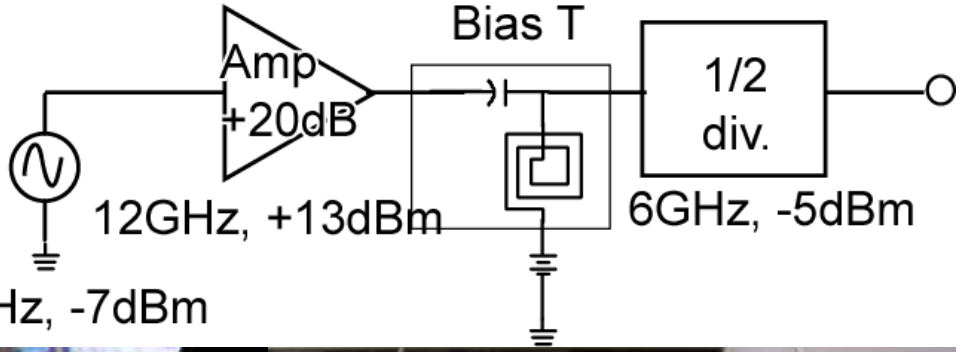
0.18μm Si CMOS process, PMOS type cross-couple is fabricated.
Oscillation frequency: 12GHz, phase noise @1MHz offset: -113dBc/Hz
IO buffer: inductive load, 2nd stage common source for high frequency operation

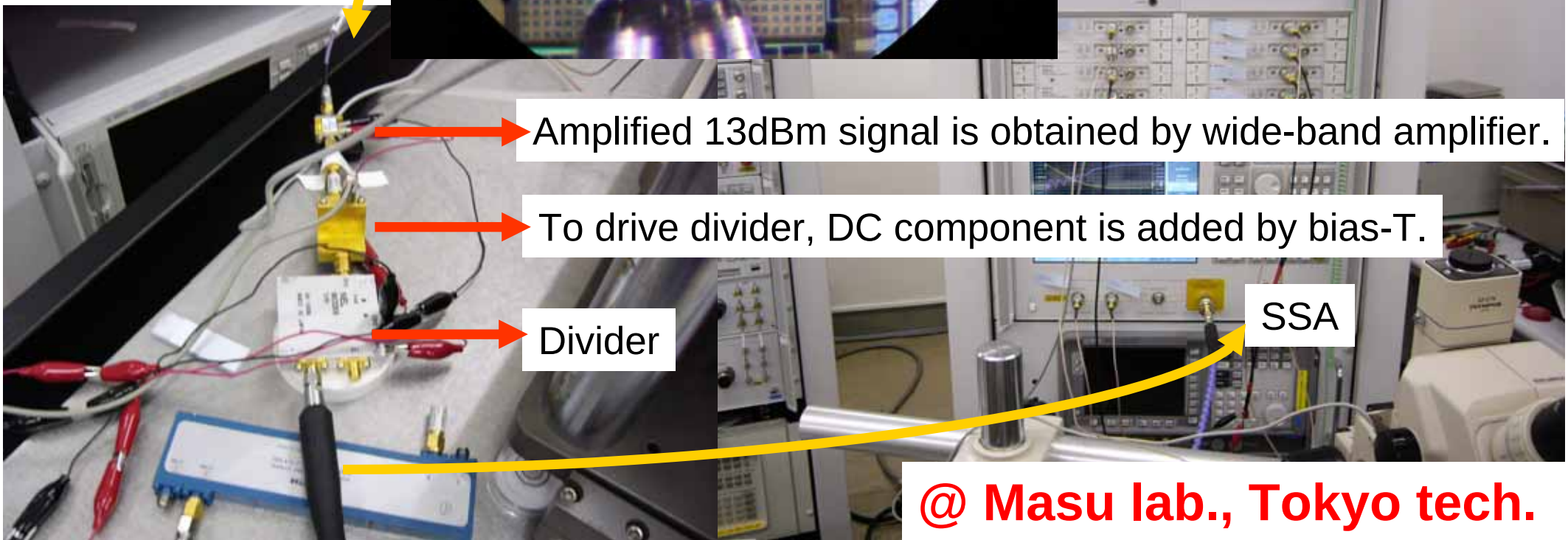
12. Measurement

- Wide-band amplifier is used to compensate low VCO output power -7dBm.
- Signal Source Analyzer can measure lower than 7GHz, signal divided by 2 is measured.



On-wafer probe





Amplified 13dBm signal is obtained by wide-band amplifier.

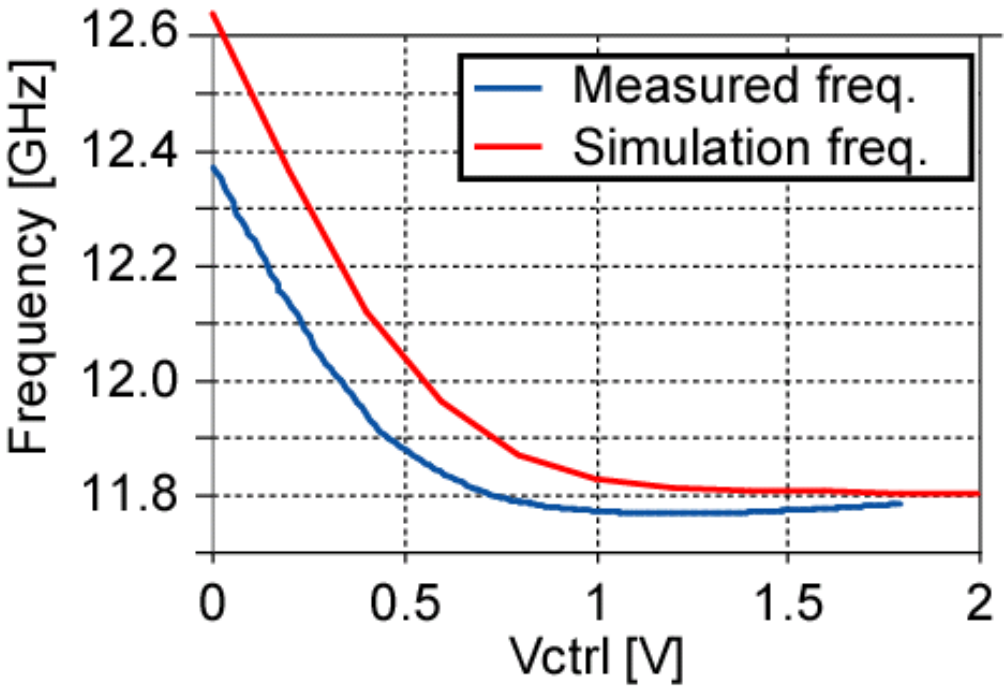
To drive divider, DC component is added by bias-T.

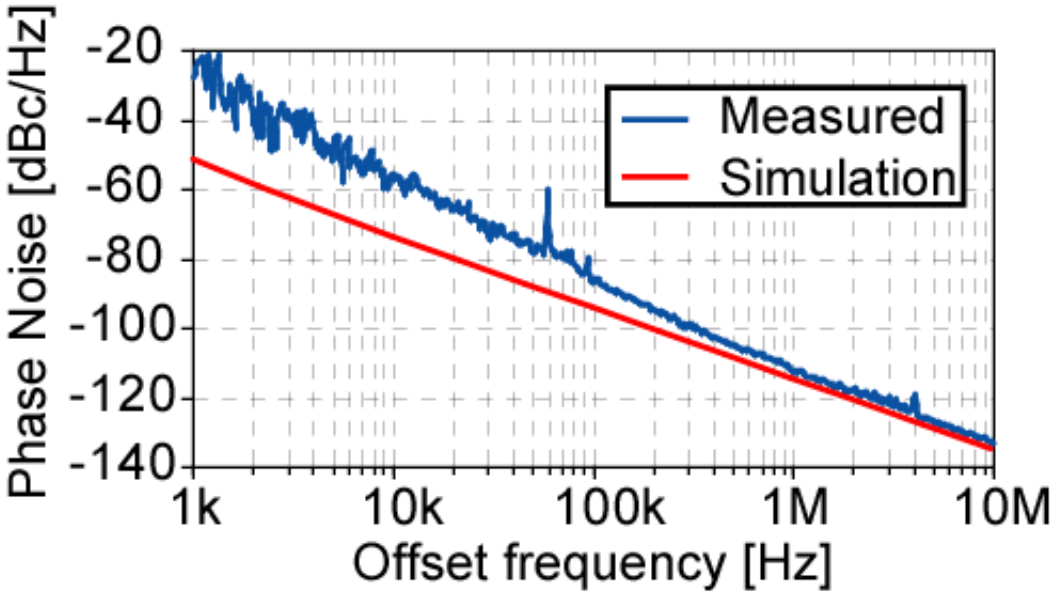
Divider

SSA

@ Masu lab., Tokyo tech.

13. Oscillation frequency and phase noise





	Simulation result	Measured result
Oscillation freq.	12.6GHz	12.4GHz
Phase noise@1MHz offset	-113.1dBc/Hz	-112.6dBc/Hz

- Simulation results and measured results are almost same.

14. Conclusion

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- **I explained trade-offs between VCO cross-couple topologies at more than 10GHz.**
- PMOS transistors have lower 1/*f* noise while they have larger gate capacitances.
- **In our comparison using circuit simulations, PMOS cross-coupled VCO has lower phase noise characteristic at less than 12.5GHz.**
- In experimental result, a phase noise is −112.6 dBc/Hz@1MHz offset, and Figure of Merit is −184.9 dBc/Hz.
- The VCO is fabricated by a 180 nm Si CMOS process.
- In this presentation, I showed the capability of PMOS cross-couple topology at more than 10GHz.

15. Acknowledgement

- This work was partially supported by JSPS. KAKENHI, MIC. SCOPE, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.
- Special thanks to Masu lab., Tokyo tech. for offering RF measurement environment.

16. FoM

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VCO PERFORMANCE COMPARISON.

Reference	Topology	Frequency	Output Power [dBm]	Phase Noise [dBc/Hz]	f_offset [MHz]	PowerConsumption [mW]	Technology	FOM
[1]	Injection locked	39.2–40.3	-8	-108.7	1	6.0	0.18 μm Si CMOS	-192.9
[2]	LCVCO	10.18–11.37		-118.7	1	11.8	0.18 μm Si CMOS	-188.6
This Work	TLVCO	11.8–12.4	-7.5	-112.6	1	8.6	0.18 μm Si CMOS	-184.9
[2]	LCVCO	19.84–22.01		-111.7	1	40.3	0.18 μm Si CMOS	-182.0
[3]	NMOS LCVCO	19.9		-111.0	1	32.0	0.18 μm Si CMOS	-181.9
[4]	Distributed Oscillator	40		-99.0	1	27.0	0.18 μm CMOS	-176.7
[2]	LCVCO	39.33–43.67		-102.0	1	115.9	0.18 μm Si CMOS	-173.7
[5]	balanced VCO	21.9–22.33	-0.3	-108.2	1	140.0	InGaP/GaAs HBT	-173.6
[6]	Colpitts	23–24.4	–	-94.0	1	22.0	BiCMOS	-168.1
[7]	Varactorless VCO	23.2–29.4		-96.2	3	36.5	0.13 μm Si CMOS	-159.4
[8]	Distributed Oscillator	11.03–11.19	–	-84.0	1	9.0	0.35 μm Si Bipolar	-155.4

$$FoM = -10\log\{L\Delta\omega\} + 20\log\frac{\omega_0}{\Delta\omega} + 10\log\frac{Power}{1\mathrm{mW}}$$