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Analog IC Technologies for Future Wireless Systems

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SUMMARY The analog IC technology, might sound old-fashioned, is still important for the future wireless systems such as 4G cellular phone systems, broadband wireless networkings, and wireless sensor networkings. The analog features and issues of the scaled CMOS transistor, the basic issue and the technology trend for the ADC as an important building block of wires systems, and the feature of the digital RF architecture proposed recently are reviewed and discussed. Higher speed and lower power consumption are expected for low SNR systems along with the further technology scaling. However, the high SNR system is not realized easily due to a decrease of signal voltage. One of the important technology trends is the digitalization of RF signal to realize the system flexibility, robustness, area shrinking, and TAT shortening.

key words: *analog circuit, integrated circuit, wireless system, CMOS, analog to digital converter, radio frequency*

1. Introduction

Wireless technologies must play important role for not only conventional broadcasting tuners, cellular phones, and wireless LANs but also for ubiquitous networks such as censor networks. A basic technology trend for the future wireless systems can be listed as follows;

1) Higher data transmission
2) Address multi-standards and multi-bands
3) Higher integration and lower power consumption.

SoC technology that uses shorter design rule such as 65 nm node or 45 nm node will be used in wireless systems. Because of only technology scaling enables high speed processing, large system integration, and low power consumption, simultaneously. Analog circuits should be integrated on the SoC [1]. An impact of analog technology on the performance of wireless system is still large. However the future perspective of the analog technology is not rosy compared with the digital technology, because it does not follow the great scaling rule such as the digital scaling rule. This paper reviews and discusses a trend and issues of analog technologies for the future wires systems.

2. Analog Performance of Scaled MOS Transistor

The cutoff frequency of the future scaled MOS transistor will continue to increase along with the technology scaling, as shown in Fig. 1 [2]. The peak cutoff frequency of MOS

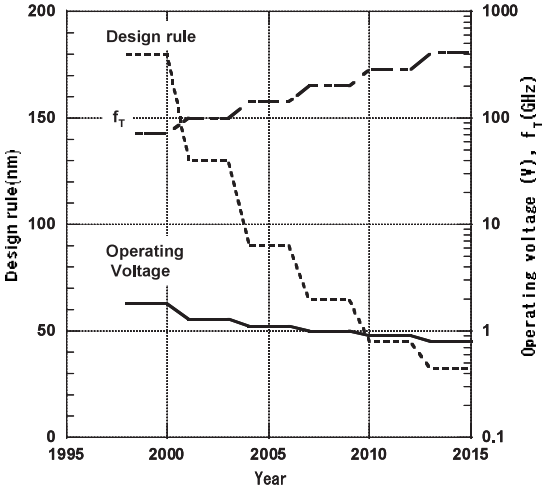

Fig. 1 Trend of design rule, f_T and operating voltage in CMOS technology.

transistor f_{Tmax} is approximately given by

$$f_{Tmax} \approx \frac{v_{sat}}{2\pi L}, \tag{1}$$

where v_{sat} is a saturation career velocity and L is the channel length of MOS transistor. Cutoff frequency is inversely proportional to the channel length and will reach about 200 GHz at 65 nm node. On the contrary, a major career frequency of the future wires systems will stay 7 GHz at most, at that time the noise figure of LNA will be small enough. f_{Tmax} can not be expressed in the simply expression; however it also will increase moderately due to an increase of cutoff frequency and a decrease of the gate resistance. Therefore, frequency characteristics for RF circuit will be improved continuously.

However, the most serious present and future issue must be the operating voltage lowering. Every device has a fundamental tradeoff between cutoff frequency and maximum operating voltage V_{max}, as below.

$$f_{Tmax} \times V_{max} \approx const. \tag{2}$$

The constant is basically determined by its band gap voltage that is about 200 VGHz for silicon devices. Figure 1 shows the maximum operating voltage vs. technology nodes. According to recent ITRS technology load map, the maximum operating voltage around 1 V will be expanded to 45 nm node in future scaled devices [3]. This value becomes higher compared with that of the past ITRS technology load

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map. And that sounds tough to realize high performance analog circuits; however it is not impossible to attain the high performances by some analog circuits.

The realization of the high SNR analog circuit however is severe challenge. The SNR of a differential sample and hold circuit, which is often used in many analog circuits, can be expressed as,

$$SNR = \frac{CV_{pp}^2}{4kT}, \tag{3}$$

where C is the sampling capacitor, V_{pp} is the differential peak voltage of sinusoidal signal, k is the Boltzmann's constant, and T is the absolute temperature. Because of SNR decreases with a decrease of signal amplitude, the larger capacitances are needed to keep the same SNR at the low operating voltage; however this results in increase of the power consumption or decrease of the signal bandwidth. Therefore, the increase of signal bandwidth with moderate SNR is promising; however the increase of SNR becomes quite tough. This issue is essentially common in almost all the analog circuits, such as ADCs, filters, and VCOs.

The head room issue where a lot of transistors cannot be piled for a low operation voltage analog circuit becomes more serious. Also CMOS switch will make serious problem. CMOS switch has the source node which is connected to the input terminal and the on-resistance takes largest value when the signal voltage is about half operating voltage. The conventional threshold voltage of MOS transistor is about 0.2 V but it increases up to about 0.4 V due to the back gate effect, the temperature decrease, and the process variation. Only 0.1 V can be applied as an effective gate voltage when the operating voltage is 1 V. A switch will not be able to achieve sufficiently small on-resistance.

Other issues are the reduction of gain of amplifier caused by the reduction of a drain resistance and an increase of a noise coefficient. The transistor gain for the 90nm MOS transistor is about 10 at most, then the design of the high gain amplifier with scaled CMOS process is quite tough compared with that with conventional 0.35 μm CMOS process. The increase of V_T mismatch might be concerned, however the mismatch coefficient is not expected to increase so much and mismatch can be compensated by circuit technology.

3. ADC

An ADC will keep the important position for future digital wireless systems even though the other analog circuit blocks will be removed. The wireless technology trend shows the software defined radio architecture that high performance ADC should be located near by the antenna becomes mainstream to realize performance flexibility for addressing multi-standard and multi-band functions. Almost all the filter functions such as the channel selection should be done in the digital domain. Thus the high performance, yet low power and low cost ADC is crucial for the future wires systems.

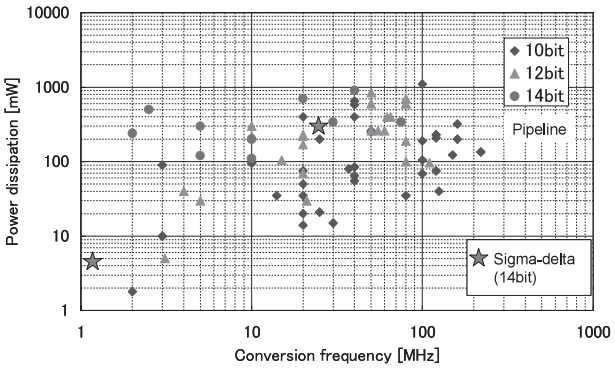

Fig. 2 Power dissipation and conversion frequency of 10 bit, 12 bit, and 14 bit ADCs.

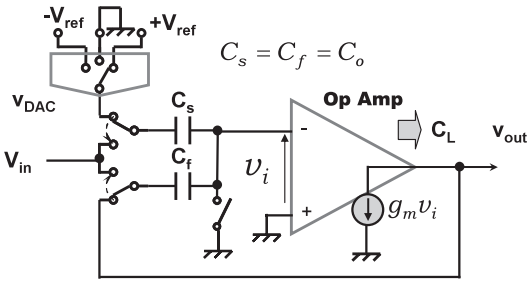

Fig. 3 A unit amplifier of the pipeline ADC.

Several-hundred MHz conversion speed and 10 bit to 14 bit resolution must be needed for the future cellular phone systems and wires LAN systems. Therefore pipeline ADC architecture, that uses comparator and accurate switched capacitor amplifier to convert the input analog signal to the digital values with a few bits per clock in a pipeline fashion must be the strong candidate.

Figure 2 shows the conversion frequency and the power consumption of published 10 bit, 12 bit, and 14 bit pipeline ADCs and some sigma delta ADCs. A higher resolution ADC consumes much power; however its conversion frequency is low. The maximum conversion frequency is about 200 MHz and the normalized power consumption by conversion frequency is about 0.3 mW/MHz for the 10 bit pipeline ADC. Since the ADC is the most important analog core block for the future wireless systems, this paper will discuss the fundamental performance limitation and estimation with respect to the technology scaling.

3.1 Signal Capacitance

A pipeline ADC consists of cascade connection of a unit amplifier as shown in Fig. 3 and it's the most important design point is to determine the signal capacitance, C_s and C_f [4].

Closed loop gain bandwidth (GBW) and the maximum conversion frequency of pipeline ADC can be described as;

$$GBW_{close} = \frac{g_m}{2\pi C_L} \cdot \beta, \tag{4}$$

$$f_c \approx \frac{3 \times GBW_{close}}{N}, \tag{5}$$

where g_m is the transconductance of input transistor, C_L is the load capacitance, beta is the feedback factor, N is the resolution. Since g_m has the following relationship with a drain current I_{ds} and an effective gate voltage V_{eff},

$$g_m \approx \frac{2I_{ds}}{V_{eff}}. \tag{6}$$

Therefore, the conversion frequency normalized by the operating current I_{ds} is given by

$$\frac{f_c}{I_{ds}} \approx \frac{3}{\pi V_{eff}} \cdot \frac{1}{C_L} \cdot \frac{\beta}{N}. \tag{7}$$

This result shows that the reduction of capacitance is crucial to increase this metrics, since the effective voltage V_{eff} can not be reduced to less than 0.1 V due to the device physics.

The capacitance is determined by the capacitance mismatch and the thermal noise.

The needed capacitance mismatch for the N bit resolution with the error of 1/4 LSB in a 1.5 bit pipeline ADC can be expressed as

$$\frac{\Delta C}{C}(3\sigma) < \frac{1}{2^N}. \tag{8}$$

The capacitor mismatch is inversely proportional to the square root of capacitance and can be given by

$$\frac{\Delta C}{C}(3\sigma) = \frac{6 \times 10^{-4}}{\sqrt{C(\mathrm{pF})}}, \tag{9}$$

when using the conventional mismatch coefficient. Therefore, the needed capacitance is

$$C(\mathrm{pF}) \geq 3.6 \times 10^{-7} 2^{2N}. \tag{10}$$

The needed capacitance increases with an increase of resolution rapidly as shown in Fig. 4, for example only 0.4 pF is needed for the 10 bit resolution. However about 100 pF is needed for the 14 bit resolution. This large capacitance needed for the high resolution ADC decreases the conversion rate and increases power consumption so much. To address this issue, the digital error compensation technique has been developed [5]. Figure 5 shows conversion characteristics with or without the digital error correction. The large linearity errors occur at the comparator's change points in the first stage. These errors are once measured and obtained as error values V_{e1} and V_{e2} and are stored in registers, next the conversion values are compensated by the addition or the subtraction of these values digitally depended on the comparator's states in the first stage, as shown in Fig. 5. Linearity errors in the other stages can be compensated in similar way from the lower bits. Then the recent ADC can reduce the capacitance by using the digital error correction compared with the conventional one.

Therefore the capacitance value is determined by noise,

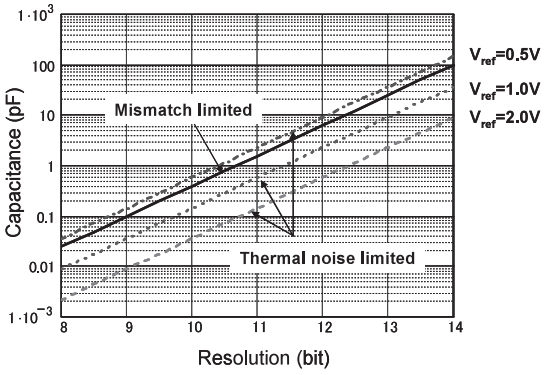

Fig. 4 The needed capacitance for several resolutions.

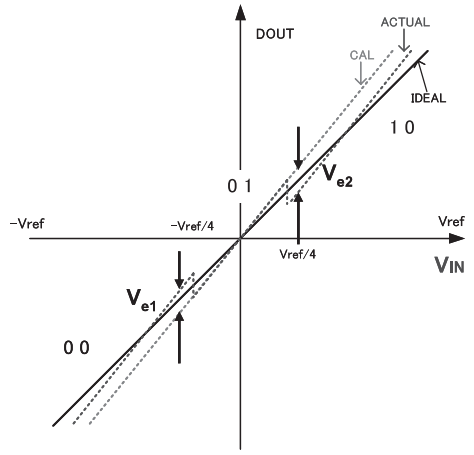

Fig. 5 Conversion characteristics with and without digital error correction.

finally.

The input referred noise power can be estimated as

$$v_n^2 \approx 4\frac{kT}{C_o}, \tag{11}$$

where C_o is the unit capacitance in the first stage. The needed capacitance of which noise power is half of quantization noise power can be derived as

$$C(\mathrm{pF}) \geq 1.32 \times 10^{-7} \left(\frac{2^N}{V_{ref}(\mathrm{V})} \right)^2, \tag{12}$$

where V_{ref} is the single side reference voltage. Figure 4 also shows the needed capacitance derived from Eq. (12) as a function of resolution. The capacitance increases by four times for the one bit higher resolution; however it can be decreased by using the larger reference voltage. In other words, the low voltage operation results in increase of capacitance. The serious issue due to further low voltage operation comes out.

3.2 Design Rule and ADC Performance

Will technology scaling in analog increase performance or not? This question is essentially important for the future

wireless systems. Therefore we have estimated the influence of CMOS design rule on a pipeline ADC performance [6]. Rough estimations for the conversion frequency and the power consumption are given by Eq. (5) and Eq. (7). At this point, the effect that load capacitor C_L and the feedback factor beta are influenced by the parasitic capacitances of MOS transistor is considered.

A unit conversion circuit can be modeled using the parasitic input capacitance C_{pi}, the parasitic output capacitance C_{po}, and the trans-conductance g_m, as shown in Fig. 6. The closed-loop bandwidth can be derived as,

$$GBW\_close = \frac{g_m}{2\pi C_o} \frac{1}{\left(2 + \frac{C_{pi}}{C_o}\right)\left(1 + \frac{C_{po}}{C_o}\right) + \left(1 + \frac{C_{pi}}{C_o}\right)}, \tag{13}$$

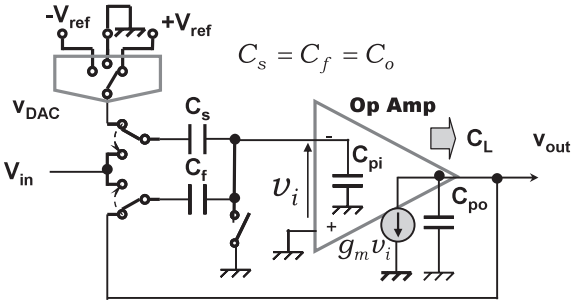

Fig. 6 A unit amplifier of pipeline ADC with parasitic capacitors.

where C_o stands for the signal capacitances C_s and C_f.

The parasitic input and output capacitances, C_{pi} and C_{po} depend on the used design rule and proportional to the operating current when V_{eff} keeps same value. Thus, $C_{pi} = \alpha_{pi} \cdot I_{ds}$ and $C_{po} = \alpha_{po} \cdot I_{ds}$ and Eq. (13) can be modified as,

$$GBW\_close = \frac{I_{ds}}{2\pi C_o V_{eff}} \cdot \frac{1}{\left(2 + \frac{\alpha_{pi} I_{ds}}{C_o}\right)\left(1 + \frac{\alpha_{po} I_{ds}}{C_o}\right) + \left(1 + \frac{\alpha_{pi} I_{ds}}{C_o}\right)}. \tag{14}$$

The coefficients of the parasitic input and output capacitance, C_{pi} and C_{po} are decreasing with a decrease of design rule. The coefficients become half along with one technology generation advance. Figure 7 shows estimated maximum conversion frequency for 8 to 14 bit ADCs as a function of the sink current of the input MOS transistor in the first stage operational amplifier for the several design rules such as 0.35 μm, 0.25 μm, 0.18 μm, 0.13 μm, and 90 nm.

The maximum differential signal voltage is assumed two times larger voltage that 0.7 V is subtracted from the maximum operating voltage for each design rule. C_o is given by Eq. (12) and V_{eff} is assumed to be 0.175 V.

The characteristics curve is convex and takes the highest value at the certain sink current. In the region of the current being less than this value, the conversion frequency increases with an increase of the sink current. There are two reasons for this. At first, the g_m is proportional to the sink current, and the parasitic capacitances are smaller than that

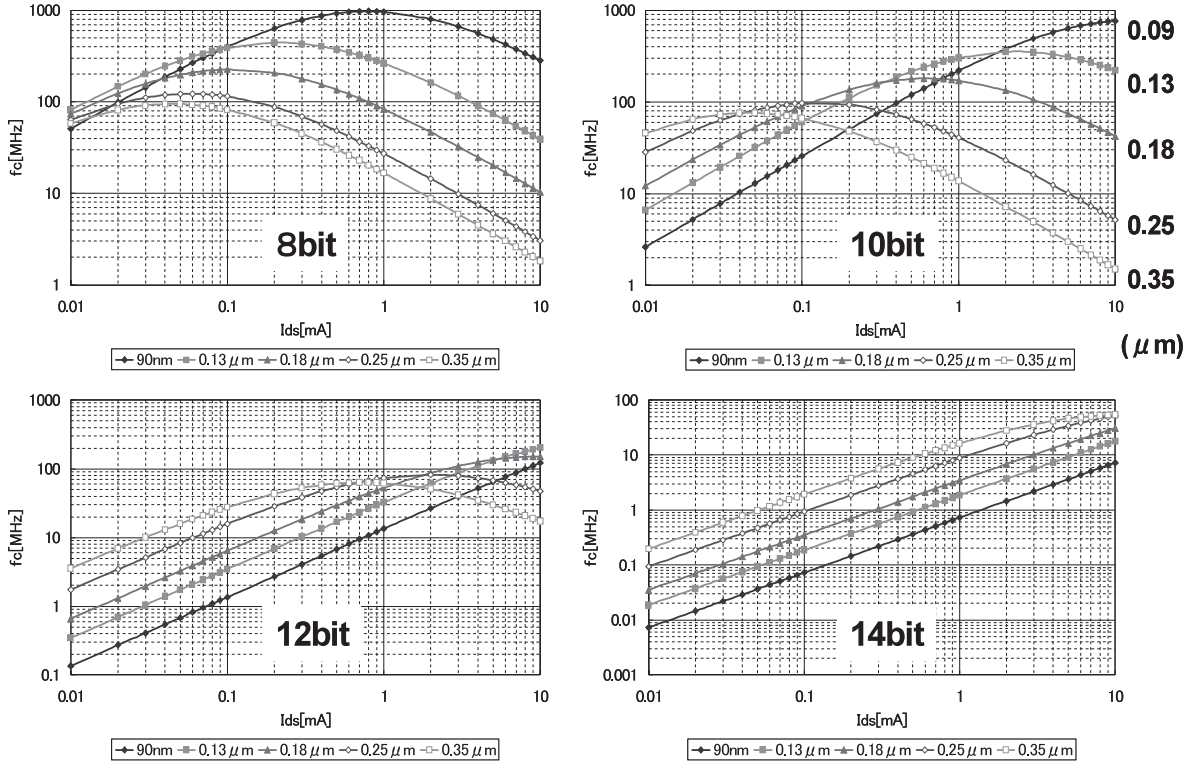

Fig. 7 Conversion frequency vs. sink current of the input stage for several resolutions and design rules.

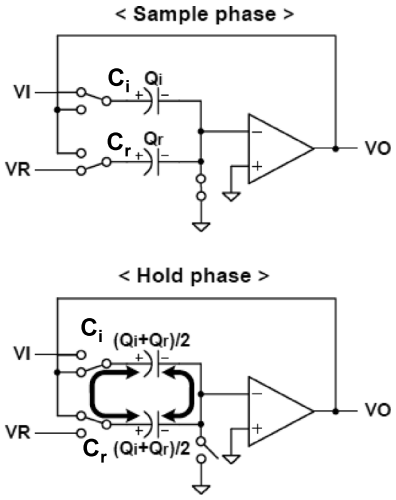

Fig. 8 A circuit to reduce beta.

of the signal capacitance. At around the peak, at least one of the parasitic capacitances becomes equal to the signal capacitance. In the region of the current being larger than that value, both parasitic capacitances become larger than that of the signal capacitance and the conversion frequency will decrease with increase of the sink current.

Estimated performance curves exhibit interesting results in terms of relation ship between the performances and the design rules. For the 8 bit resolution, the case of 0.13 μm CMOS process is the fastest in low current operation, but the case of 90 nm CMOS process attains the highest conversion frequency. For the 10 bit resolution, the case of 0.35 μm CMOS process is faster than the other processes in the ultra low power region, and the finer design rule gets better for the high frequency conversion along with an increase of the sink current. The case of 0.35 μm CMOS process takes the best position for 12 bit or 14 bit resolutions, in terms of the high speed conversion and the low power consumption. Because of this, for the lower resolution, the signal capacitance is smaller and the use of the fine design rule transistors is effective to reduce the parasitic capacitances. However to achieve the higher resolution, the signal capacitance when using the fine design rule transistors increases to keep high SNR with small signal voltage. At this moment, a reduction of parasitic capacitance is not effective any more.

This result shows that the technology scaling is not always effective to the progress of analog performance. The technology scaling is not effective to increase SNR or resolution but effective to increase speed with low SNR.

One way to increase the conversion frequency is increase of the feedback factor beta. Figure 8 shows the conversion circuit that can increase the feedback factor [7]. The capacitor C_i samples the signal and the capacitor C_r stores needed reference voltage in a sampling mode. The C_i and C_r are connected in parallel between the input and the output terminals of the operational amplifier. The charge redistribution makes following voltage,

$$V_{out} = \frac{1}{2} v_{in} - V_R. \tag{15}$$

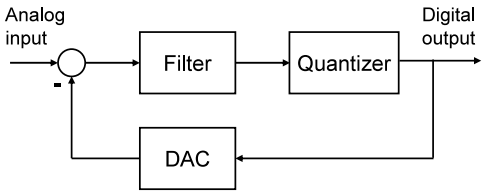

Fig. 9 Sigma-delta ADC.

The feedback factor beta is so ideally unity, which is two times higher than conventional one, which increases the closed loop bandwidth. As a result, high speed conversion or low power consumption is expected. However this architecture requires four times larger input voltage due to the low voltage gain and it causes some problems for the low voltage operation.

3.3 Delta-Sigma ADC

A delta-sigma modulation method can realize higher SNR with a low resolution quantizer by using a filter and the negative feedback loop, as shown in Fig. 9. The noise spectrum of the quantizer is modulated and the lower frequency component is suppressed so that the high SNR can be realized by the operation of the digital low pass filter when using higher sampling frequency. The theoretical SNR is derived below,

$$SNR = 10 \log \left\{ \frac{3}{2} \frac{2L+1}{\pi^{2L}} G^2 M^{2L+1} (2^N - 1)^2 \right\}, \tag{16}$$

where N is the resolution of quantizer, L is the order of filter, G is the gain from input to quantizer, and M is the over sampling ratio.

High SNR might be expected if increasing system parameters, however it is not so easy to realize. This feedback system becomes unstable when using a higher order of filter. For that reason, a feedback or a feed forward compensation is needed. These compensations result in deterioration of SNR due to the decrease of filter performance. An increase of resolution is effective, however the high precision DAC is needed at the same time. The linearity error of the DAC is not suppressed by the delta-sigma modulation method and affects to SNR directly. Thus the high precision DAC is needed for the high SNR ADC. Also the noise of the first stage operational amplifier cannot be suppressed. The total noise and the contribution of each stage in fourth order system is given by,

$$P_{N\_tot} = P_{N1} \frac{1}{M} + P_{N2} \frac{\pi^2}{3A_2^2 M^3} + P_{N3} \frac{\pi^4}{5A_3^2 M^5} + P_{N4} \frac{\pi^6}{7A_4^2 M^7}, \tag{17}$$

where P_{Ni} and A_i are the noise power and the gain of i'th stage, respectively. The noise of the first stage is suppressed merely with the over sampling ratio M. Thus The increase of the over sampling ratio M is sound way to increase SNR, however this means an useful signal bandwidth is limited.

Since SNR of 80 dB needs the over sampling ratio of 16 or 32, for the bandwidth which is less than 10 MHz higher SNR can be realized with sigma-delta method [8], however it seems very tough for higher bandwidth [9]. Figure 2 shows high SNR with low power consumption has been attained with delta-sigma ADC for the signal frequency being less than several MHz, however this technology looses the advantage for the 10 MHz signal.

Although the delta-sigma method has several issues, it is still attractive for the wireless systems because of flexibility. High SNR yet low signal bandwidth and high bandwidth yet low SNR are realized simultaneously by changing circuit parameters.

The band pass filter and the complex filter can be used as well as the conventional low pass filter to apply the low IF wireless architecture [10].

As has been mentioned, further technology scaling will increase the conversion frequency of the relatively low resolution pipeline ADC such as 8 bit or 10 bit, however it would be quite tough to realize the high resolution ADC such as 12bit or 14bit. A delta-sigma ADC can realize the high SNR ADC such as 14 bit for relatively narrow bandwidth which is less than 10 MHz, however it would be quite tough to increase signal bandwidth on keeping high SNR.

4. Digital RF Architecture

Recent the most important circuit and system idea for the future wireless systems must be the "digital RF architecture" proposed by TI [11]. The essence of this idea is to apply the discrete time processing technology to the radio frequency. Namely the circuits are formed with small and robust circuits, such as digital circuits, switches, and capacitors so as to kick out the conventional continuous time analog circuits and the inductors. Because these are delicate, non-scalable, non flexible, and area consume. The backgrounds of this idea can be listed below;

1) Degradation of analog performance due to technology scaling
2) Increase of cost and development time for analog circuits
3) Increasing needs for flexibility and re-configurability for multi-band and multi-mode systems

4.1 Sampling Mixer

Figure 10 shows the sampling mixer. The output signal from the LNA is once converted to the current signal by the transconductance amplifier. The current signal is sampled and held in capacitor C_h and C_r. The switch 1 is driven with the fast clock of which frequency is a carrier frequency and the switch 2_a to 2_h are rotated in every N clocks. Two capacitor banks A and B are used. At every capacitors in the bank A are charged, All capacitors are connected to the capacitor C_b by the switch 3 followed by resetting all capacitors. During this step, the capacitor bank B samples signal in each capacitor and these actions are repeated. Mixer action and filter action are realized through this process. Next this paper will consider the detail filter action.

First of all, the charge accumulates in the capacitor C_h and C_r through N times switching of the switch 1. The accumulated charge $W(z)$ is expressed using $U(z)$ that is the sampled charge at each clock,

$$W(z) = \sum_{n=0}^{N-1} U(z)z^{-n} = \frac{1-z^{-N}}{1-z^{-1}}U(z). \tag{18}$$

The Sinc filter characteristics is obtained by replacing $z = e^{j2\pi\frac{f}{f_s}}$.

$$|W(f)| = \left|\frac{\sin\left(N\pi\dfrac{f}{f_s}\right)}{\sin\left(\pi\dfrac{f}{f_s}\right)}\right|. \tag{19}$$

Figure 11 shows the filter characteristics when N is 8. The stop band is located at the integral multiple of f_s/N.

Next, the charge is stored in the capacitor C_h and C_r, however the C_r is changed every N clocks.

The total stored charge $S(z)$ in C_h and C_r is expressed using $W(z)$ that is the instantaneous charge of C_h.

$$S(z) = \frac{W(z)}{1-az^{-N}}, \tag{20}$$

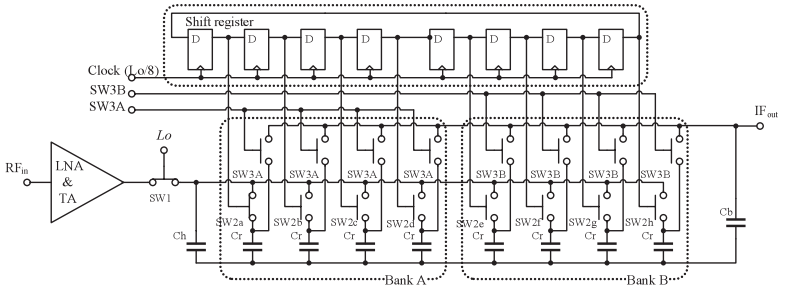

Fig. 10 Sampling mixer.

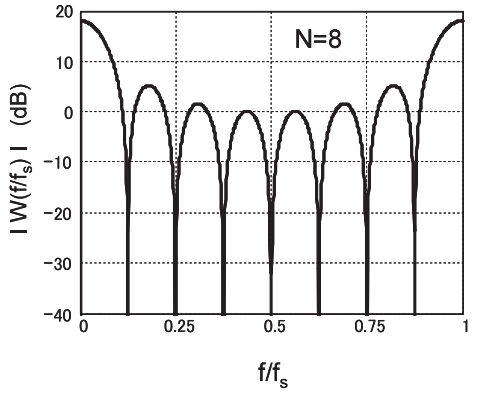

Fig. 11 Frequency characteristics of the Sinc filter.

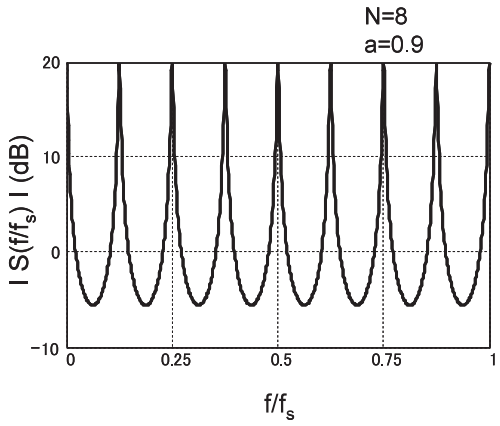

Fig. 12 Frequency characteristics of the IIR filter.

where $a = \frac{C_h}{C_h+C_r}$.

The IIR filter characteristic is obtained by

$$|S(f)| = \frac{1}{\sqrt{1 + a^2 - 2a\cos\left(N2\pi\dfrac{f}{f_s}\right)}}. \tag{21}$$

Figure 12 shows the IIR filter characteristics, when $N = 8$ and $a = 0.9$. A deep attenuation can be obtained by the setting the coefficient close to unity as possible. Since the pass band of this IIR filter is located at the integral multiple of f_s/N and this location is same as the stop band frequency of the Sinc filter, unwanted signals can be suppressed.

At the reading mode, M capacitors are connected parallel and this forms the Sinc filter.

The reading charge $T(z)$ is expressed using the stored charge $(1 - a)S(z)$.

$$\begin{aligned} T(z) &= (1-a)\sum_{l=1}^{M} S(z)z^{-Nl} \\ &= (1-a)\frac{z^{-N}\left(1-z^{-MN}\right)}{1-z^{-N}}S(z). \end{aligned} \tag{22}$$

The frequency characteristics is

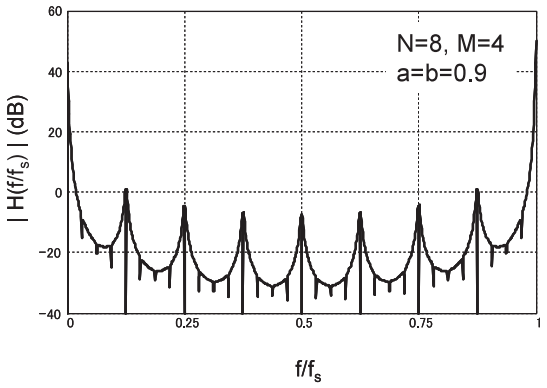

Fig. 13 Frequency characteristics of the sampling mixer.

$$|T(f)| = (1-a)\left|\frac{\sin\left(MN\pi\dfrac{f}{f_s}\right)}{\sin\left(N\pi\dfrac{f}{f_s}\right)}\right|. \tag{23}$$

Also the charge transfer to C_b forms a IIR filter.

The stored charge in capacitor C_b, $Y(z)$ is expressed using the instantaneous charge of C_b, $T(z)$.

$$Y(z) = \frac{Y(z)}{1 - bz^{-MN}}. \tag{24}$$

The frequency characteristics is given as

$$|Y(f)| = \frac{1}{\sqrt{1 + b^2 - 2b\cos\left(MN2\pi\dfrac{f}{f_s}\right)}}, \tag{25}$$

where $b = \frac{C_b}{4C_r+C_b}$.

The total filter characteristics is summarized

$$\begin{aligned} |H(f)| = (1-a)&\left|\frac{\sin\left(MN\pi\dfrac{f}{f_s}\right)}{\sin\left(\pi\dfrac{f}{f_s}\right)}\right| \\ &\cdot\frac{1}{\sqrt{1 + a^2 - 2a\cos\left(N2\pi\dfrac{f}{f_s}\right)}} \\ &\cdot\frac{1}{\sqrt{1 + b^2 - 2b\cos\left(MN2\pi\dfrac{f}{f_s}\right)}}. \end{aligned} \tag{26}$$

Figure 13 shows the total filter characteristics of the sampling mixer when $N = 8$, $M = 4$, $a = 0.9$, $b = 0.9$. The pass bands are located at the DC and the carrier frequency and direct conversion mixer action is realized with filter characteristics. 50 dB suppression for unwanted signals is expected. In contrast to the conventional RF and IF filters such as the LC filter and the SAW filter are difficult to be integrated on a LSI and difficult to change the characteristics, while this technology enables an integration on

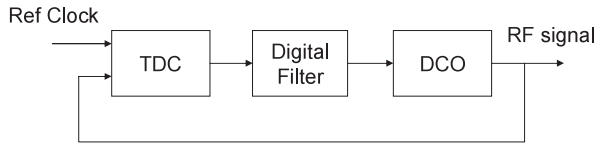

Fig. 14 All digital PLL.

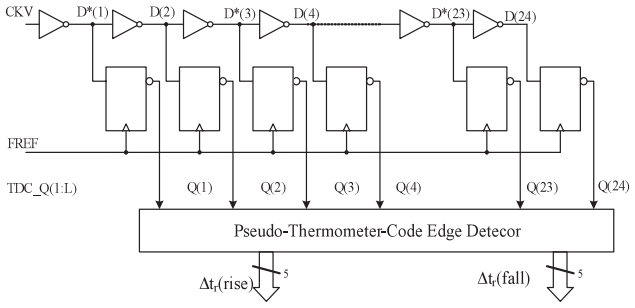

Fig. 15 Time to Digital converter (TDC).

LSI and flexibility of the filter characteristics by changing the parameters, such as M, N, a, and b. Furthermore the low power consumption and the high linearity are expected since no active devices but passive devices, such as switches and capacitors are used.

4.2 All Digital PLL

The PLL technology is very important for the wireless systems to be used in frequency synthesizer to generate accurate frequency with small phase noise. The conventional PLL system uses the PFD, the charge pump, the analog filter, and the VCO. In contrast, the all digital PLL uses the Time to Digital Converter (TDC) that measures time difference by the inverter chain and latches, the digital filter, and the Digital Controlled Oscillator (DCO) as shown in Fig. 14 [11]. Digitalization enables an adaptive filter and free from gate leakage issue of MOS capacitor that causes the timing jitter and becomes serious along with the technology scaling. The TDC measures phase difference between the reference clock and the VCO signal by using inverter delay, as shown in Fig. 15. Time resolution is 40 ps and will be reduced along with the technology scaling. Frequency is controlled by the array of varactors. In contrast to the conventional analog control way that uses most sensitive region of varactors, this technology uses the most insensitive two regions and control the capacitance by changing the number of connected capacitors to suppress the phase noise, as shown in Fig. 16 [12], [13].

This way reminds us that the most controllable point that uses in analog technology is also the most sensitive point to the noise. The resolution of this DCO is 6 bit and the delta-sigma modulation is used to suppress the quantized phase noise. The other remarkable features have not been announced so far and the future progress should be expected.

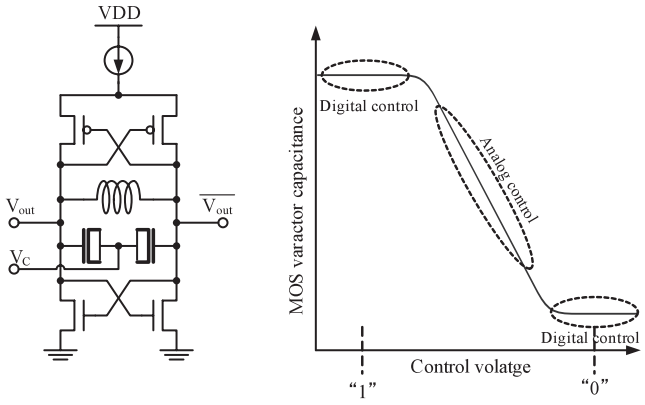

Fig. 16 Digital Controlled Oscillator (DCO).

5. Conclusion

This paper reviews and discusses the analog IC technology for the future wireless systems. Namely, the analog features and the issues of a scaled CMOS transistor, the basic issue and the technology trend of ADC as an important building block of wireless systems, and the feature of the digital RF architecture that has been proposed recently as an important technology trend have been reviewed and discussed.

High speed and low power consumption is expected for the low SNR systems along with the further technology scaling, however the realization of high SNR system becomes difficult due to the decrease of signal voltage affected by the operation voltage lowering. One important technology trend is the digitalization of RF signal to realize the system flexibility, robustness, area shrinking, and TAT shortening. An expansion of application area of the digital signal processing to the RF signal must become the big technology trend and an increase of the clock frequency of CMOS technology supports it. Through this process, the conventional continuous time analog circuits will be replaced by the discrete time analog circuits or digital circuits.

However the analog technology in a broad sense become important more and more, for example the accuracy of the TDC and the characteristics of the sampling mixer should be progressed and these depend on the analog characteristics. The progress of new circuit and system technology that involves the mixture of analog and digital technology should be expected.

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