Nano-scale CMOS and Low Voltage Analog to Digital Converter Design Challenges

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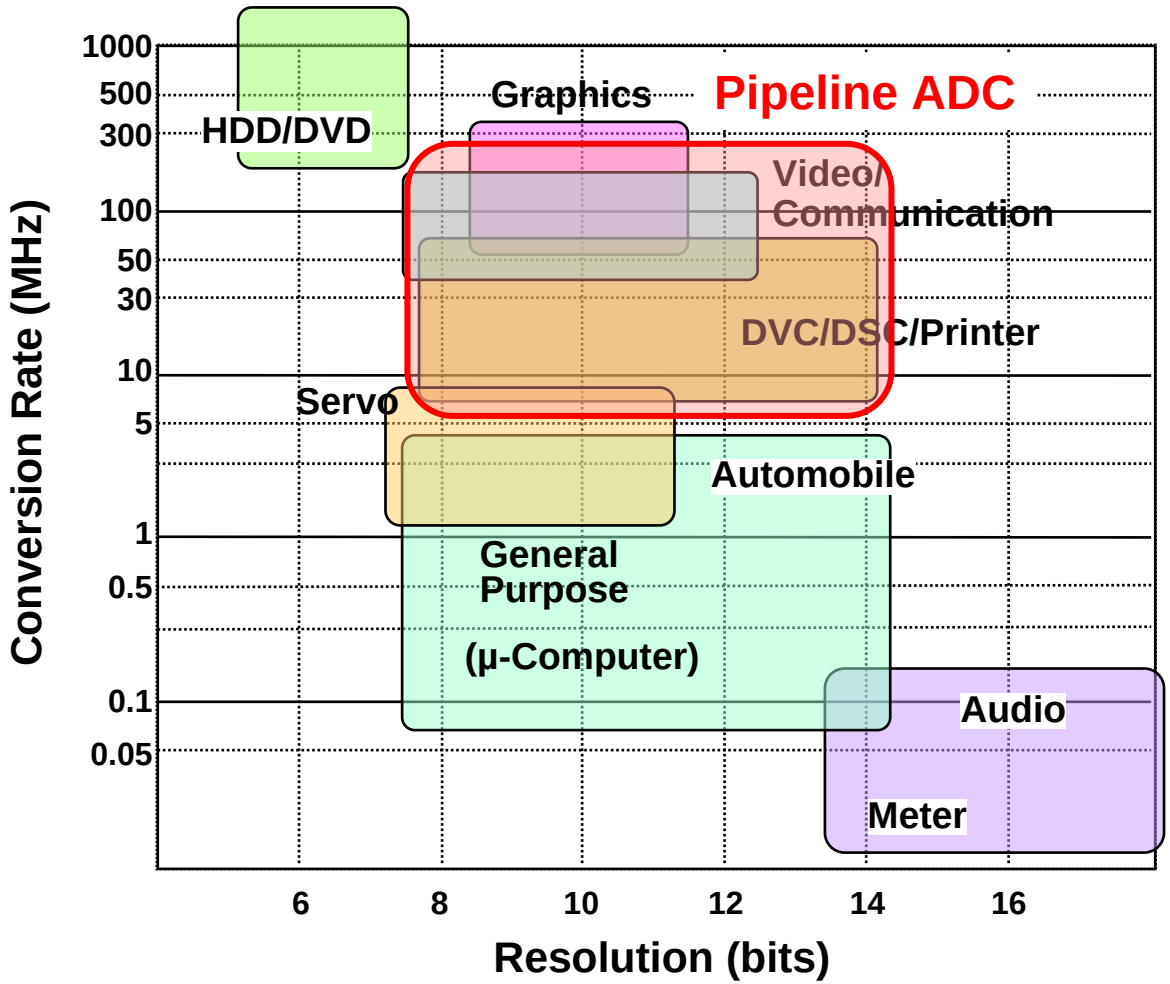
   - Successive approximation ADC
   - Sub-ranging ADC

4. **Summary**

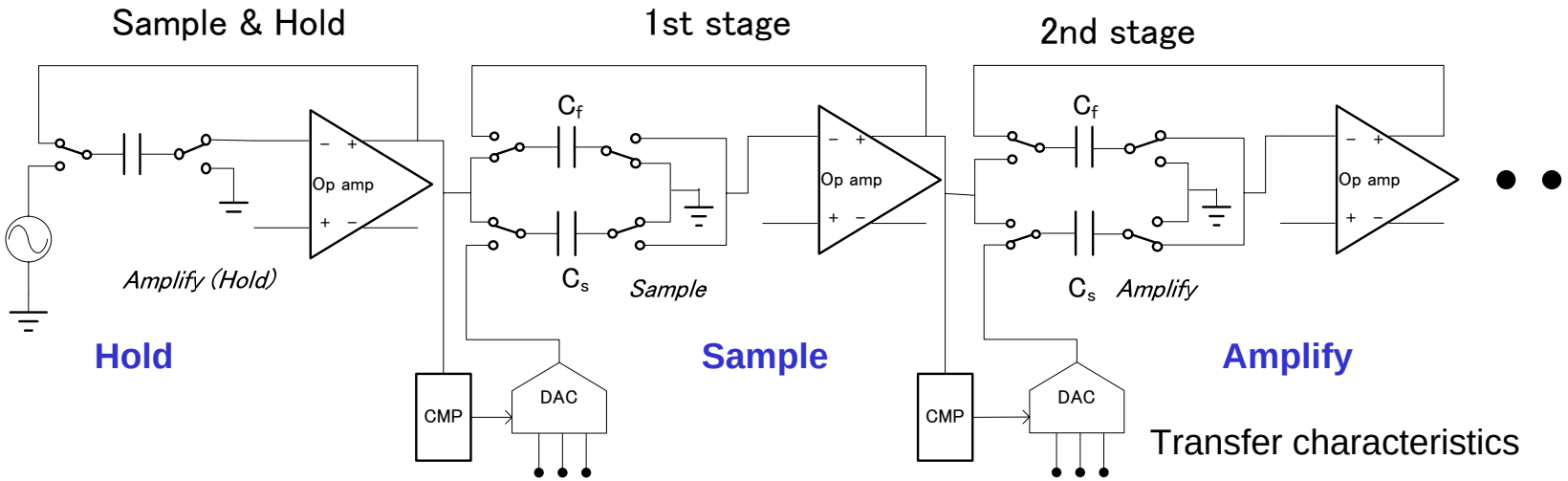
Performance and applications

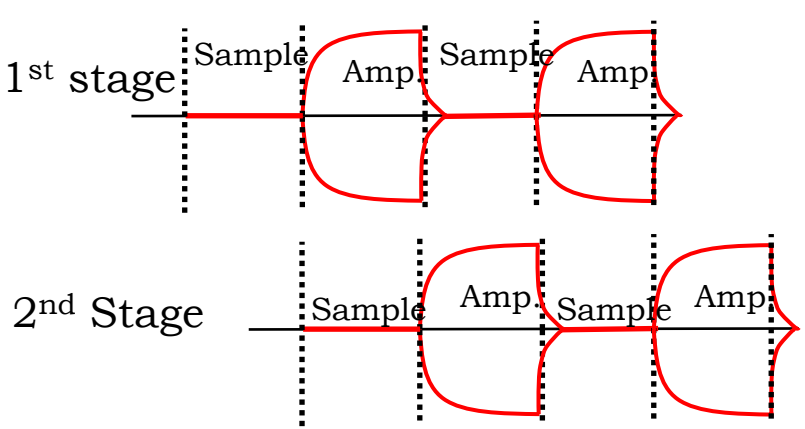
Pipeline ADC is the major conversion architecture for communications and digital consumer products.

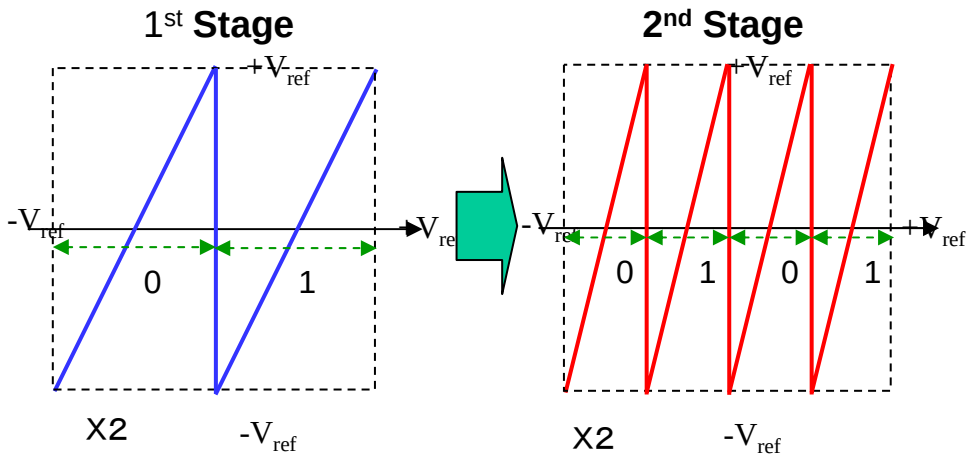


Pipeline ADC

Folding I/O characteristics makes higher resolution along with pipeline stages.

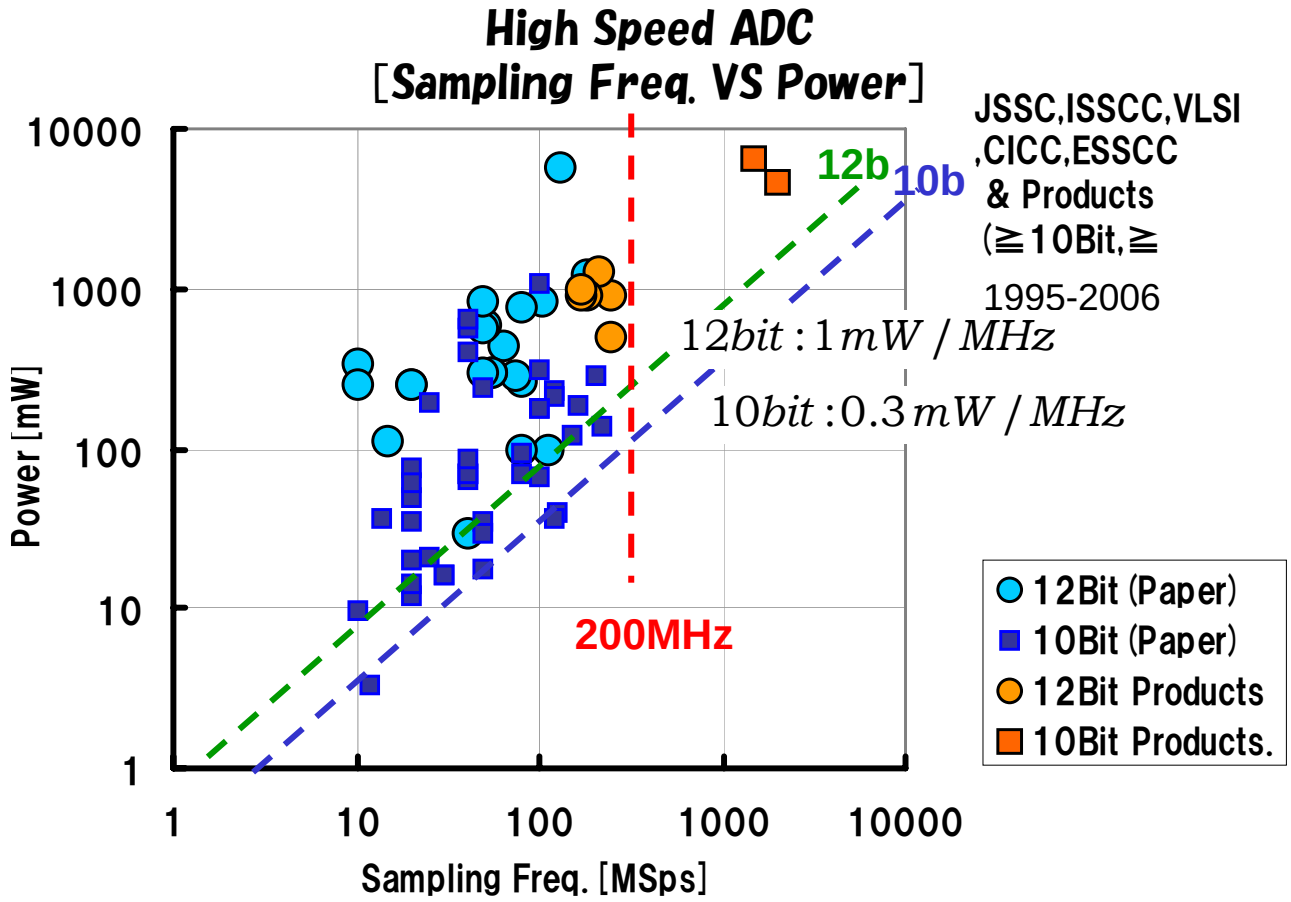






Speed and power

Conversion speed has saturated at 200 MHz
Smaller mW/MHz is needed for low power operation.
0.3mW/MHz for 10bit and 1mW/MHz for 12bit are the bottom lines.

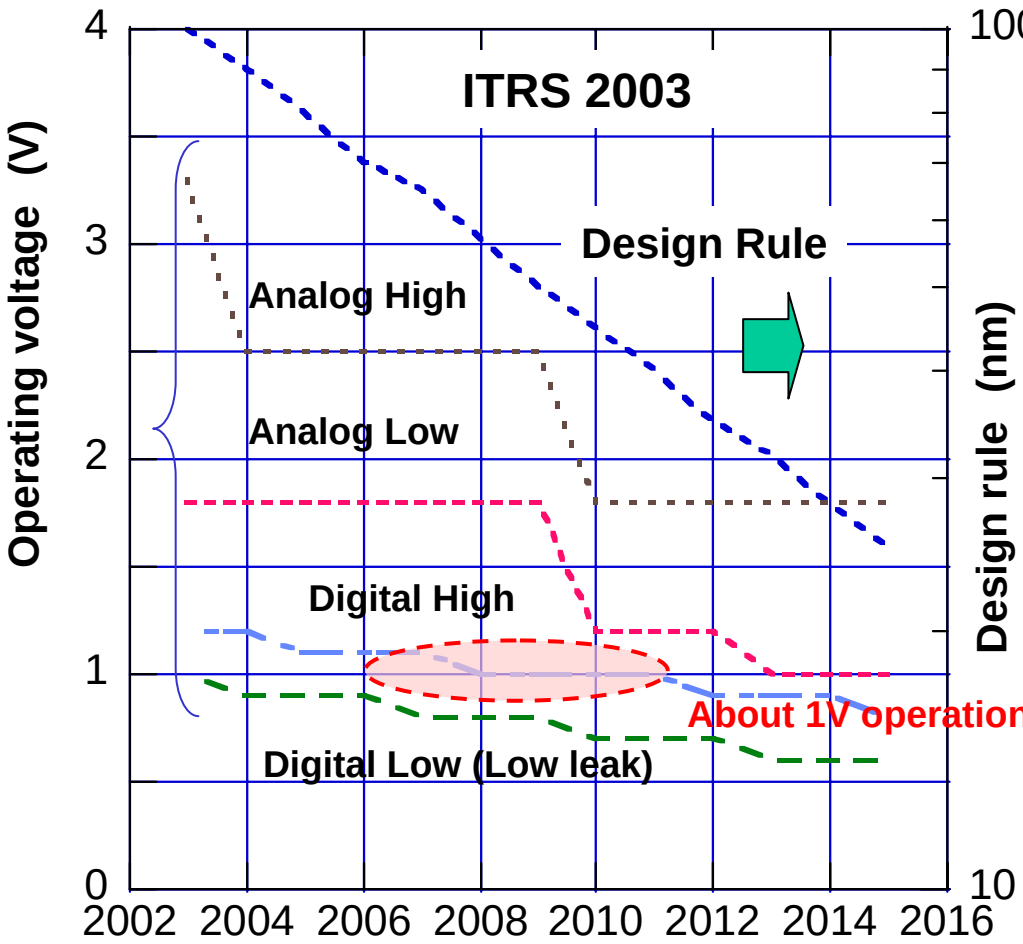


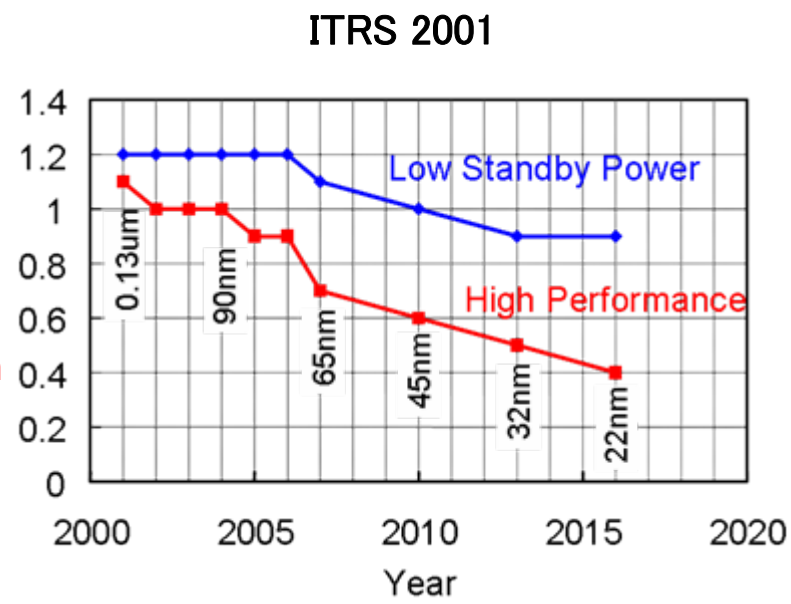
Effect of technology scaling on analog performance

Technology scaling and performance of pipeline ADC

Operating voltage trend

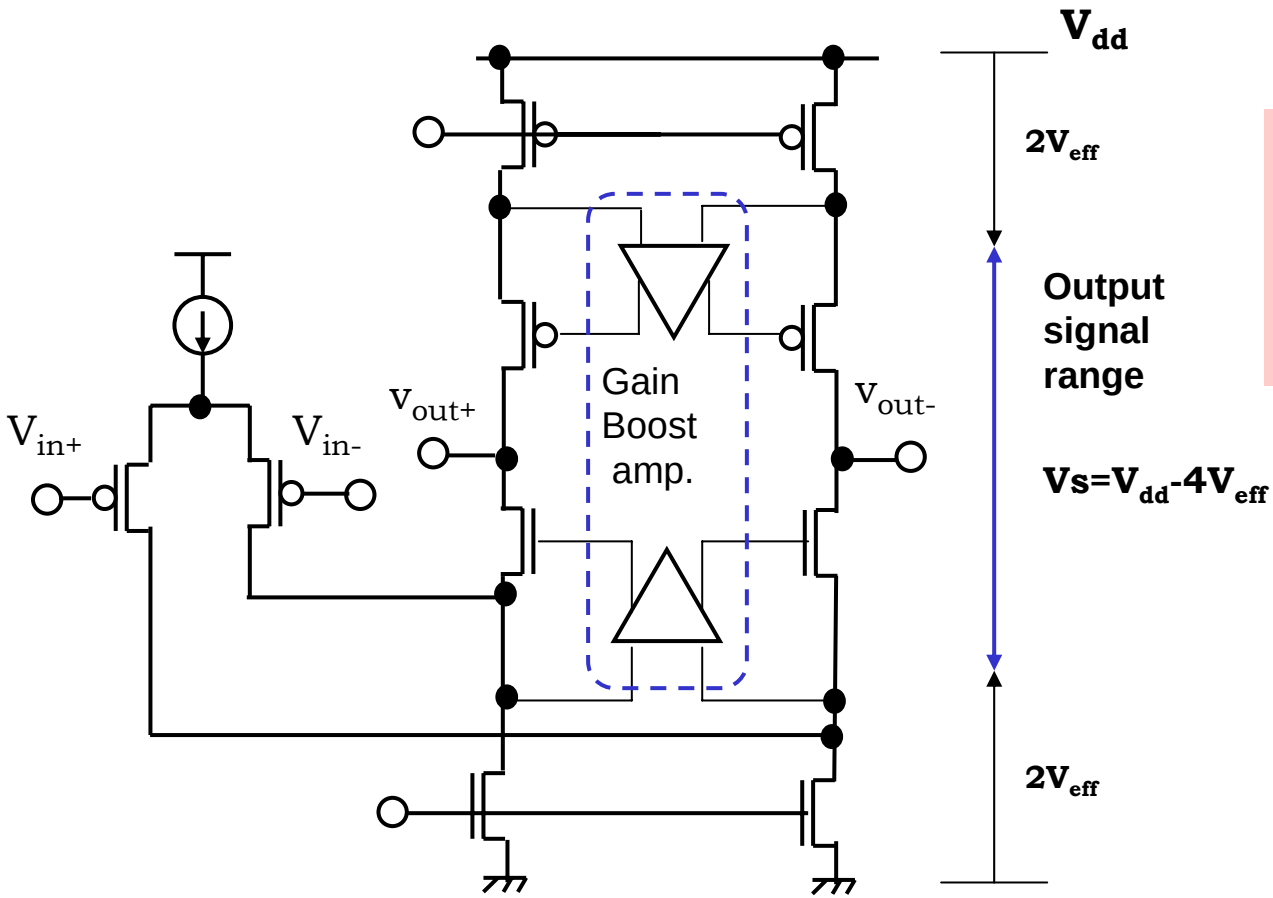
Operating voltage of scaled device will keep about 1V





Operational amplifier for ADC

Pipeline ADC needs high performance amplifier.
The output signal range will be reduced along with voltage lowering.



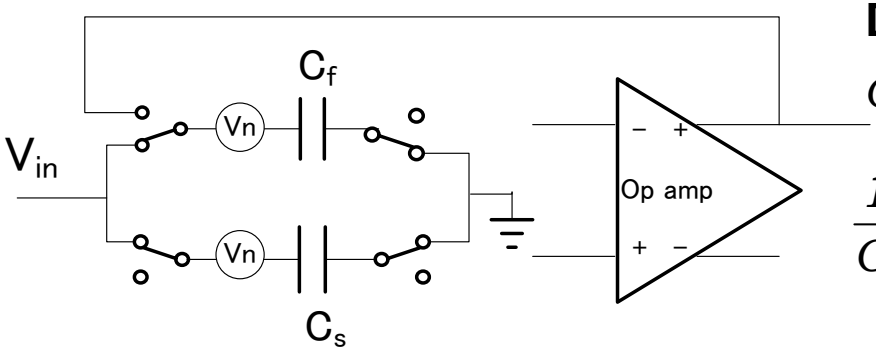
$V_s=V_{dd}-0.7V$

$V_s=0.5V$ @$V_{dd}=1.2V$
$V_s=0.3V$ @$V_{dd}=1.0V$

Requirements for operational amplifier

Higher resolution requires higher open loop gain.
Higher conversion frequency requires higher closed loop GBW.

Sampling



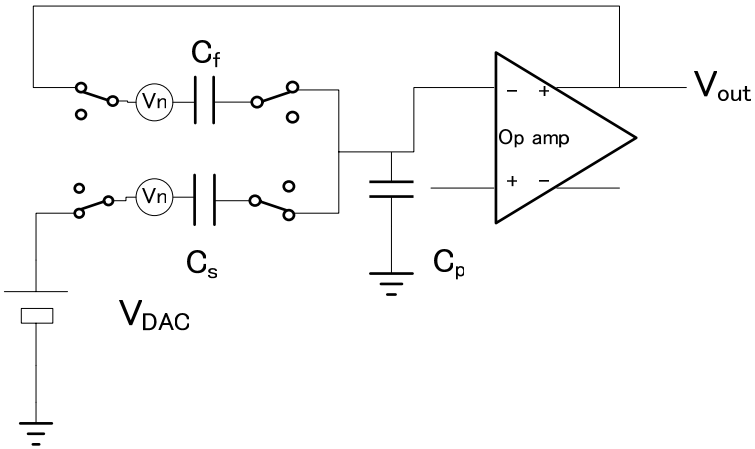
DC gain

$$G_{error} \approx -\frac{1}{G}\left(2+\frac{C_p}{C_f}\right) \approx -\frac{1}{G\beta} \qquad \beta \equiv \frac{1}{\left(2+\frac{C_p}{C_f}\right)}$$

$$\frac{1}{G} \le \frac{\beta}{2^{N-M+1}}$$

N:ADC resolution
M : Stage resolution

Amplify



$$G(dB) > 6N + 10$$ **for 1.5b pipeline ADC**

Closed loop gain-bandwidth

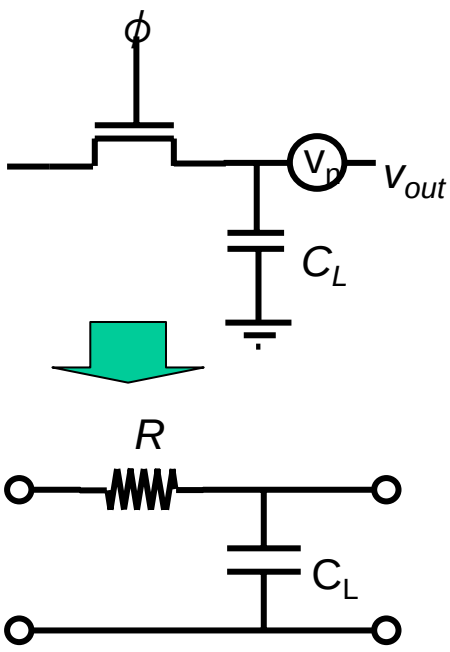
$$GBW_{\_close} = \frac{g_m \beta}{2\pi C_L} > \frac{N \cdot fc}{3}$$

$$\beta = \frac{C_f}{C_f + C_s + C_{pi}}$$

$$C_L = C_{po} + C_{oL} + \frac{C_f\left(C_s + C_{pi}\right)}{C_f + C_s + C_{pi}}$$

kT/C noise

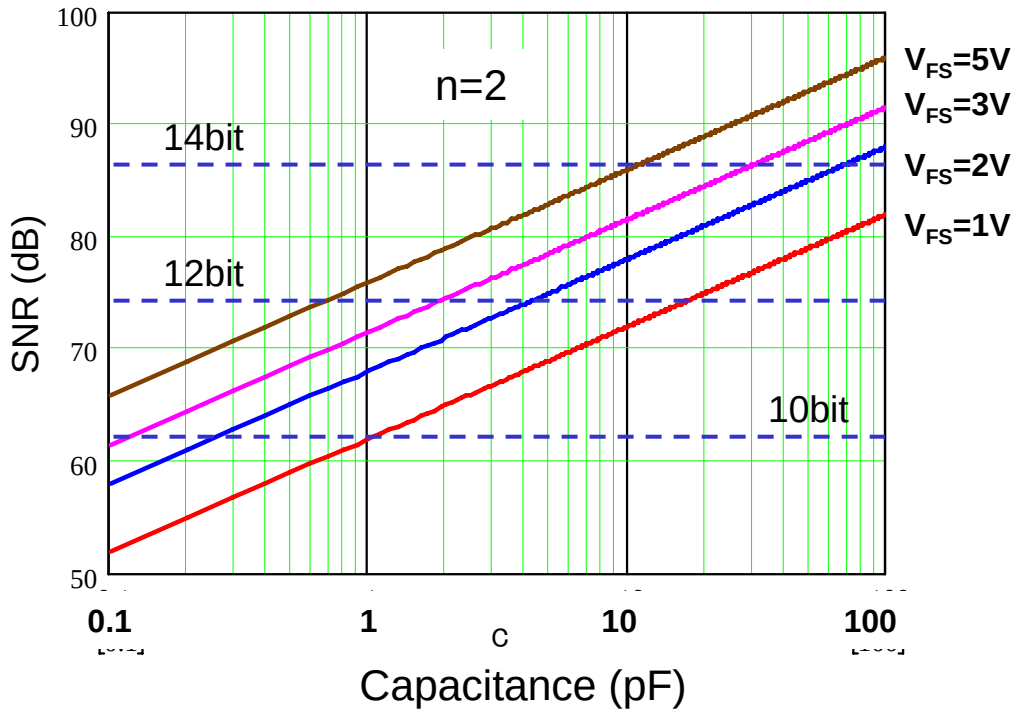
Larger SNR requires larger capacitance and larger signal swing.
Low signal swing increases required capacitance.



$$\overline{v_n^2} = \frac{nkT}{C}$$ n: configuration coefficient

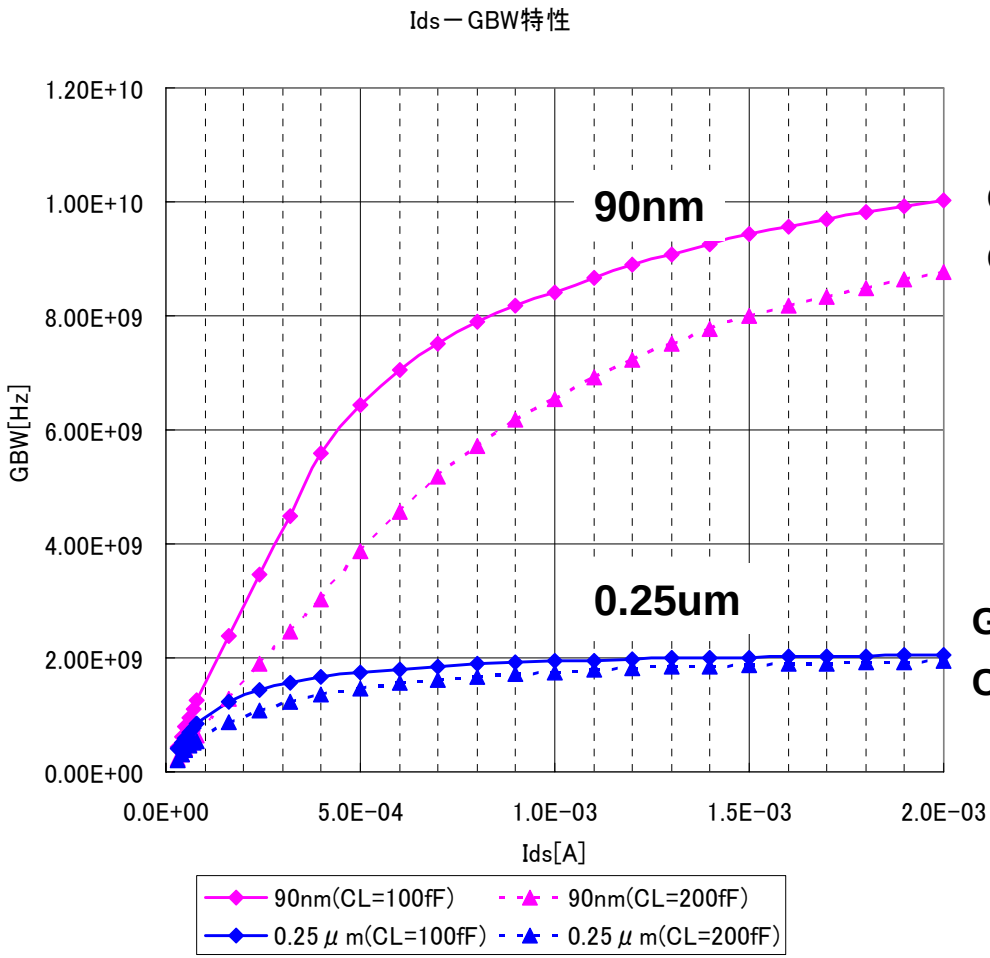
$$SNR(dB) = 10\log\left(\frac{CV_{FS}^2}{8nkT}\right)$$

$$\left\langle v_n^2 \right\rangle = 4kTR\int \frac{1}{1+(\omega CR)^2}\frac{d\omega}{2\pi} = \frac{kT}{C}$$



Effect of technology scaling

Gain bandwidth of OpAmp increases along with technology scaling.
However, can we increase every needed performances for ADCs?



GBW: 10GHz

Conversion freq. : 1GHz

GBW: 2GHz

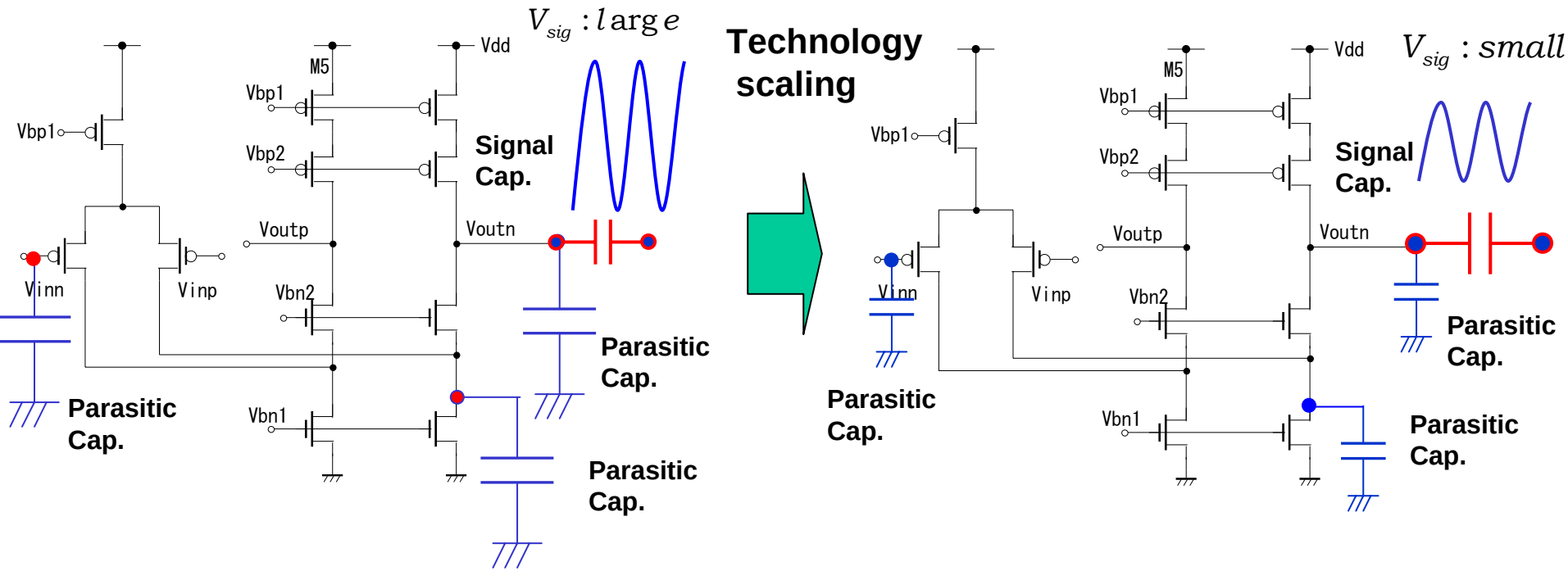
Conversion freq. : 200MHz

Technology scaling for analog

Technology scaling can reduce parasitic capacitances. However signal capacitance will increase to keep the same SNR at lower voltage operation.

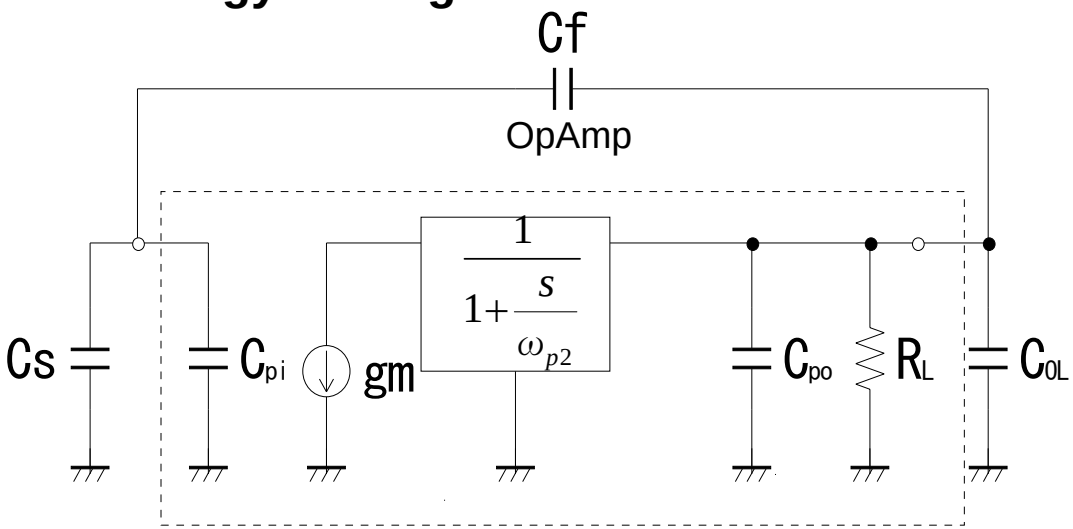
Parasitic capacitance → smaller
Operating voltage → lower
Signal swing → lower

Signal capacitance →larger
Voltage gain →lower



Performance model for pipeline ADC

We have developed the performance model for pipeline ADC that can treat technology scaling.



g_m : *Transconductance of input stage*
C_s, C_f : *Signal capacitance for feedback loop*
C_{pi}, C_{po} : *input & putput paracitic capacitance*
C_{oL} : *Load capacitance*
R_L : *Output resistance*
ω_{p2} : *Second pole of OpAmp*

A. Matsuzawa, "Analog IC Technologies for Future Wireless Systems," IEICE, Tan on Electronics, Vol. E89-C, No.4, pp. 446-454, April, 2006.

$$GBW_{\_close} = \frac{g_m}{2\pi C_L}\beta$$

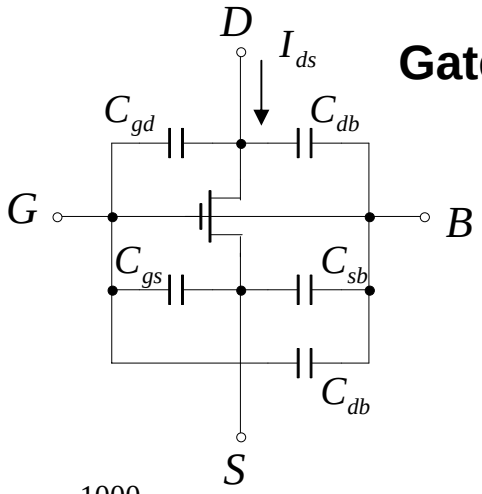
$$\beta = \frac{C_f}{C_f + C_s + C_{pi}}$$

$$C_L = C_{po} + C_{oL} + \frac{C_f\left(C_s + C_{pi}\right)}{C_f + C_s + C_{pi}}$$

$$C_{oL} = \frac{C_s + C_f}{2} \qquad C_o = C_s = C_f = C_{oL}$$

$$GBW_{\_close} = \frac{g_m}{2\pi C_o}\frac{1}{\left(2+\frac{C_{pi}}{C_o}\right)\left(1+\frac{C_{po}}{C_o}\right)+\left(1+\frac{C_{pi}}{C_o}\right)} = \frac{I_{ds}}{\pi C_o V_{eff}}\frac{1}{\left(2+\frac{\alpha_{pi}I_{ds}}{C_o}\right)\left(1+\frac{\alpha_{po}I_{ds}}{C_o}\right)+\left(1+\frac{\alpha_{pi}I_{ds}}{C_o}\right)}$$

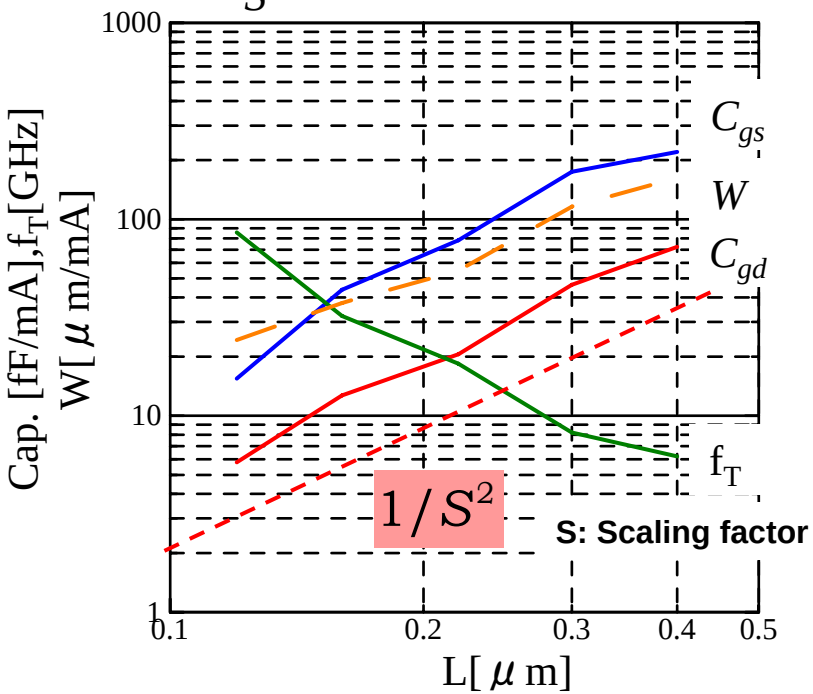
Scaling and analog device and circuit parameters



Gate width and capacitances decrease with technology scaling.

V_{eff}=0.175V

$$W = \frac{2L}{\mu C_{ox} V_{eff}^{\ 2}} I_{ds}$$



(a)W_N,W_P[μm/mA],V_{A_N}, V_{A_P}[V]

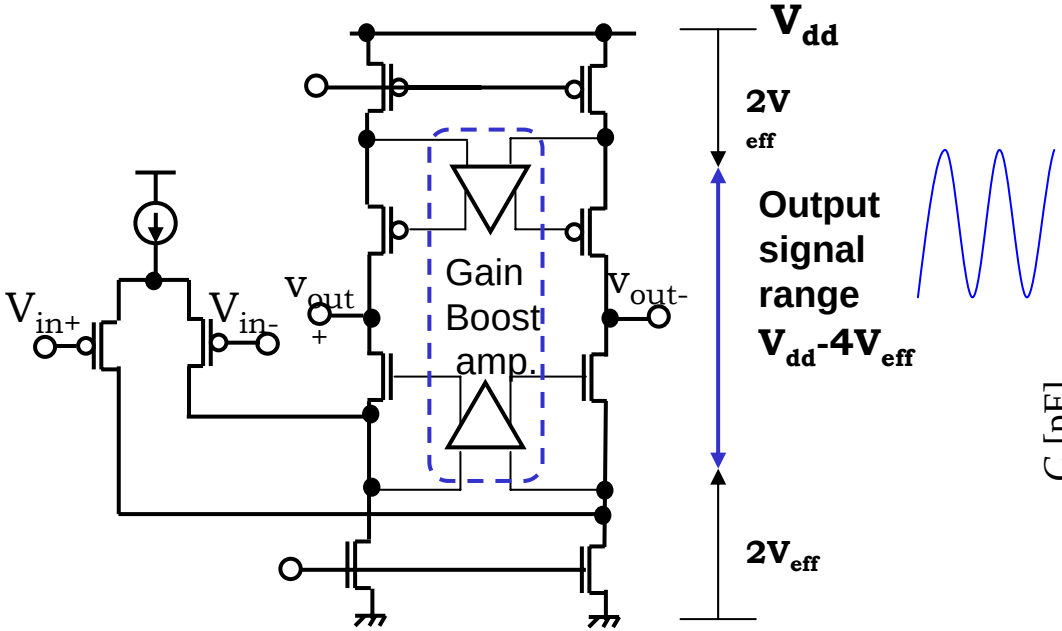
DR	W_N	W_P	V_{A_N}	V_{A_P}
90nm	24.3	74.9	0.82	0.69
0.13μm	37.5	147	0.82	0.64
0.18μm	54.8	219	0.99	0.93
0.25μm	116.0	396	0.78	0.97
0.35μm	162.0	603	1.01	0.86

(b)C_{pi_N}, C_{pi_P},C_{po}[fF/mA], ω_{p2_N}, ω_{p2_P}[GHz]

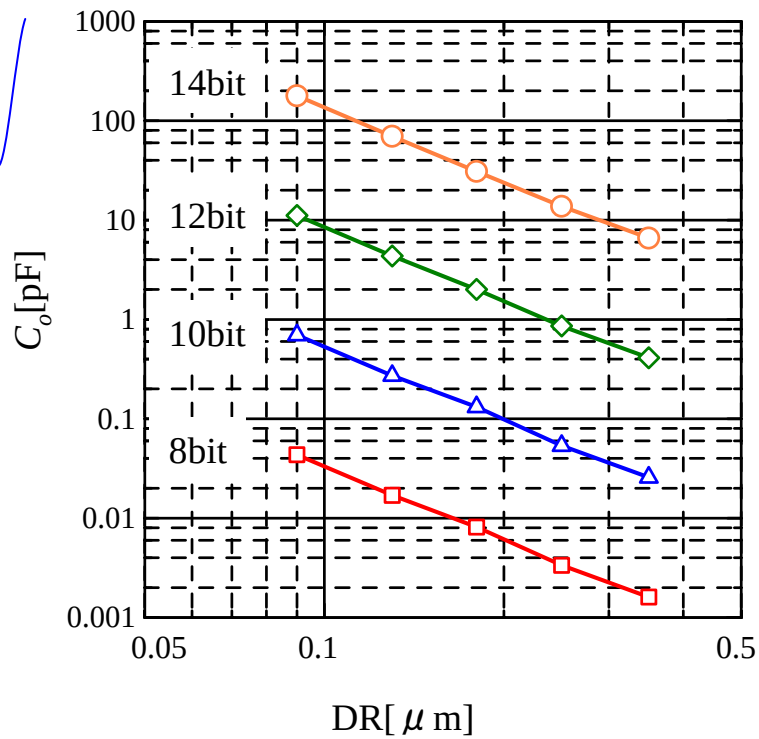
DR	C_{pi_N}	C_{pi_P}	C_{po}	ω_{p2_N}	ω_{p2_P}
90nm	23.7	93.4	94.5	9.35	15.4
0.13μm	65.5	249	168	7.7	10.3
0.18μm	115	475	340	2.06	4.7
0.25μm	236	662	832	0.83	1.7
0.35μm	303	1034	892	0.54	1.7

Determination of signal capacitance

Larger resolution requires larger signal capacitance.
Furthermore, Voltage lowering increases signal capacitance more.



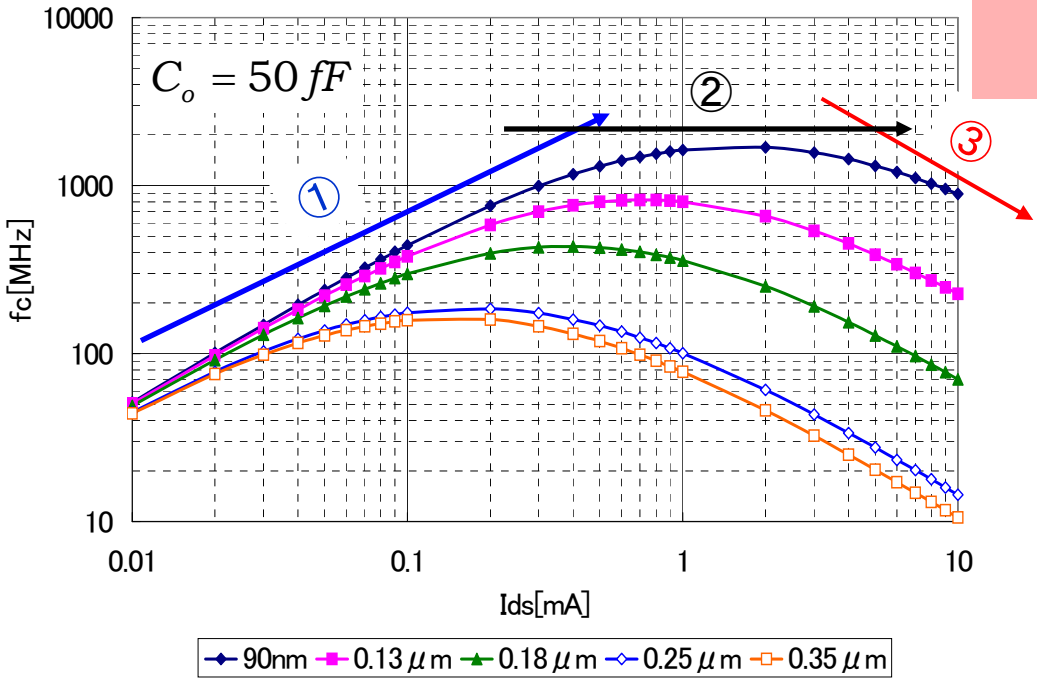
$$C_o \geq 1.66 \times 10^{-19} \left(\frac{2^N}{V_{sig}} \right)^2$$



	90nm	0.13 μm	0.18 μm	0.25 μm	0.35 μm
V_{dd}	1.2V	1.5V	1.8V	2.5V	3.3V
V_{sig_pp}	1.0V	1.6V	2.2V	3.6V	5.2V

Performance curve

Performance exhibits convex curve.
There is the peak conversion frequency and the optimum current.
Current increase results in increase of parasitic capacitances and decrease of conversion frequency in the higher current region.



$$GBW_{\_close} = \frac{g_m}{2\pi C_o} \frac{1}{\left(2+\frac{C_{pi}}{C_o}\right)\left(1+\frac{C_{po}}{C_o}\right)+\left(1+\frac{C_{pi}}{C_o}\right)}$$

$$g_m = \frac{2I_{ds}}{V_{eff}},\quad C_{pi} = \alpha_i I_{ds},\quad C_{po} = \alpha_o I_{ds}$$

①$C_o \gg C_{po}, C_{pi}$

$$GBW_{\_close} \approx \frac{I_{ds}}{\pi C_o V_{eff}} \cdot \frac{1}{3} \qquad (\propto I_{ds})$$

②$C_{pi} < C_o < C_{po}$

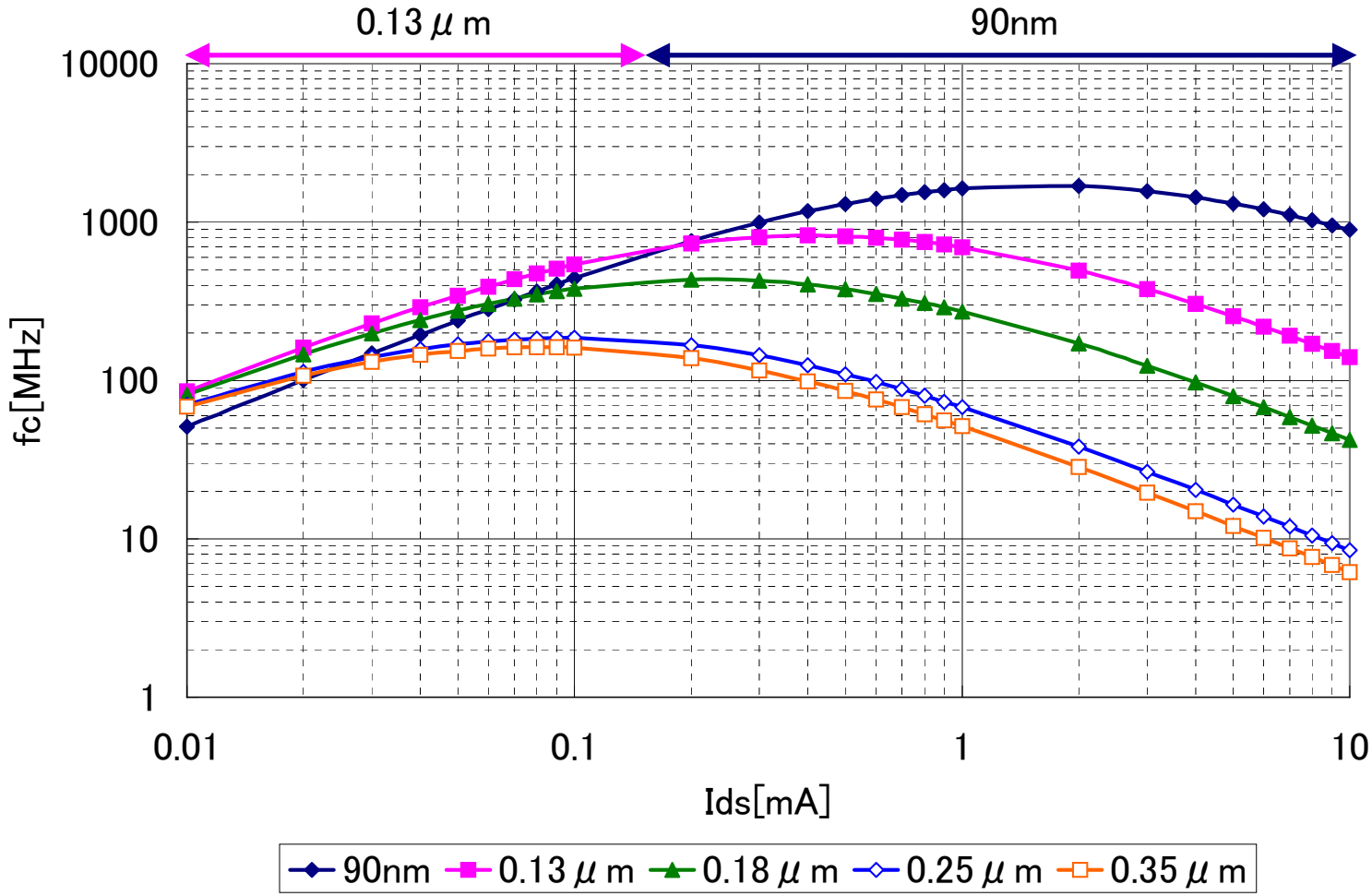
$$GBW_{\_close} \approx \frac{1}{\pi C_o V_{eff}} \cdot \frac{1}{3+\alpha_o} \qquad (Constant)$$

③$C_o < C_{po}$、$C_o < C_{pi}$

$$GBW_{\_close} \approx \frac{1}{\pi C_o V_{eff}} \cdot \frac{1}{3+\alpha_i \alpha_o I_{ds}} \qquad \left(\propto \frac{1}{I_{ds}}\right)$$

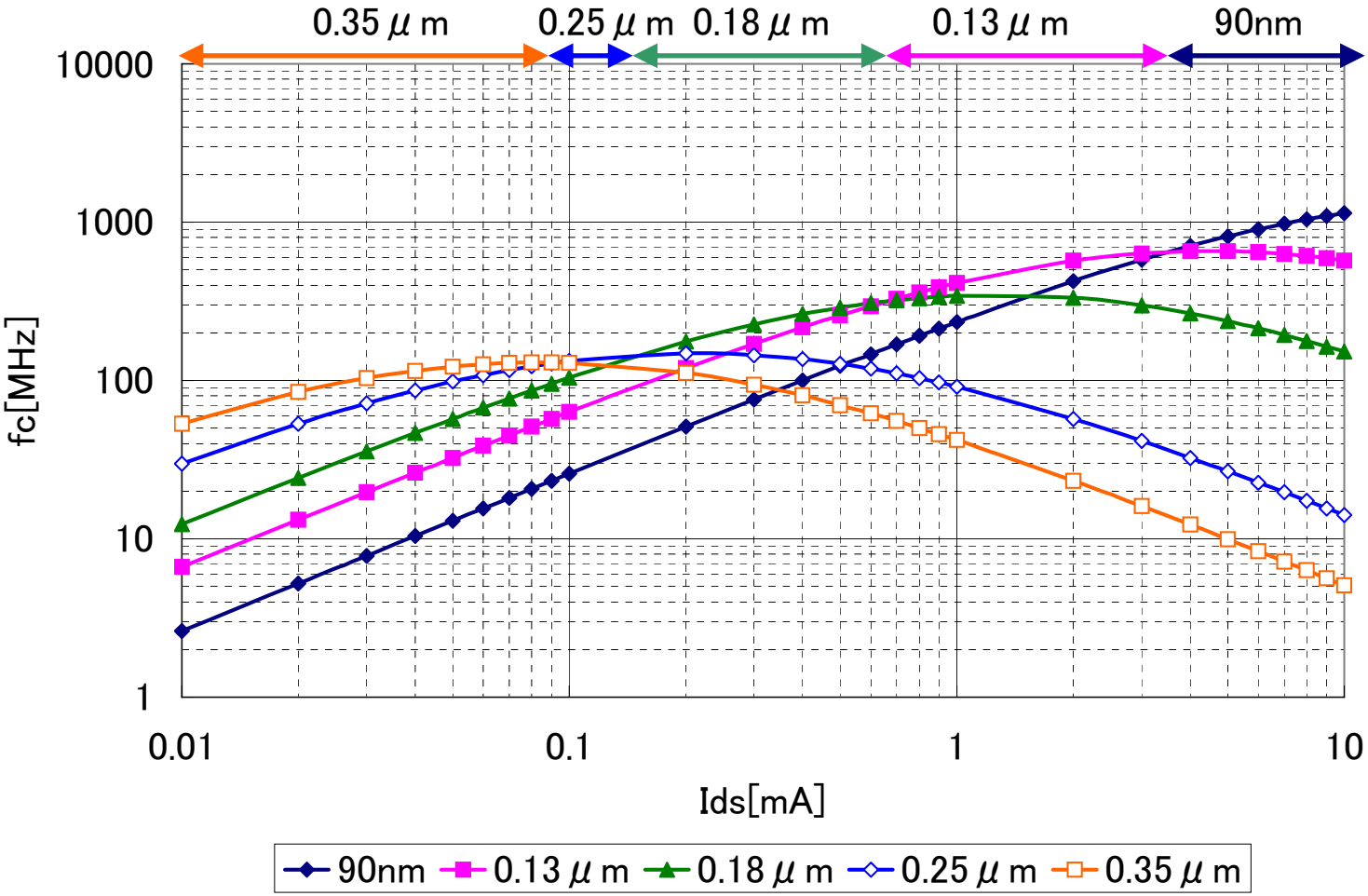
8 bit

0.13um attains highest conversion frequency in a low current region.
However 90nm is over striding 0.13um along with increase of the current.



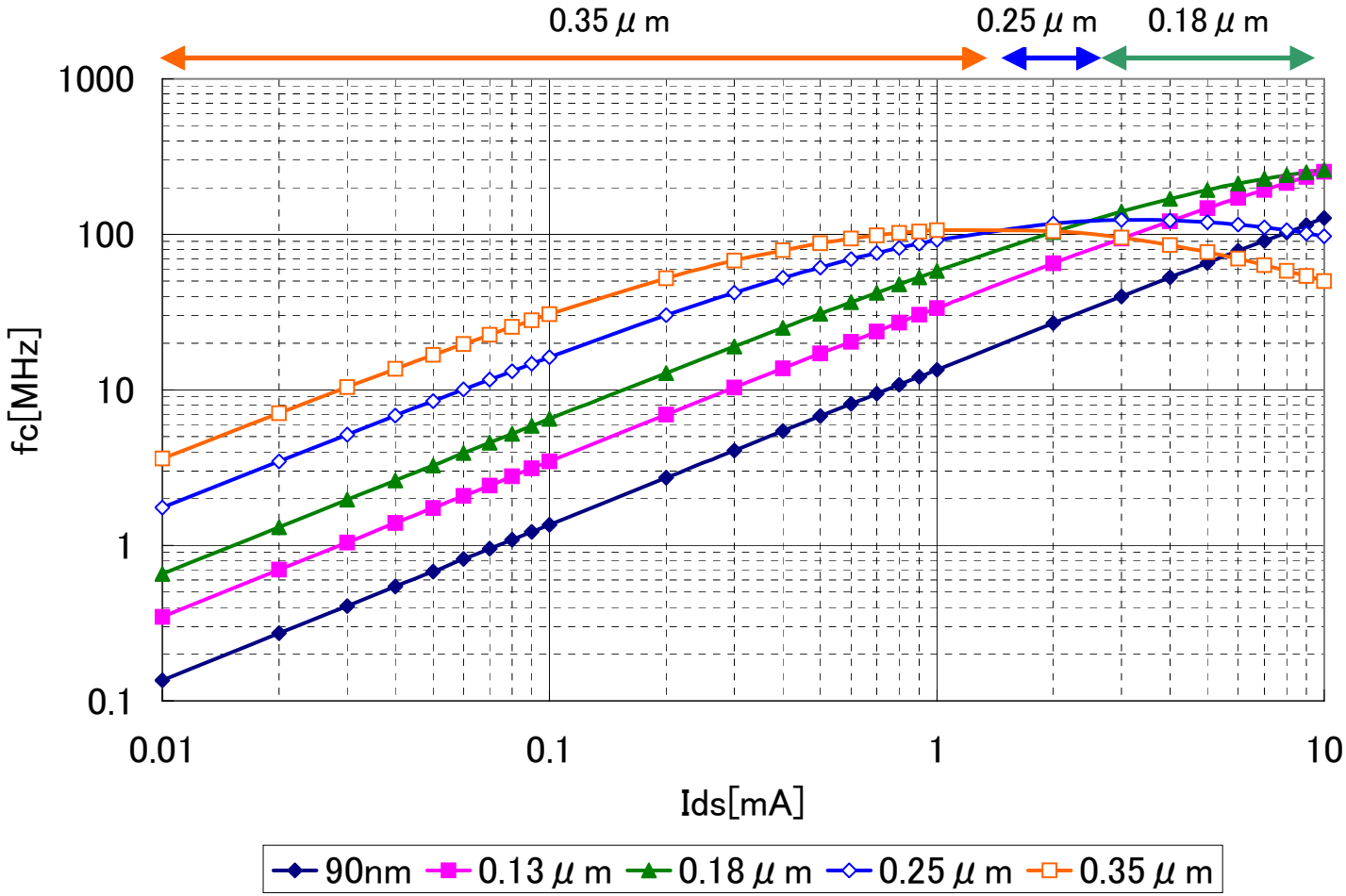
10 bit

The best design rule depends on operating current.
0.35um attains highest conversion frequency in low operating current region!



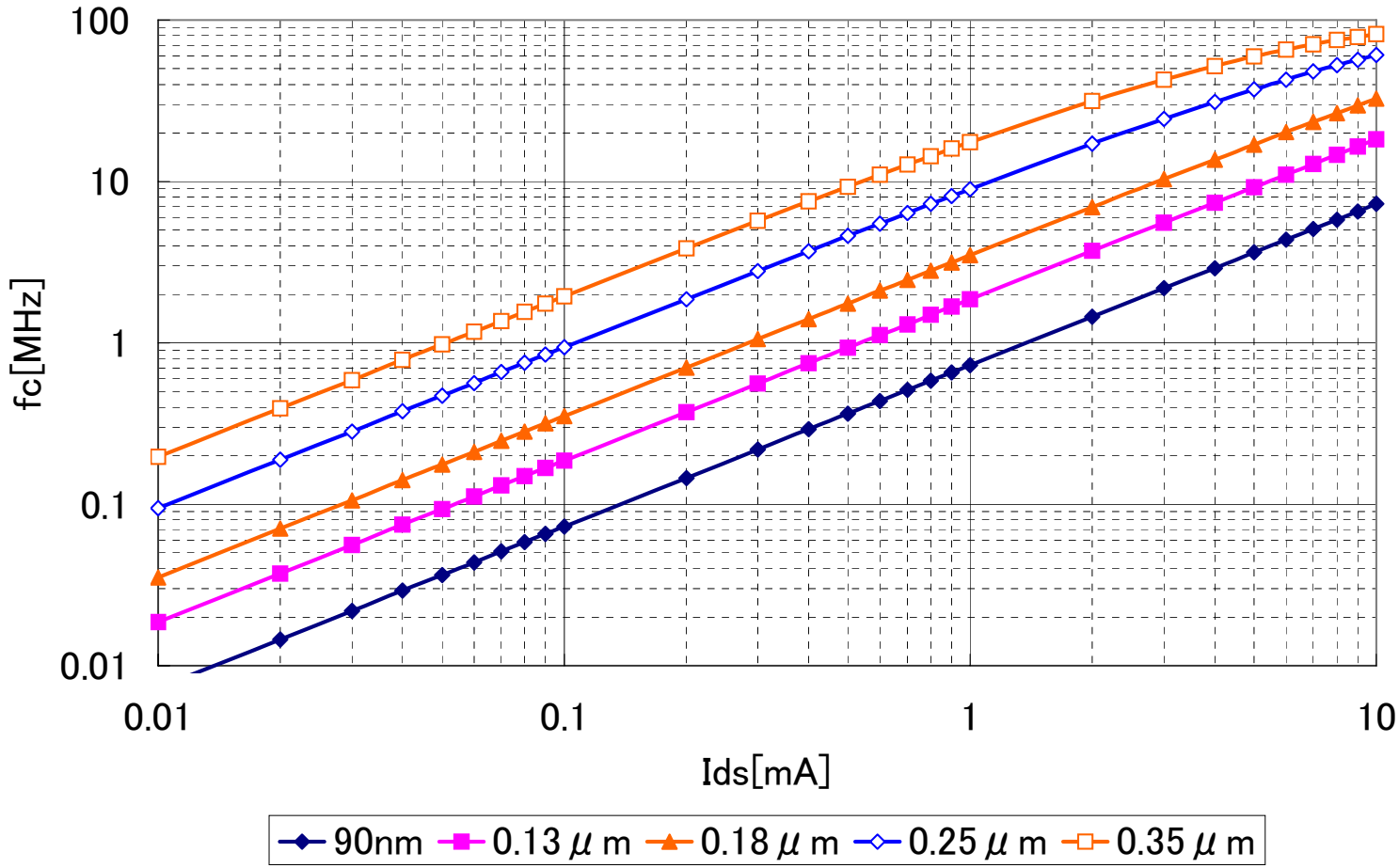
12 bit

Relaxed design rule is suitable for wider current range.



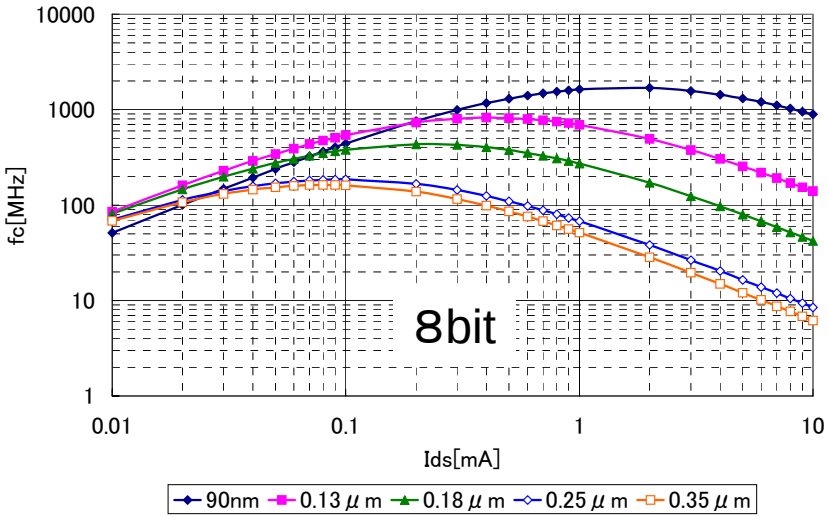
14 bit

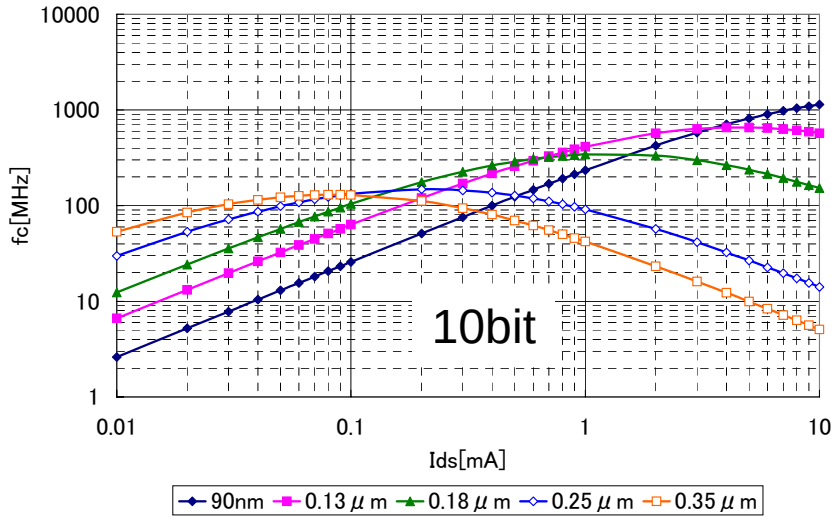
Scaled CMOS is not suitable for higher resolution ADC.

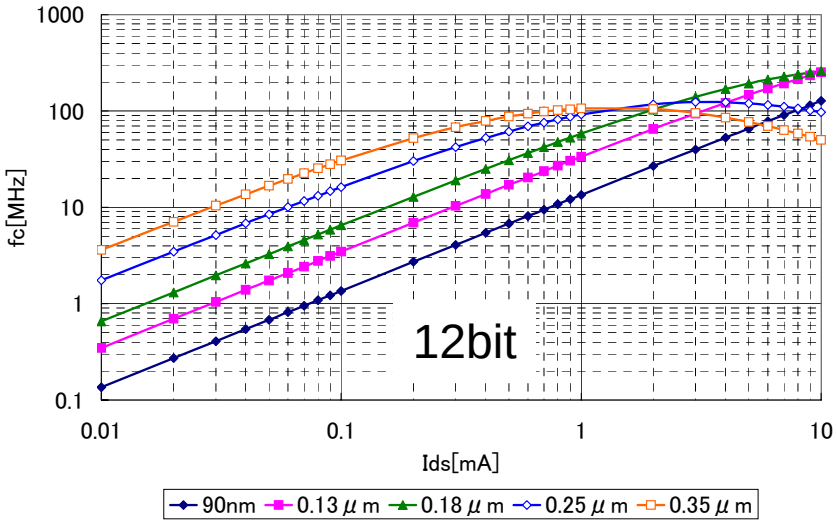


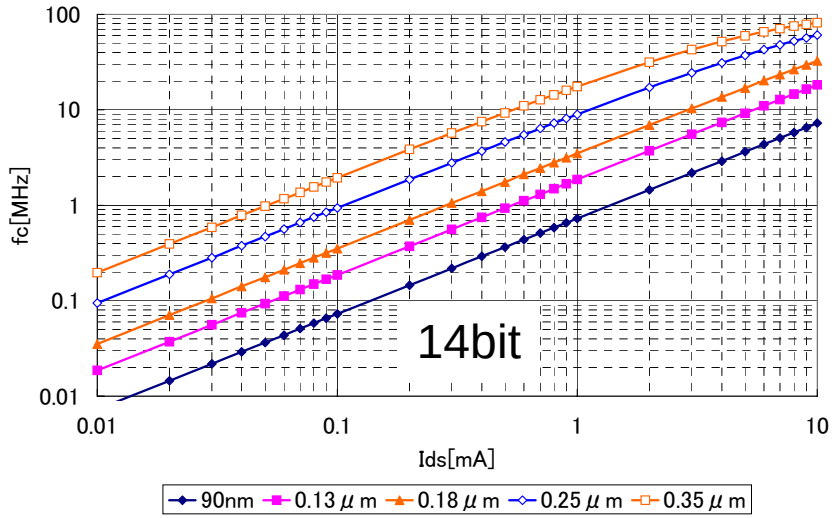
Performance summary

Scaled CMOS is effective for just low resolution ADC.
Scaled CMOS is not effective for high resolution ADC.





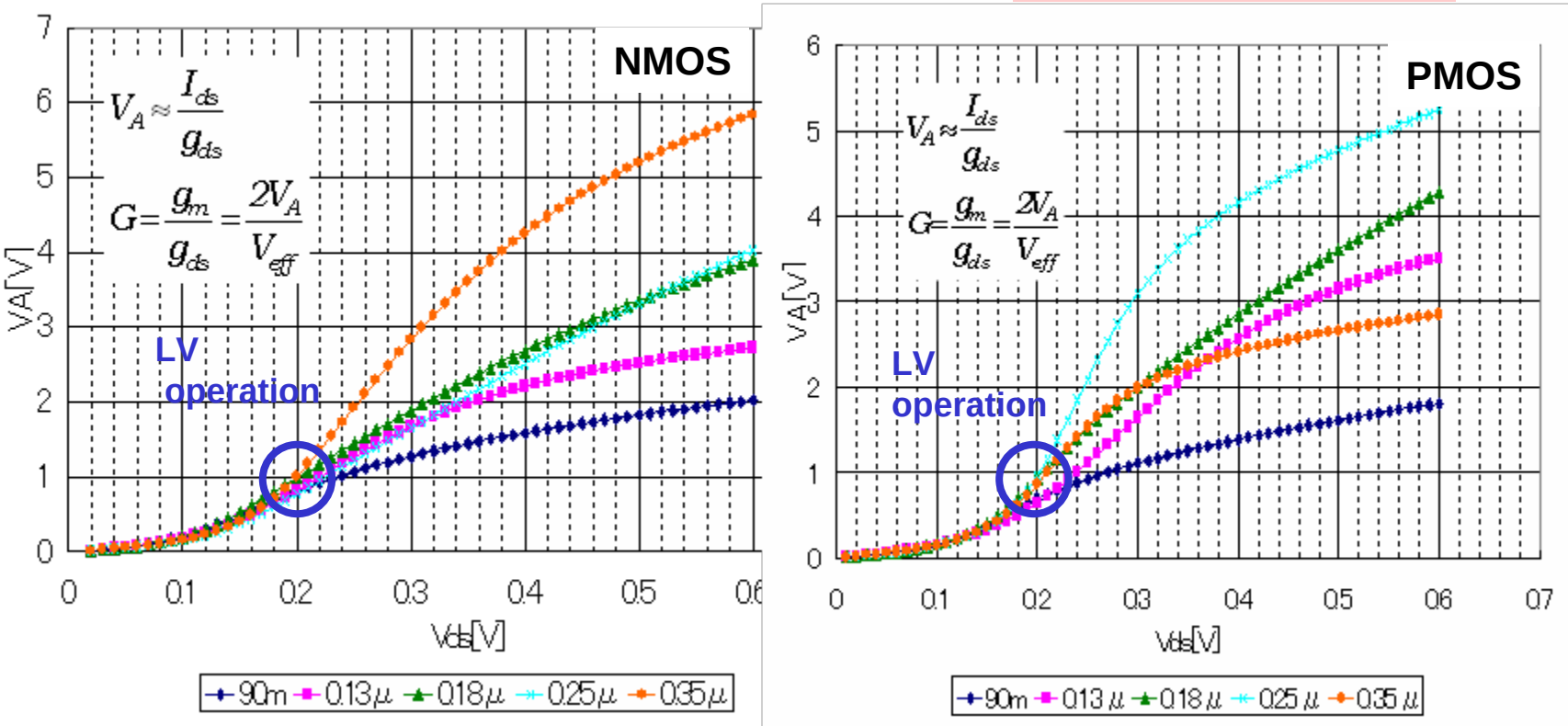




Voltage gain

V_A decreases with scaling and operating voltage lowering. High gain can not be expected.

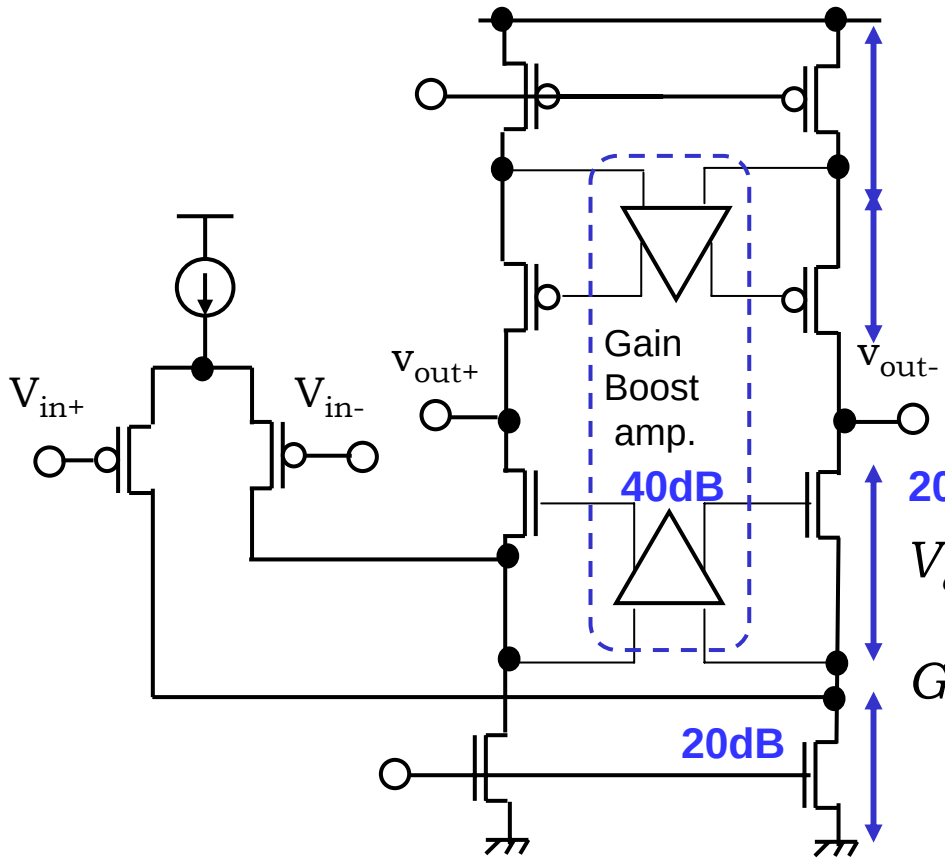
$$G_i = g_m \cdot r_{ds} \qquad g_m = \frac{2I_{ds}}{V_{eff}},\ r_{ds} = \frac{V_A}{I_{ds}} \qquad G_i = \frac{2V_A}{V_{eff}} \approx 10V_A$$



Voltage gain of operational amplifier

Voltage gain of OpAmp for scaled CMOS and LV operation is 80dB at most.

Less than 10 bit ADC can be designed with scaled and low voltage CMOS.



Total gain is 80dB @max

$$V_{ds} \approx V_{eff} \approx 0.2V$$

$$G_i = \frac{2V_A}{V_{eff}} \approx \frac{2}{0.2} = 20dB$$

Design challenges for ADC in nano-scale era

--- No use of Operational amplifier --

- Comparator controlled current source
- Successive approximation ADC
- Sub-ranging ADC

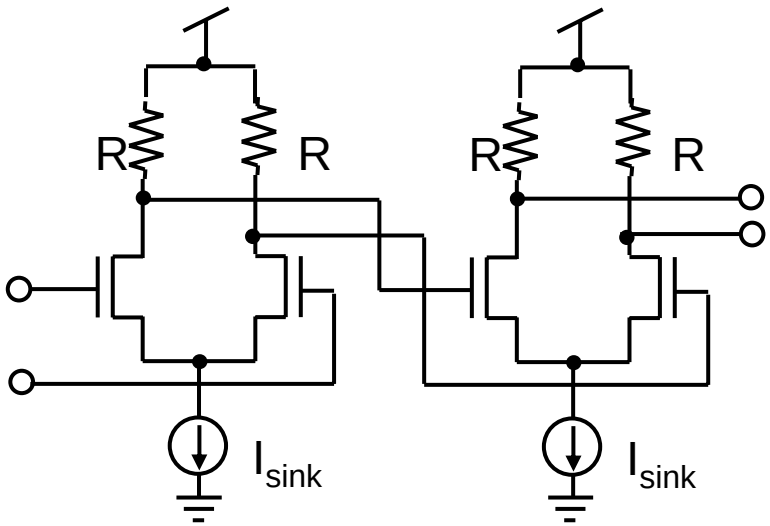
Design rule and Speed in Comparator

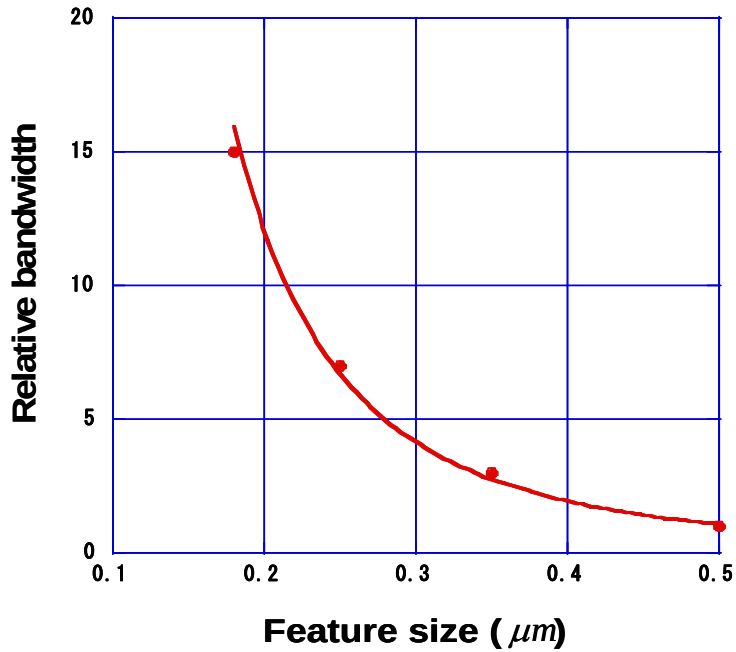
Gain bandwidth (=Speed) is inversely proportional to the L^2 (channel length).
Technology scaling is still effective to increase the comparator speed and to reduce operating current.
Furthermore, low voltage operation, such as 0.5V, is available.

$$GBW = \frac{g_m}{2\pi\left(WC_j + \frac{2}{3}C_{ox}LW\right)} = \frac{I_{sink}}{2\pi\left(WC_j + \frac{2}{3}C_{ox}LW\right)V_{eff}}$$

$$GBW = \frac{\mu V_{eff}}{2\pi L^2\left(\frac{2}{3} + \frac{C_j}{k}\right)}$$

$$I_{sink} = \frac{\mu C_{ox}}{2}\frac{W}{L}V_{eff}^2 \qquad C_{ox} = \frac{\kappa}{L}$$





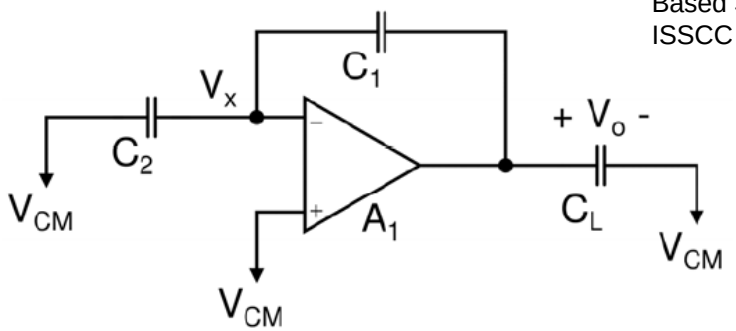
Comparator controlled current source

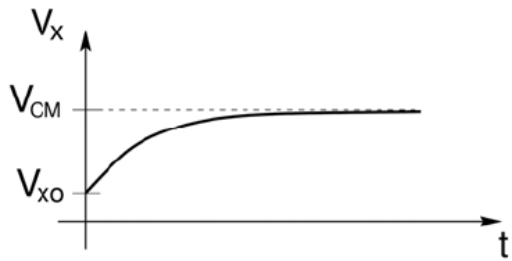
Comparator controlled current source can realize the virtual ground.

Now challenge for not use of OpAmp in ADC design has started.

Conventional OpAmp

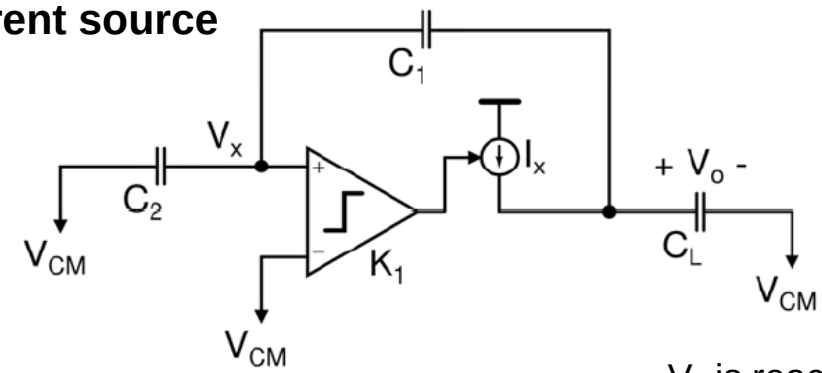
T. Sepke, J. K. Fiorenza, C. G. Sodini, P. Holloway, and H. Lee, "Comparator-Based Switched-Capacitor Circuits For Scaled CMOS Technologies," IEEE, ISSCC 2006, Dig. of Tech. Papers, pp. 574-575. Feb. 2006.

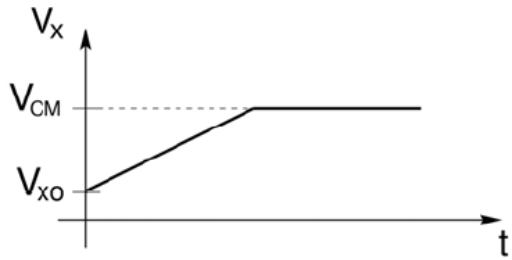




V_x is reaching the virtual ground voltage asymptotically

Comparator controlled current source

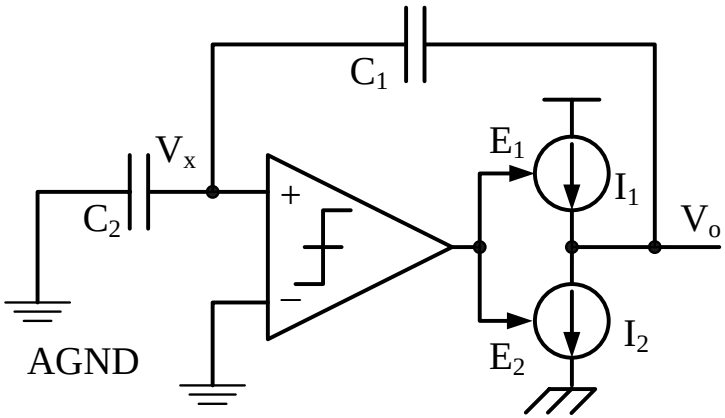




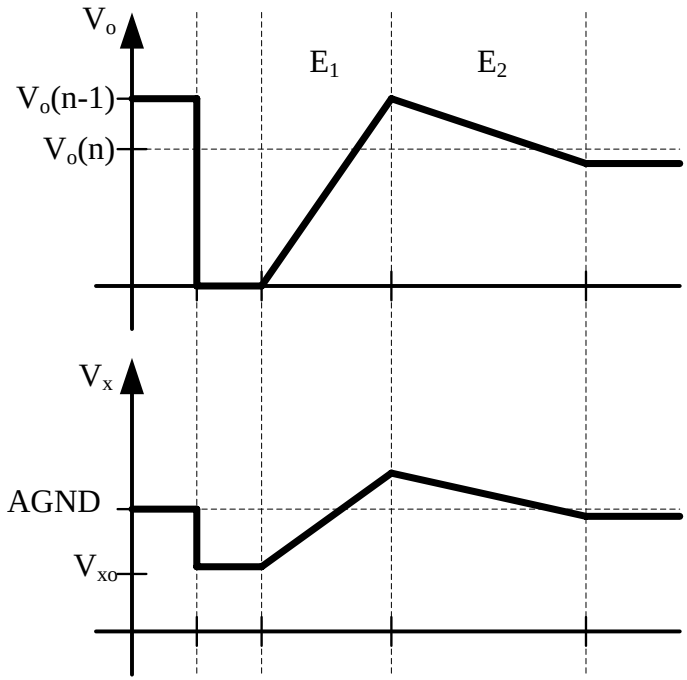
V_x is reaching the virtual ground voltage with constant rate

Realistic comparator controlled current source

Time delay (V_x → V_o) causes voltage offset. Small inverse current source has been introduced. The offset voltage can be reduced and does not effect the conversion linearity.



$I_2 << I_1$



T. Sepke, J. K. Fiorenza, C. G. Sodini, P. Holloway, and H. Lee, "Comparator-Based Switched-Capacitor Circuits For Scaled CMOS Technologies," IEEE, ISSCC 2006, Dig. of Tech. Papers, pp. 574-575. Feb. 2006.

10b, 8MHz ADC has been developed. Pd=2.5mW. Lowest Pd/MHz

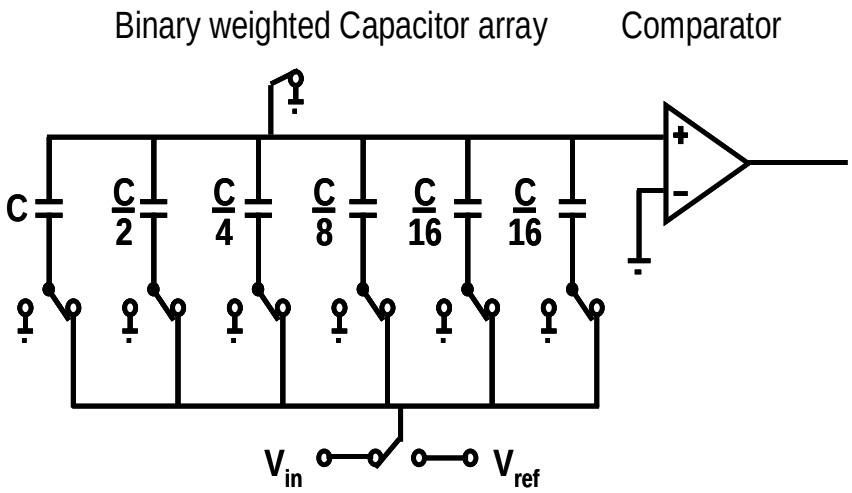
Successive approximation ADC

Successive approximation ADC has been used long time as a low power and low speed ADC. It doesn't require OpAmp but capacitor array and comparator. Thus this architecture looks suitable for scaled and low voltage CMOS.

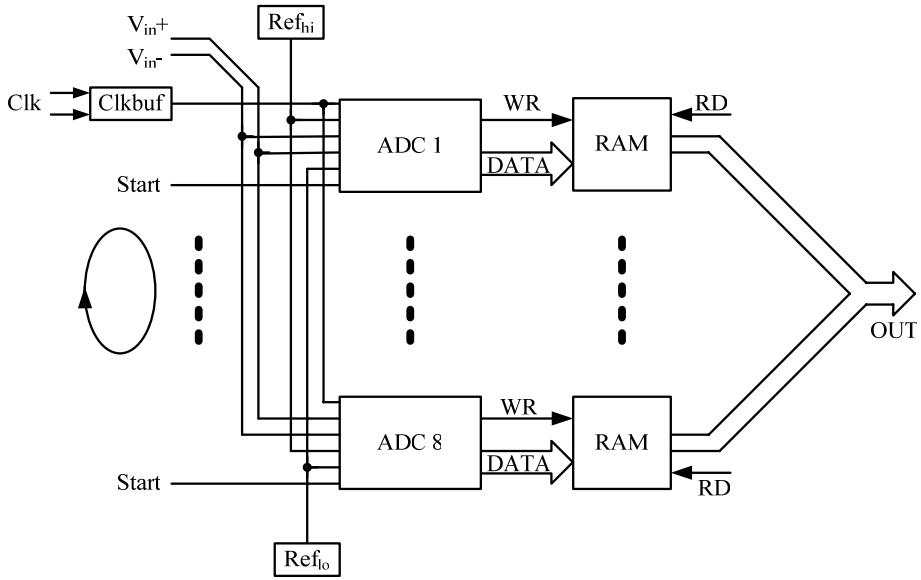
Now challenge for renewal of this conventional architecture has started.

Successive approximation ADC

SA-ADC



Eight interleaved SA-ADCs with 90nm CMOS attain 600MHz operation.

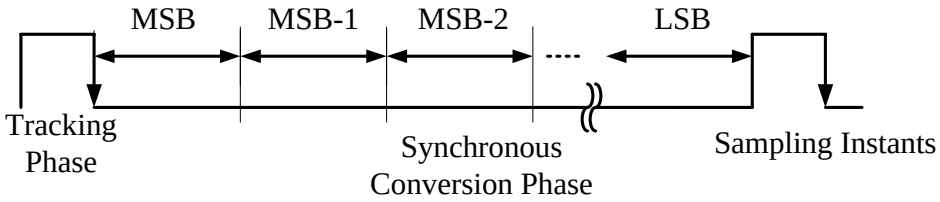


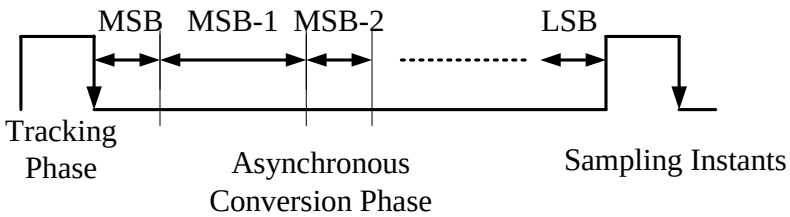
D. Draxelmayr, "A 6b 600MHz 10mW ADC Array in Digital 90nm CMOS," IEEE, ISSCC 2004, Dig. of Tech. Papers, pp. 264-265, Feb. 2004.

Improvement of SA-ADC

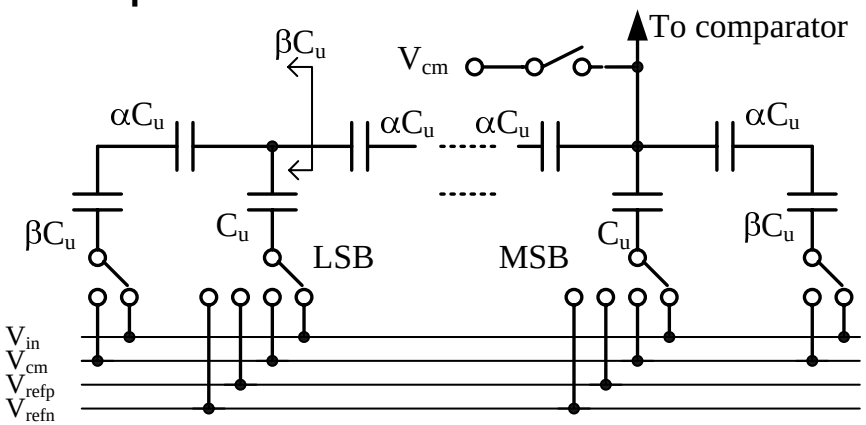
Asynchronous clock increases conversion frequency.
Use of proper radix reduces capacitance.

Asynchronous clock





Capacitor ladder with some radix number



6bit 600MHz 5.3mW ADC has been realized with 0.13um CMOS

$$\beta = 1 + \alpha \| \beta$$

$$radix = 1 + \frac{\beta}{\alpha}$$

S. W. M. Chen and R. W. Brodersen, "A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13um CMOS," IEEE, ISSCC 2006, Dig. of Tech. Papers, pp. 574-575. Feb. 2006.

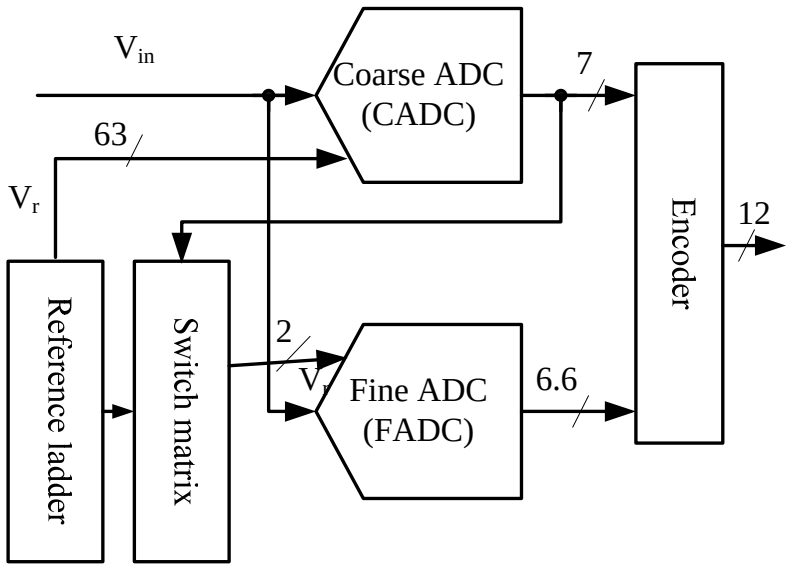
Sub-ranging ADC

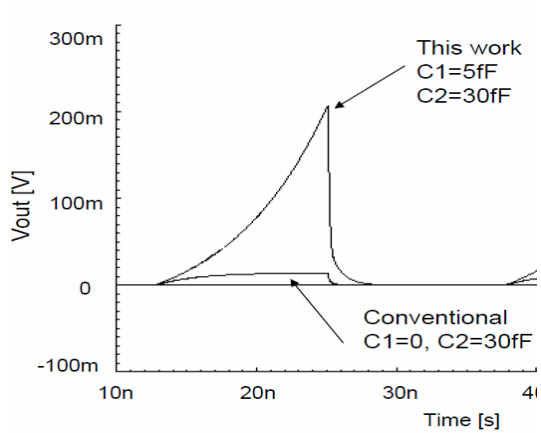
Sub-ranging ADC also doesn't require OpAmp and suitable for LV operation. However it requires low offset voltage comparators.

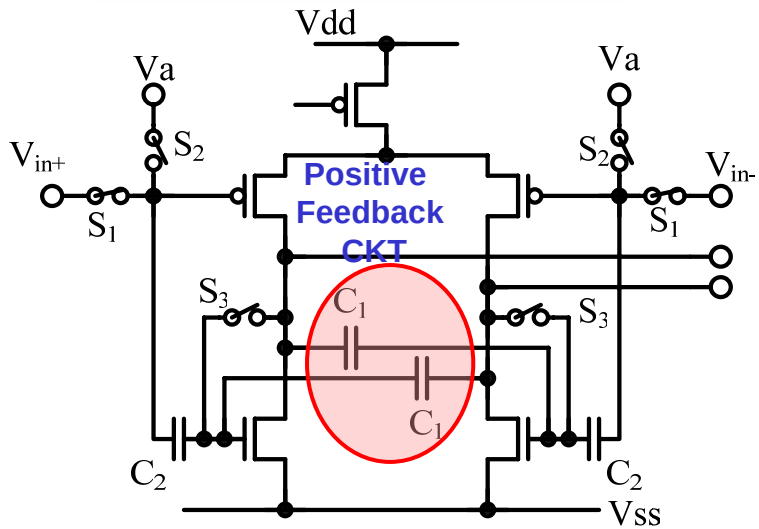
Use of positive feedback technique has realized low offset voltage.

Technology revival has been found.

Pd/MHz =0.75mW/MHz which is lowest value!!







7]Y. Shimizu, S. Murayama, K. Kudoh, H. Yatsuda, A. Ogawa, " A 30mw 12b 40MS/s Subranging ADC with a High-Gain Offset-Canceling Positive-Feedback Amplifier in 90nm Digital CMOS," IEEE, ISSCC 2006, Dig. of Tech. Papers, pp. 222-225. Feb. 2006.

Summary

- **Technology scaling is effective for increasing analog performance if not so much higher SNR is required.**
- **Technology scaling is not effective for increasing analog performance if higher SNR is required, and sometimes degrades it.**
- **Increase of signal capacitance to keep the SNR high at low voltage operation is essential serious issue for use of scaled CMOS.**
- **Furthermore, Gain lowering of OpAmp due to technology scaling and voltage lowering becomes serious issues.**
- **Design challenges for ADC has been started.**
- **No use of OpAmp is a common idea.**
- **Technology revivals have been found and the performance has been improved. Further improvement will be expected in future.**