# Direct Reference Feed-Forward Compensation for Fast Frequency Settling All-Digital Phase Locked Loops

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# Motivation

- Decreasing supply voltages make it increasingly difficult for analog circuits to work as they have in the past

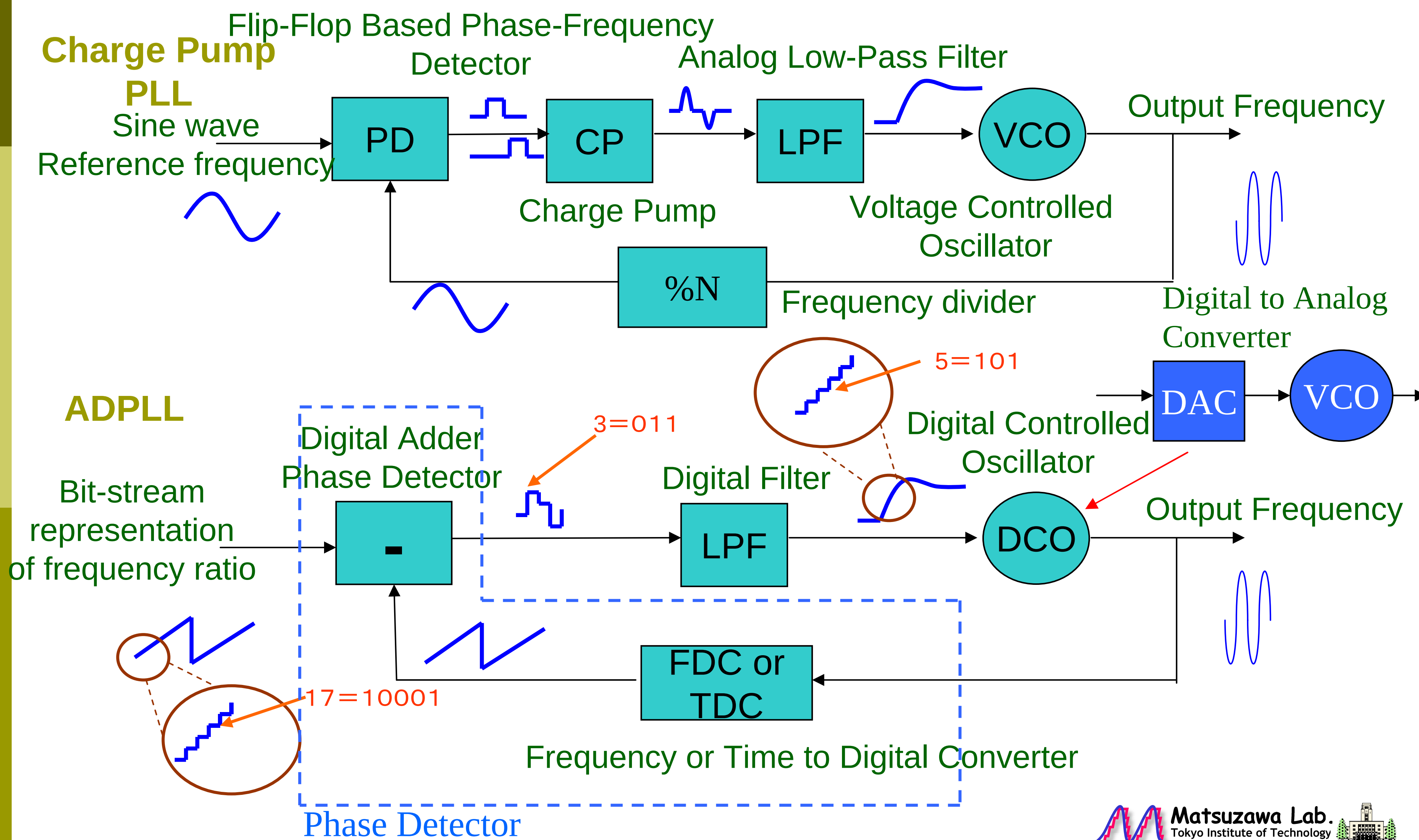
- All-Digital Phase-Locked Loop has recently been reduced to overcome the problem of low voltage for frequency synthesis

- Fast-frequency switching techniques are necessary for frequency hopping systems, or fast switching between frequency channels in future wireless systems

# Outline

- Comparison between traditional charge-pump and ADPLL
- Proposed feed-forward method
- Obtaining the feed-forward parameters
- Analysis
- Matlab simulation result
- Design Example and Verilog-AMS simulation
- Conclusion

# The Charge-Pumped based PLL VS All-Digital PLL

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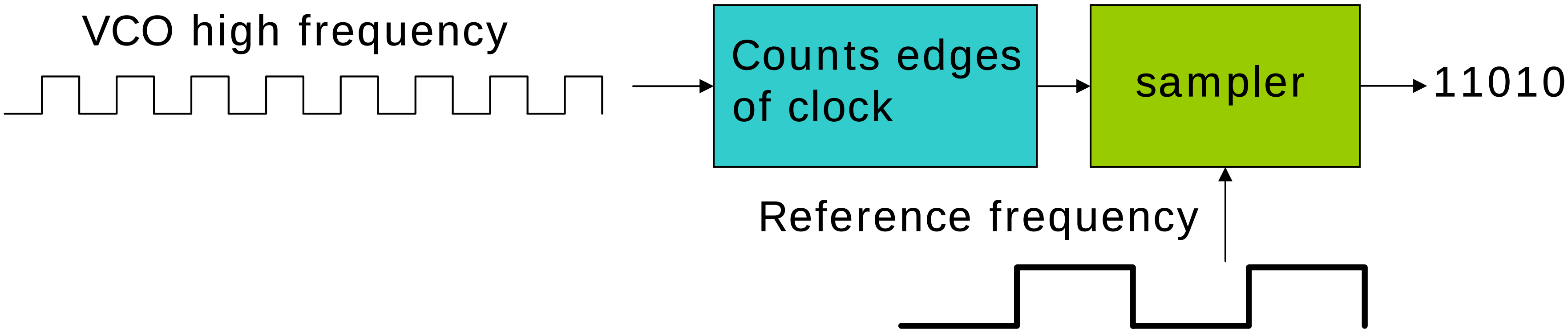
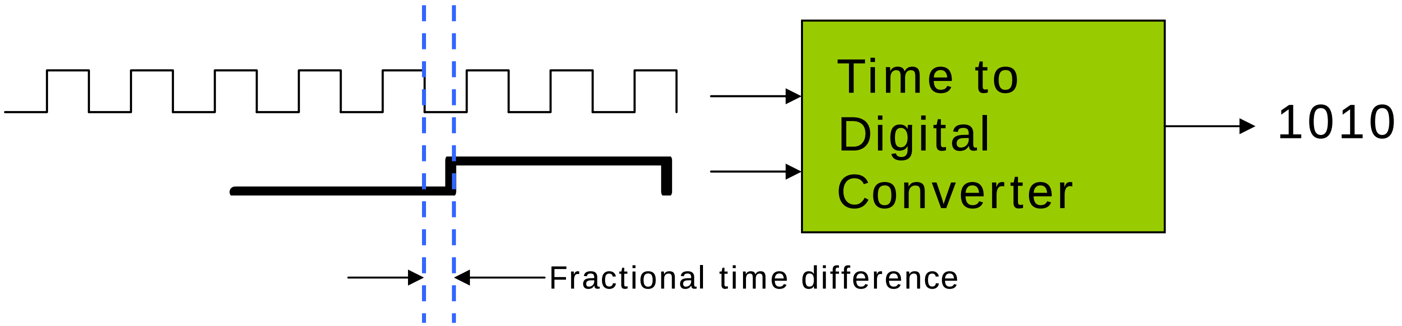
# TDC/FDC explanation

## Frequency Counter

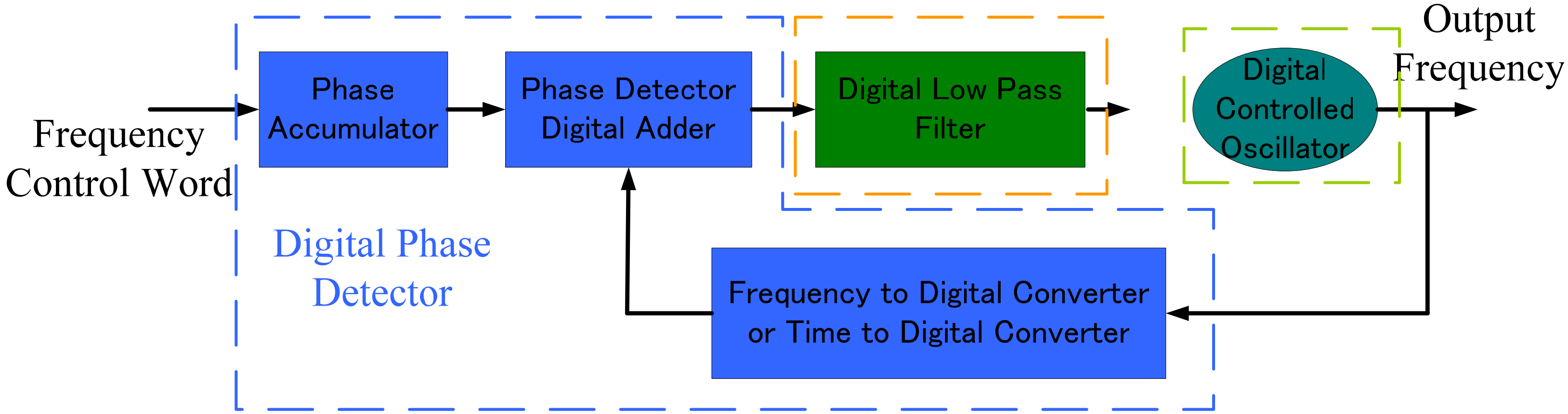



## Time to Digital converter

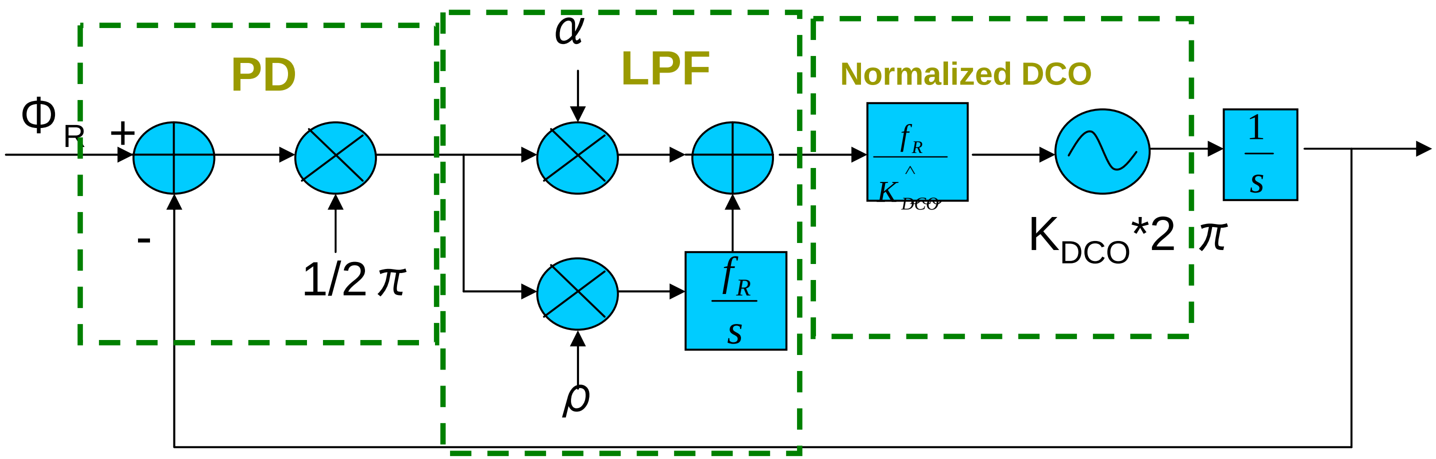


# All-Digital PLL Mathematical Model

## System Level Model of the ADPLL




## Continuous time approximation S-Domain model of the ADPLL





1. A. Kajiwara and M. Nakagawa, "A New PLL Frequency Synthesizer with High Switching Speed," IEEE Trans. Vehicular Technology, Vol. 41, pp. 407-413, Nov. 1992.
2. R. B. Staszewski and P. T. Balsar, "Phase-Domain All-Digital Phase-Locked Loop," IEEE Trans. Circuits and Systems II, Vol. 52, pp. 159-163, Mar. 2005.

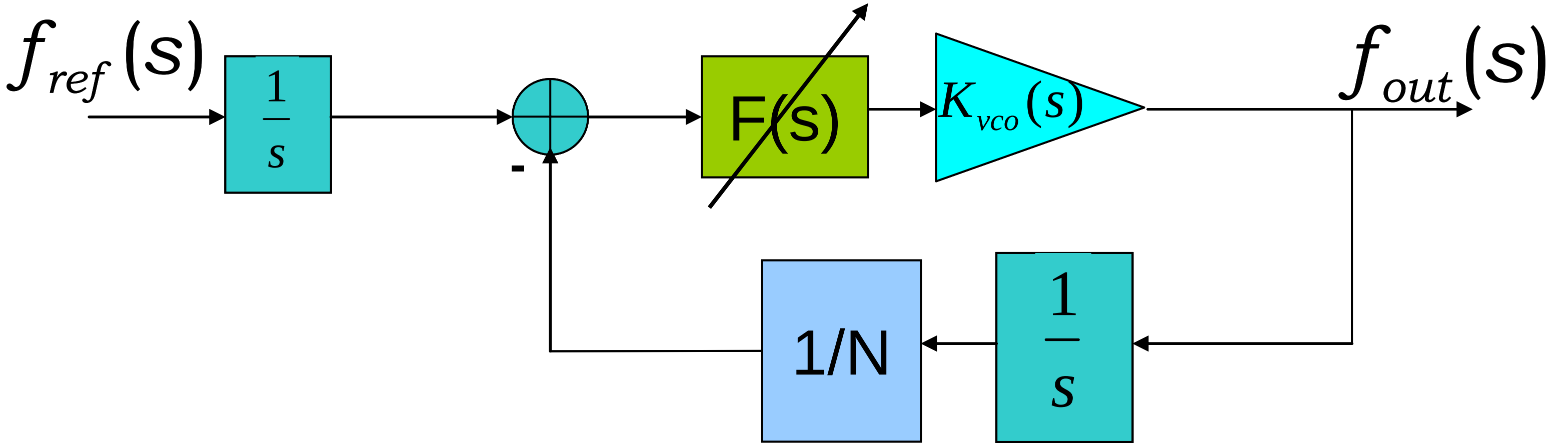
# Conventional PLL Speed-up Techniques

Loop parameter adjustment is most common

- Adjustment of loop filter's bandwidth
- Dynamic adjustment of loop gain by changing filter or charge-pump gain

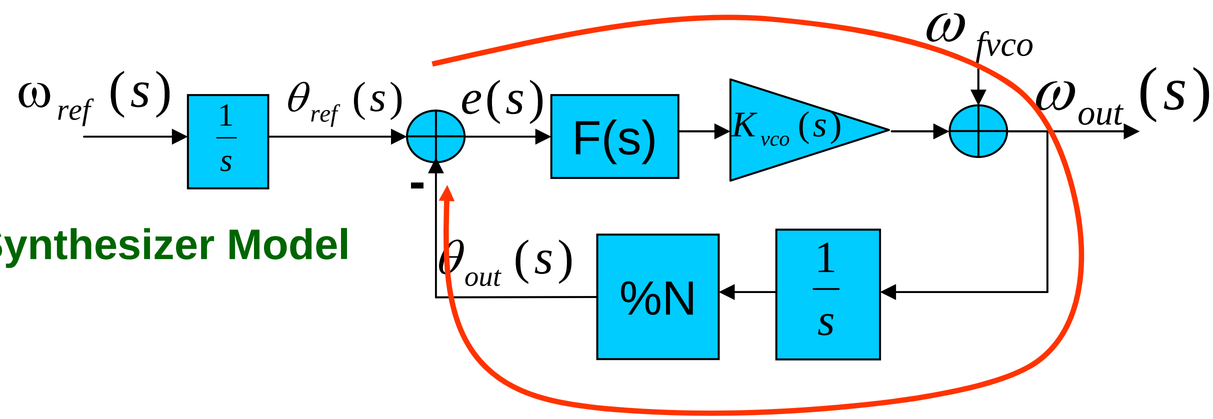
Disadvantage

- Loop stability maybe compromised
- Difficult to design, designer must make sure the system is stable over all combinations of loop parameters



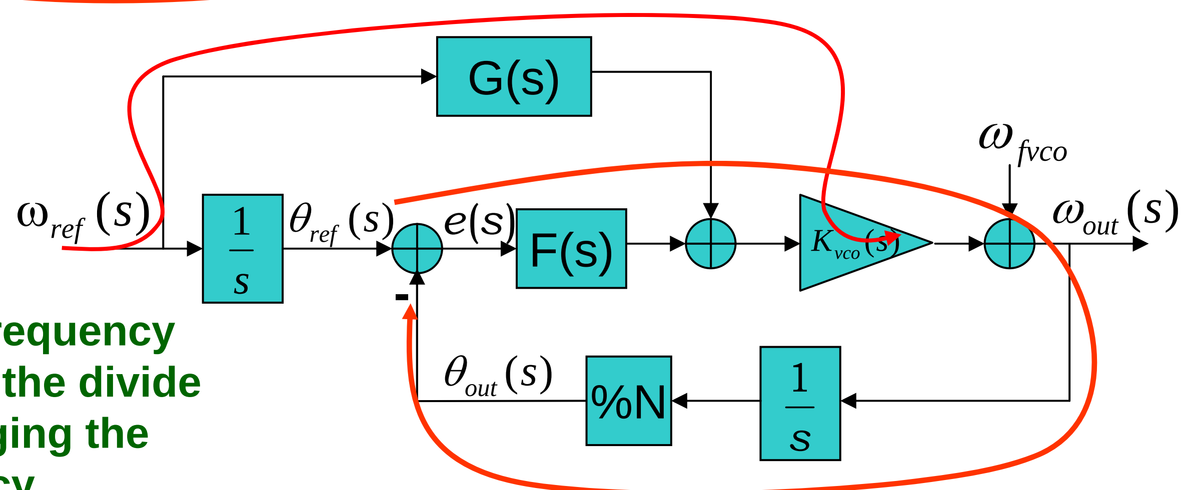
# Speeding up the PLL's Settling speed Via Feed-Forward

Speeding up the ADPLL's settling speed:




**Synthesizer Model**

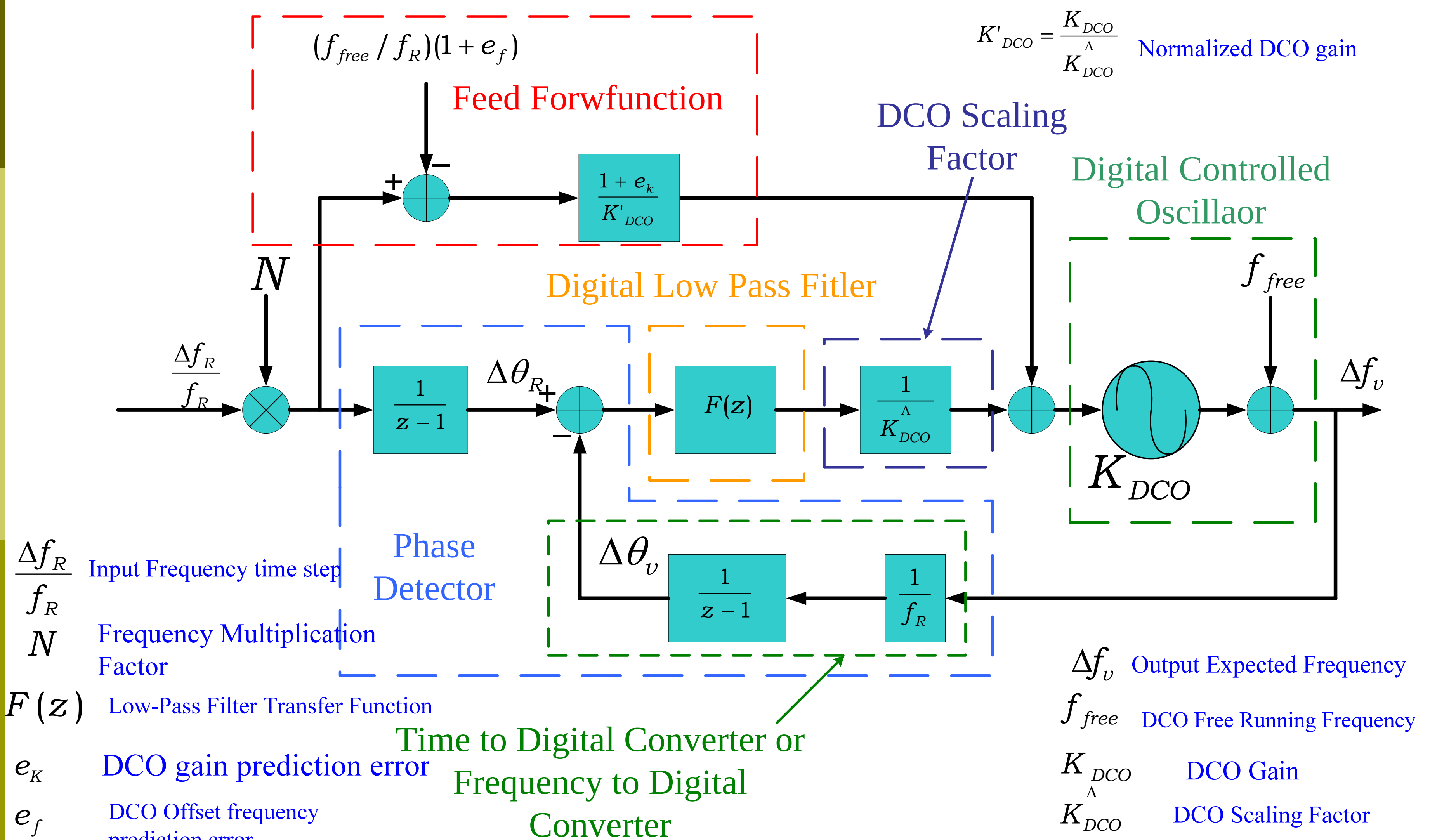
**Synthesizer Model with Feed-Forward Path**




**Assume that the frequency is changed not by the divide ratio, but by changing the reference frequency.**

*Other PLL Feed-Forward Papers:*
*Benyong Zhung und Phillip Allen*、FEED-FORWARD COMPENSATED HIGH SWITCHING SPEED DIGITAL PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER、1999

# Direct Frequency Reference Feed-Forwarding

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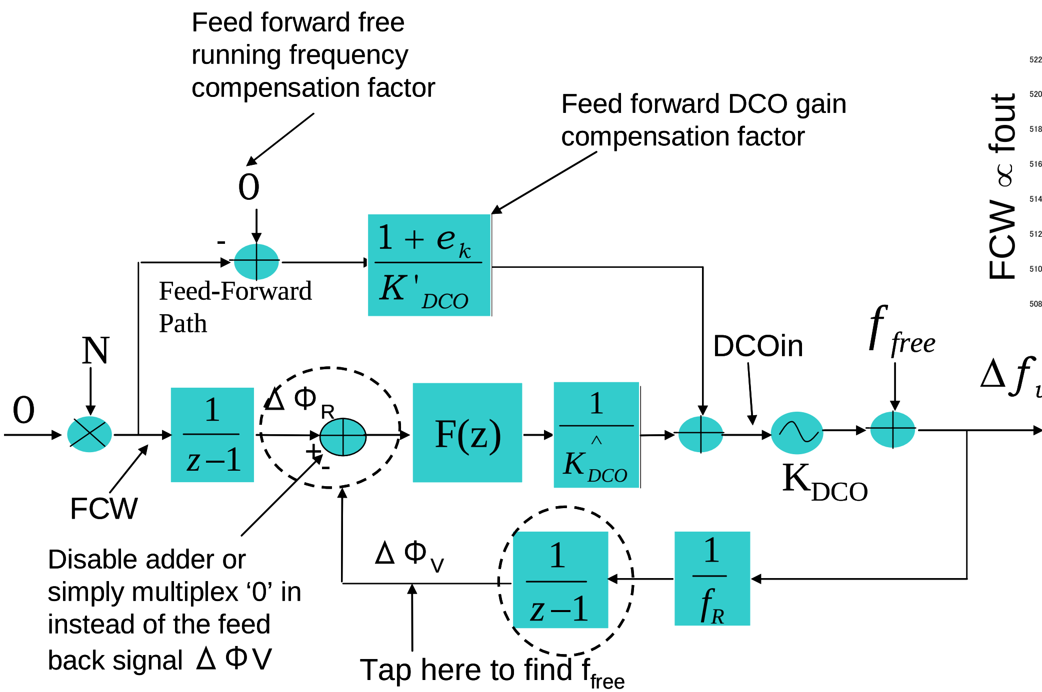
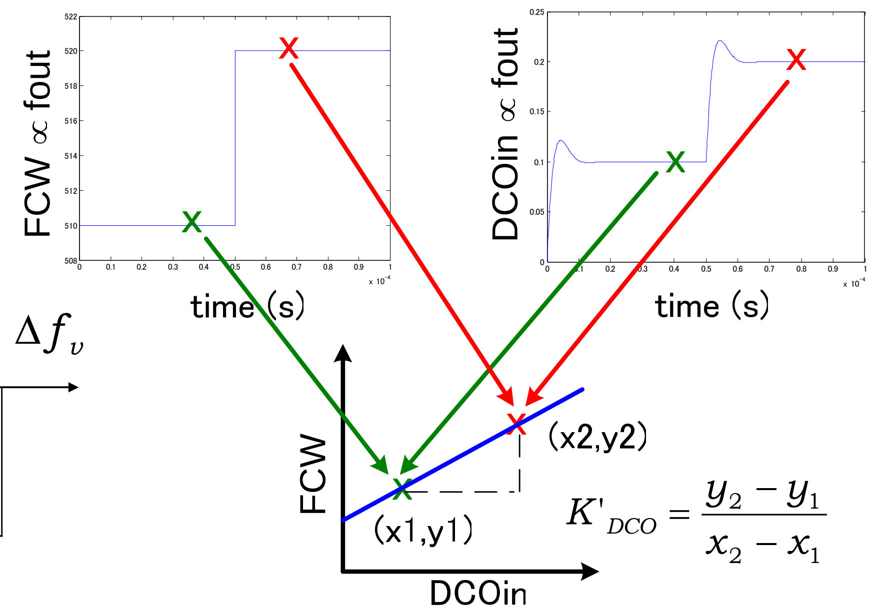
# Finding the Feed-Forward Parameters

## Finding the free running frequency




## Finding the DCO gain




[4]


[4] R. B. Staszewski, Dirk Leipold, and Poras T. Balasara "Just-In-Time Gain Estimation of an RF Digitally-Controlled Oscillator for Digital Direct Frequency Modulation," IEEE Trans. Circuits and Systems II, Vol. 50, No.11, pp. 887-892, Nov. 2003

# Perfect and Imperfect Reference Frequency Step Compensation

The output of the ADPLL without the feed-forward path

$$\Delta f_v = \frac{(N \cdot F(z) \cdot K'_{DCO})}{f_R \cdot (z-1) + F(z) \cdot K'_{DCO}} \cdot \frac{\Delta f_R}{f_R} + \frac{f_{free} \cdot (z-1) \cdot f_R}{f_R \cdot (z-1) + F(z) \cdot K'_{DCO}}$$

With ideal Feed-Forward Path

$$\Delta f_v = N \cdot f_R \cdot \frac{\Delta f_R}{f_R}$$

With realistic Feed-Forward Path

$$\Delta f_v = \frac{\Delta f_R}{f_R} \cdot N \cdot f_R + \frac{\Delta f_R}{f_R} \cdot N \cdot f_R \frac{e_k \cdot (z-1) \cdot f_R}{(z-1) \cdot f_R + F(z) \cdot K'_{DCO}} - \frac{(e_k + e_f + e_f \cdot e_k) \cdot (z-1) \cdot f_R}{(z-1) \cdot f_R + F(z) \cdot K'_{DCO}} f_{free}$$

$\Delta f_v$ Output Expected Frequency

$N$ Frequency Multiplication Factor

$\frac{\Delta f_R}{f_R}$ Input Frequency time step

$F(z)$ Low-Pass Filter Transfer Function

$f_{free}$ DCO Free Running Frequency

$e_K$ DCO gain prediction error

$K'_{DCO} = \frac{K_{DCO}}{\hat{K}_{DCO}}$ Output Expected Frequency

$K_{DCO}$ DCO Gain

$\hat{K}_{DCO}$ DCO Scaling Factor

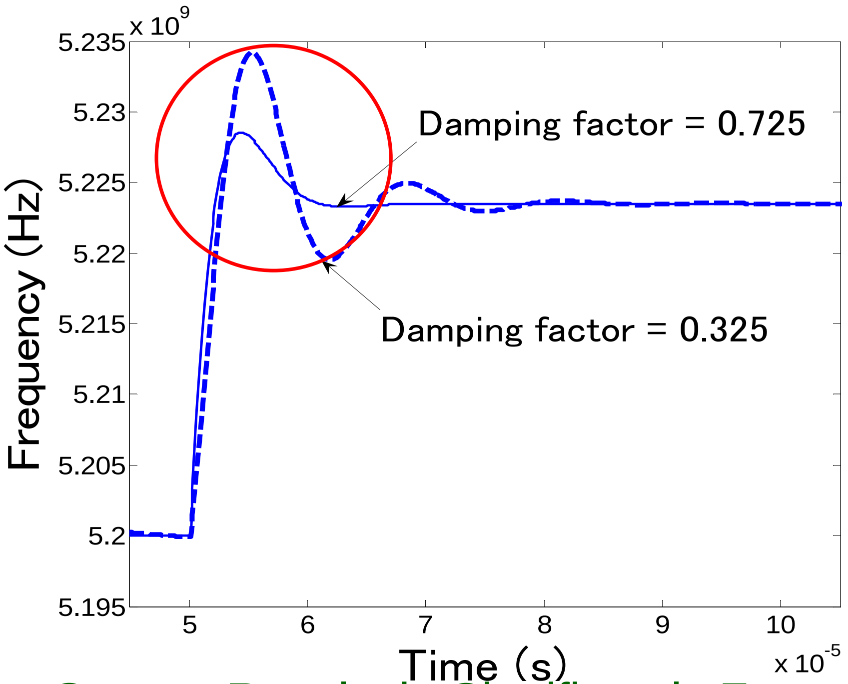
$f_R$ Reference Frequency

$e_f$ DCO Offset frequency prediction error

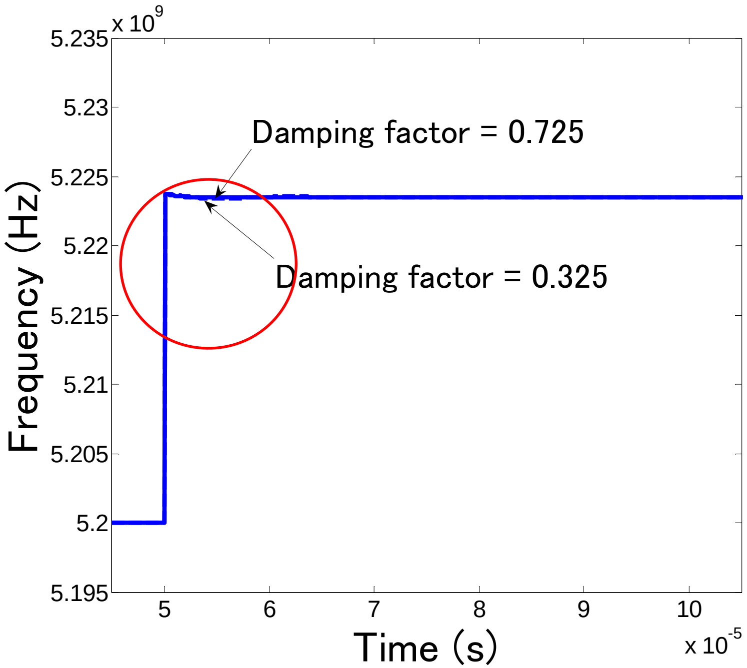
Win Chaivipas, Philipus Oh, and Akira Matsuzawa "Feed-Forward Compensation Technique for All Digital Phase Locked Loop Based Synthesizers" Proc. ISCAS 06

# Simulation Results 1

ADPLL with no Feed-Forward

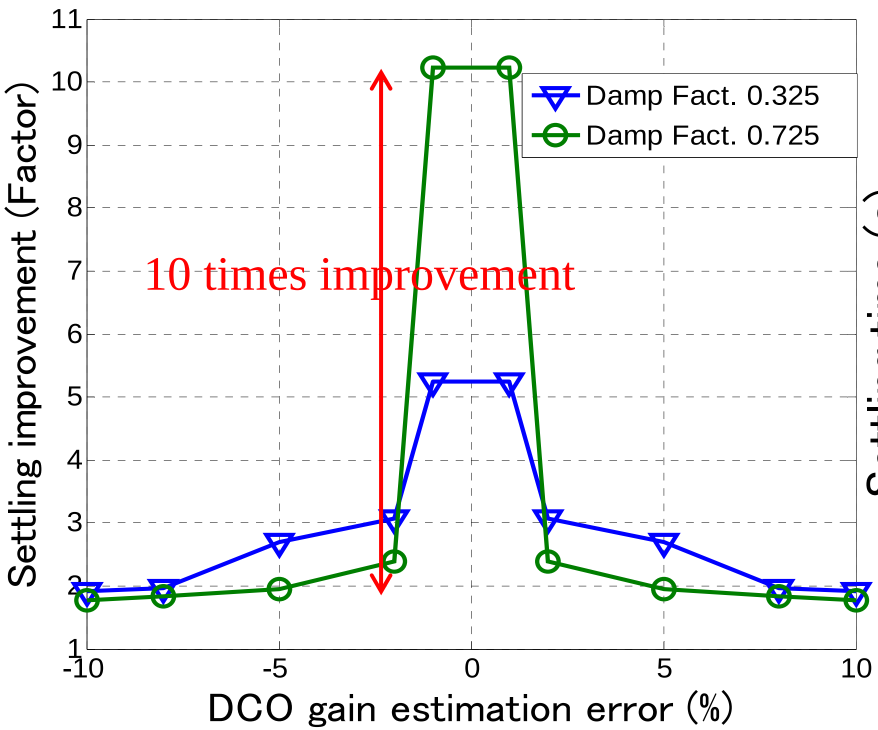



ADPLL with Feed-Forward

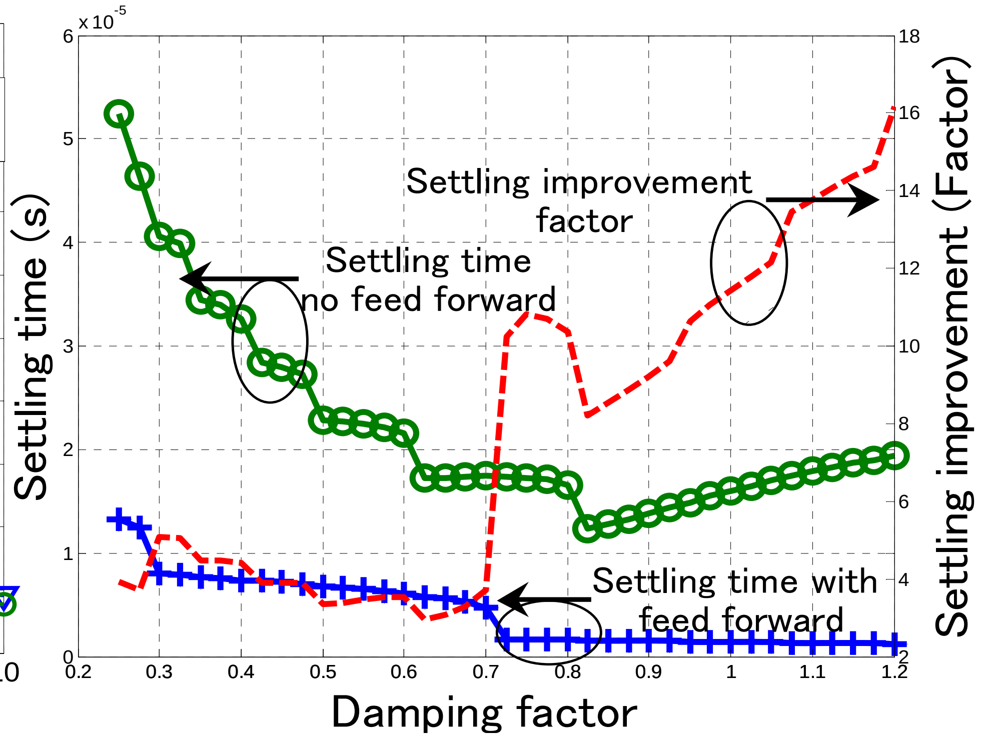



- System Results in Significantly Faster Settling
- Overshoot becomes less dependent on damping factor and is almost eliminated for good DCO gain prediction

# Simulation Results 2




All Digital Phase-Locked Loop Settling time improvement VS DCO gain estimation error




All Digital Phase-Locked Loop Settling time and improvement factor VS damping factor at 1% DCO gain prediction error

# Feed-forward does not affect stability

Assuming an arbitrary filter function

$$F(z) = K\frac{\prod_{i=1}^{m}(z-Z_i)}{\prod_{j=1}^{n}(z-P_j)} = \frac{K\cdot(z-Z_1)\cdot(z-Z_2)\cdots(z-Z_m)}{(z-P_1)\cdot(z-P_2)\cdots(z-P_n)}$$

Substituting into the transfer function for ADPLL system with and without feed-forward

System without feed-forward

$$\Delta f_v = \frac{(N\cdot K\cdot \prod_{i=1}^{m}(z-Z_i)\cdot K'_{DCO})}{f_R\cdot(z-1)\cdot\prod_{j=1}^{n}(z-P_j)+K\cdot\prod_{i=1}^{m}(z-Z_i)\cdot K'_{DCO}}\cdot\frac{\Delta f_R}{f_R}$$

System with feed-forward

$$\Delta f_v = \frac{\Delta f_R}{f_R}\cdot N\cdot f_R\,\frac{(e_k+1)\cdot(z-1)\cdot f_R\cdot\prod_{j=1}^{n}(z-P_j)+K\cdot\prod_{i=1}^{m}(z-Z_i)\cdot K'_{DCO}}{(z-1)\cdot f_R\cdot\prod_{j=1}^{n}(z-P_j)+K\cdot\prod_{i=1}^{m}(z-Z_i)\cdot K'_{DCO}}$$

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# Example Second Order System

Let the loop filter transfer function be

$$F(z) = \frac{\alpha(z-1)+\rho}{z-1}$$

Poles and Zeros of System without feed-forward

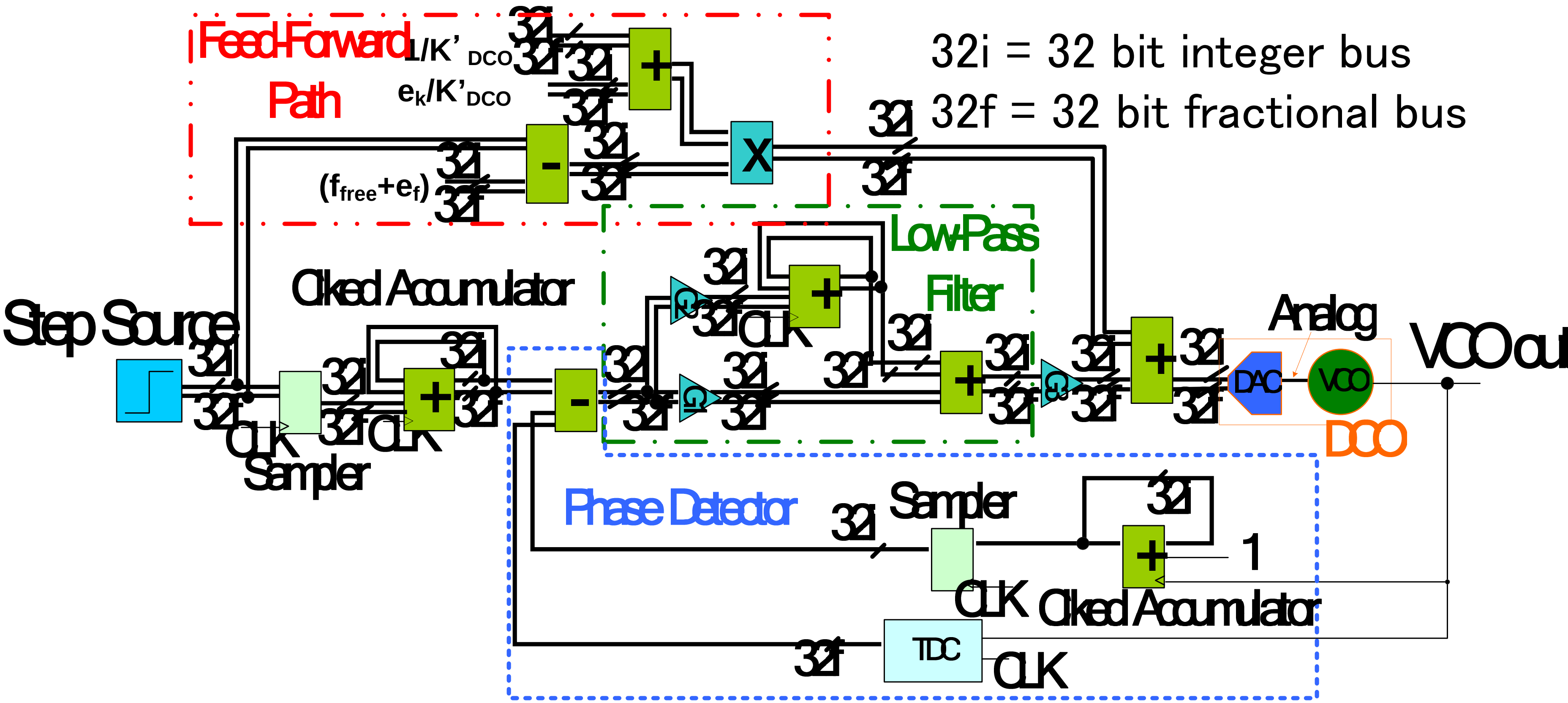
$$Z_1 = \frac{\rho-\alpha}{\alpha} \qquad P_{1,2} = -\frac{1}{2}\cdot\frac{1}{f_R}\cdot K'_{DCO}\cdot\alpha - 2\cdot f_R \pm \sqrt{K'_{DCO}{}^2\cdot\alpha^2 - 4\cdot f_R\cdot K'_{DCO}\cdot\rho}$$

Poles and Zeros of System with feed-forward

$$P_{FF1,2} = -\frac{1}{2}\cdot\frac{1}{f_R}\cdot K'_{DCO}\cdot\alpha - 2\cdot f_R \pm \sqrt{K'_{DCO}{}^2\cdot\alpha^2 - 4\cdot f_R\cdot K'_{DCO}\cdot\rho}$$

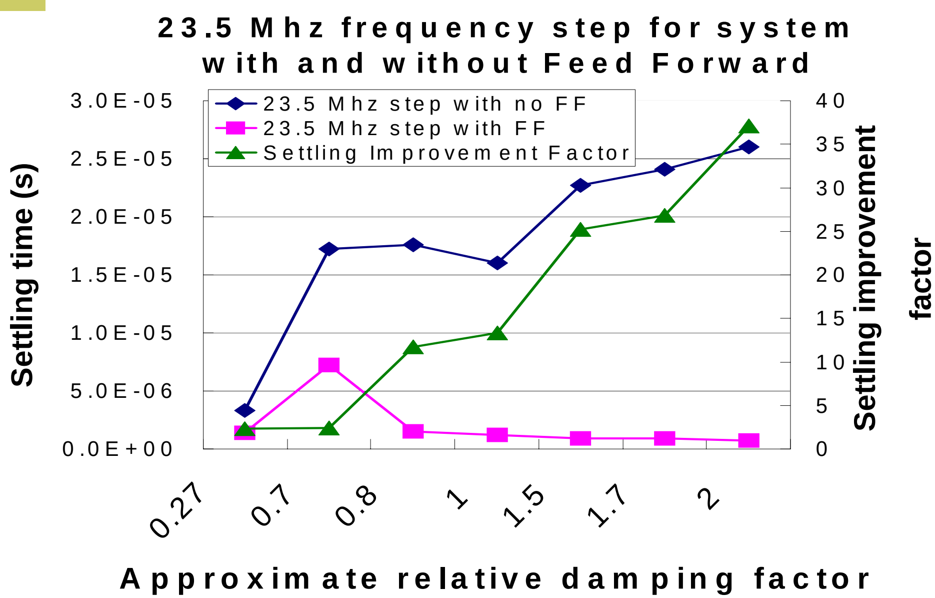
$$Z_{FF1} = -\frac{1}{2}\cdot\frac{1}{f_R(e_k+1)}\cdot[K'_{DCO}\cdot\alpha - 2\cdot f_R(1+e_k) \pm \sqrt{K'_{DCO}{}^2\cdot\alpha^2 - 4\cdot f_R\cdot K'_{DCO}\cdot\rho(e_k+1)}]$$

# Verilog-AMS Model

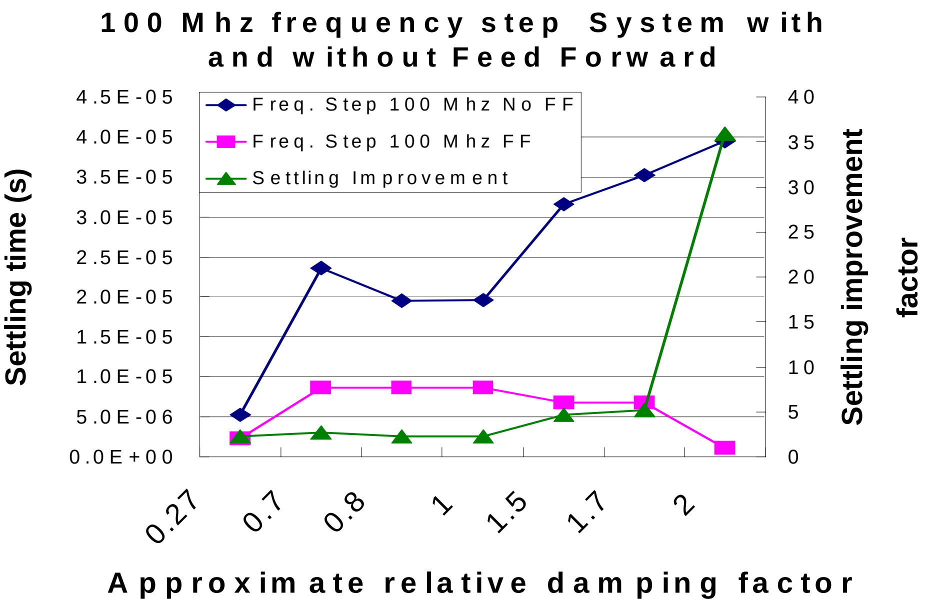


# Simulation Results

## 23.5MHz Frequency Step




## 100 MHz Frequency Step




Settling Speed improve with stability!

# Advantages and Challenges of Feed-Forward Compensation

**Advantages**

- Feed-Forward Compensation does not affect the System's stability as it does not modify the loop's bandwidth or change loop parameters.
- Offset introduced into the system will be compensated for, even if the prediction is bad it does not affect system stability, it only affects settling time
- Feed-Forward can eliminate the system's overshoot's dependence on damping factor for a reasonable DCO gain estimation
- Feed-Forward compensation's settling improvement factor increases with damping factor means faster settling improvement and stability can be improved simultaneously

**Challenges**

- The actual possible improvement factor is still unknown until a real prototype is designed
- Possibility to extend the feed-forward function from static to dynamic for increased settling improvement is possible, with the possible trade-off of the need for careful design as the stability may be compromised

# Questions?