All Digital Phase-Locked Loops, its Advantages and Performance Limitations

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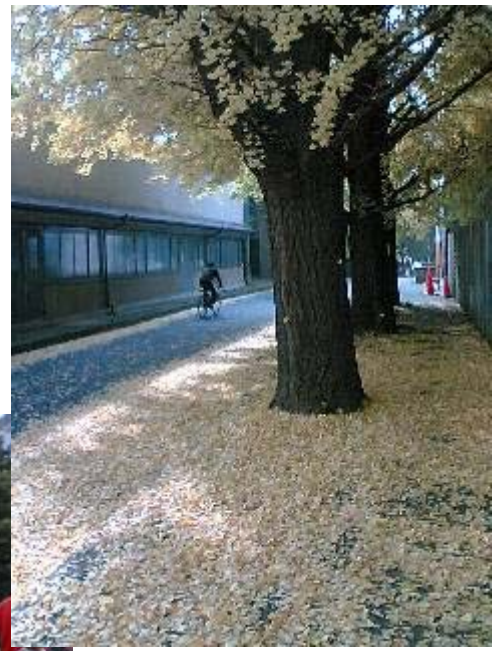
Located about 20 min from central Tokyo, Tokyo Institute of Technology is home to approximately 10,000 students, of which about 10% are international students



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松澤研究室
Matsuzawa Laboratory

Lab is new, only 2 ½ years old
As of this year Matsuzawa Lab's International student to Japanese student's ratio will be 1:1

Our main research is in Mixed-Signal Analog and RF IC design and low-Power. Two main themes concern data converters, and RF components. A project concerning low analog circuit for biomedical application is also in progress.

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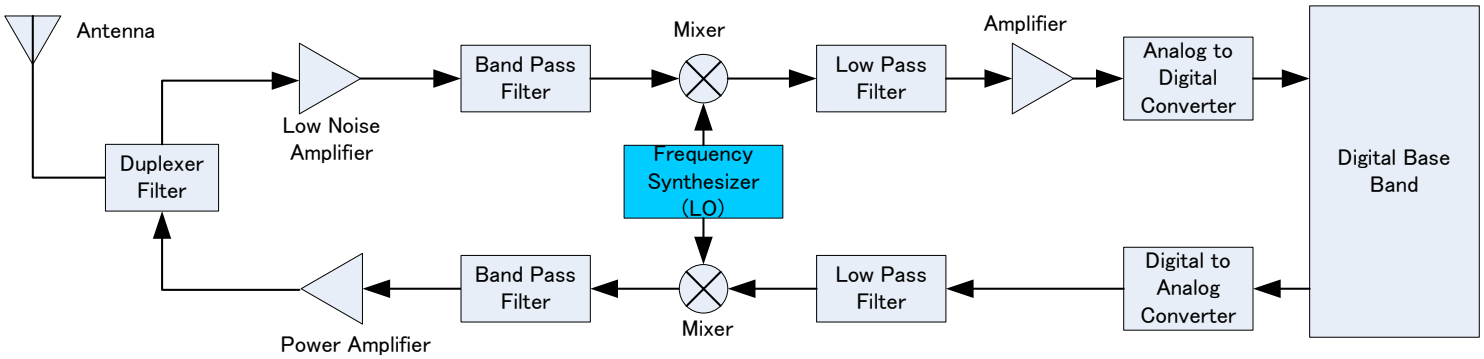
Phase-Locked Loops (PLL) and Frequency Synthesizers

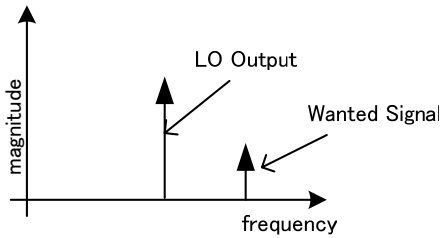
A Generic Transceiver

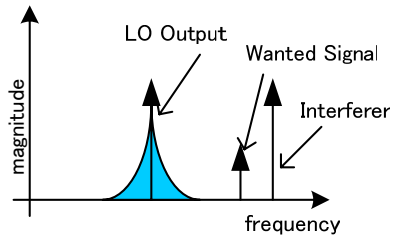


Ideal condition

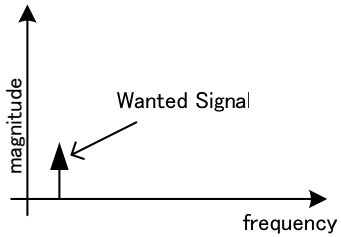
Effect of Phase Noise

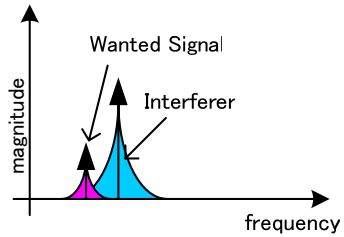
Before down conversion





After down conversion





Behzad Razavi, “RF Microelectronics”, Prentice Hall 1998

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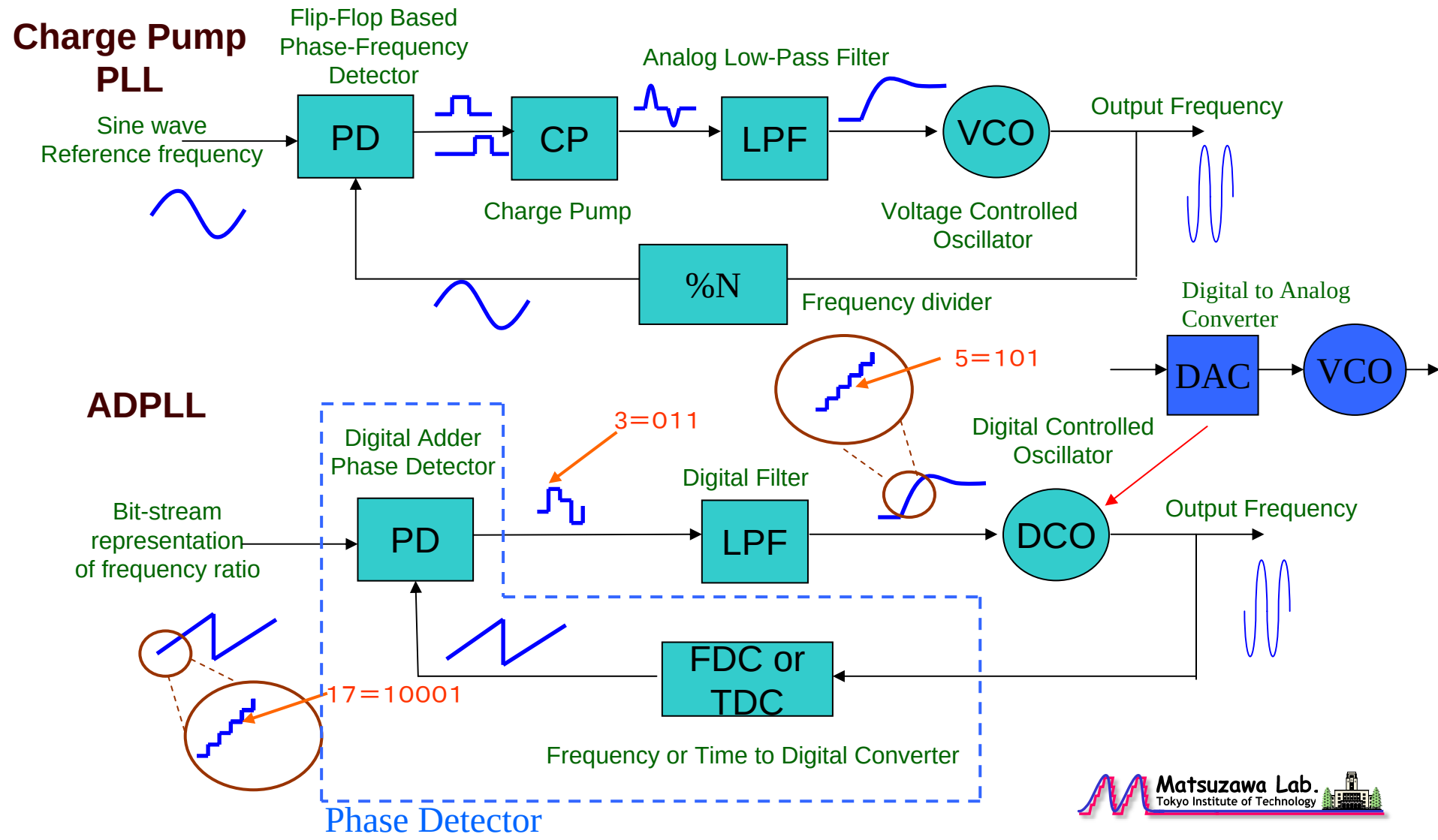
The Charge-Pumped based PLL VS All-Digital PLL



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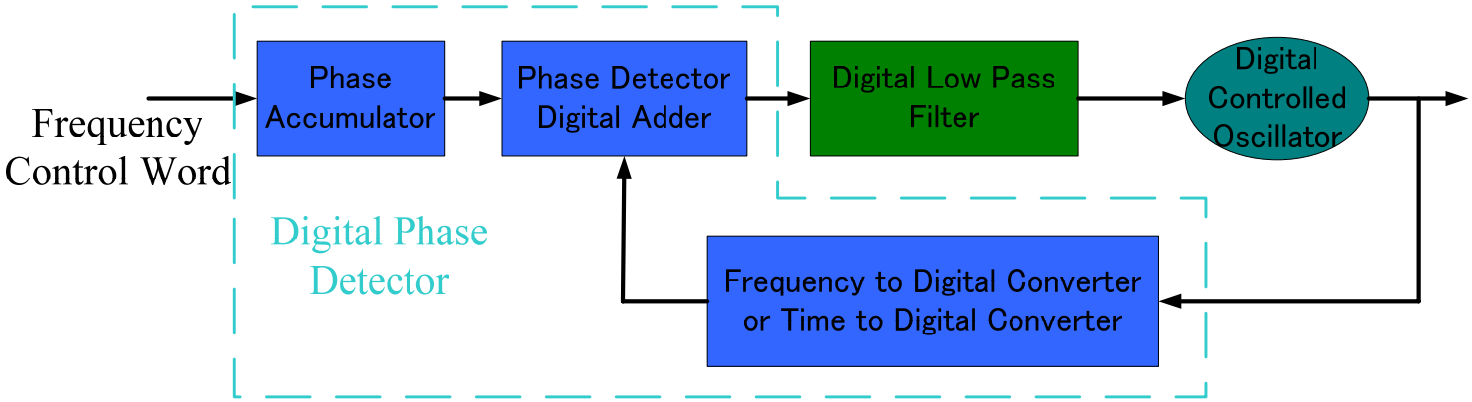
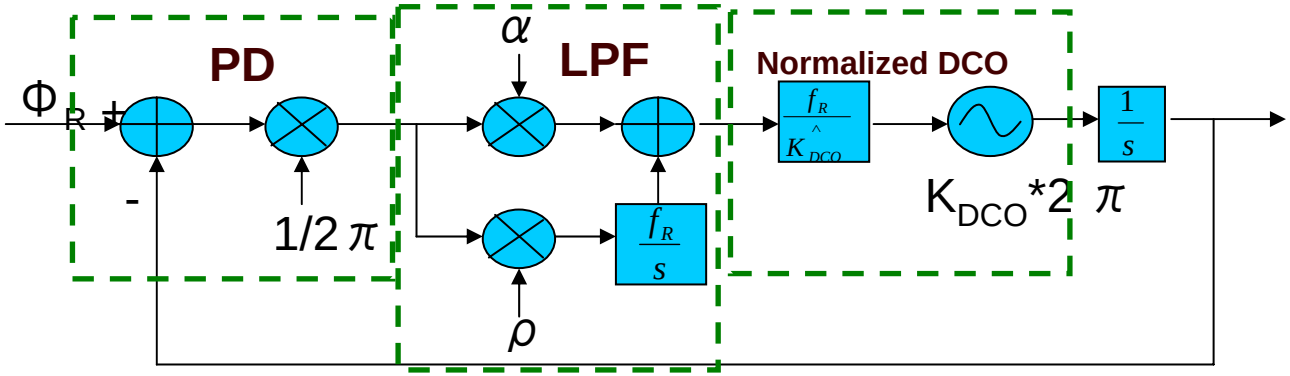
All-Digital PLL Mathematical Model

System Level Model of the ADPLL



Continuous time approximation S-Domain model of the ADPLL



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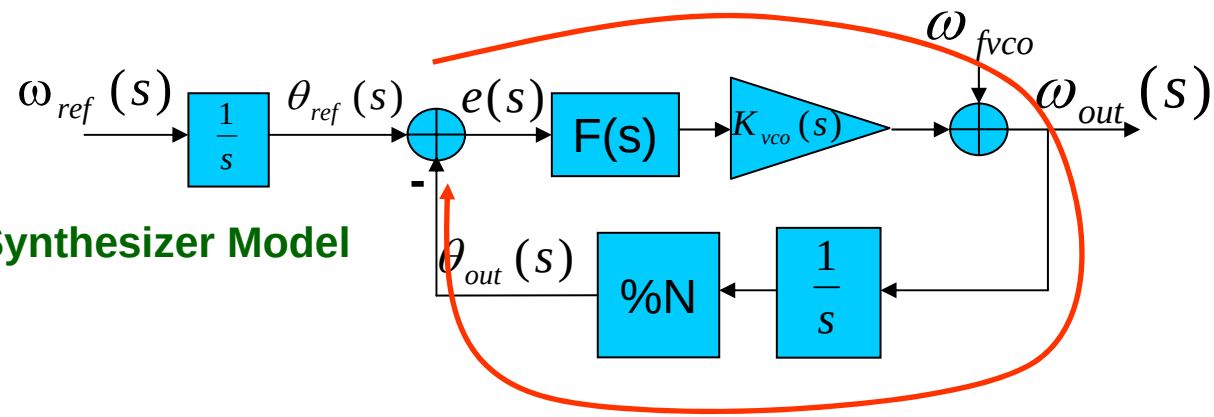
1. A. Kajiwara and M. Nakagawa, "A New PLL Frequency Synthesizer with High Switching Speed," IEEE Trans. Vehicular Technology, Vol. 41, pp. 407-413, Nov. 1992.
2. R. B. Staszewski and P. T. Balsar, "Phase-Domain All-Digital Phase-Locked Loop," IEEE Trans. Circuits and Systems II, Vol. 52, pp. 159-163, Mar. 2005.

Advantages of the All Digital PLL

- Access to intermediate signals in a digital form are significant
- Dynamic loop bandwidth adjustment can be made on the fly
- Direct frequency modulation is possible as has been shown
- Dynamic tracking of system performance is possible

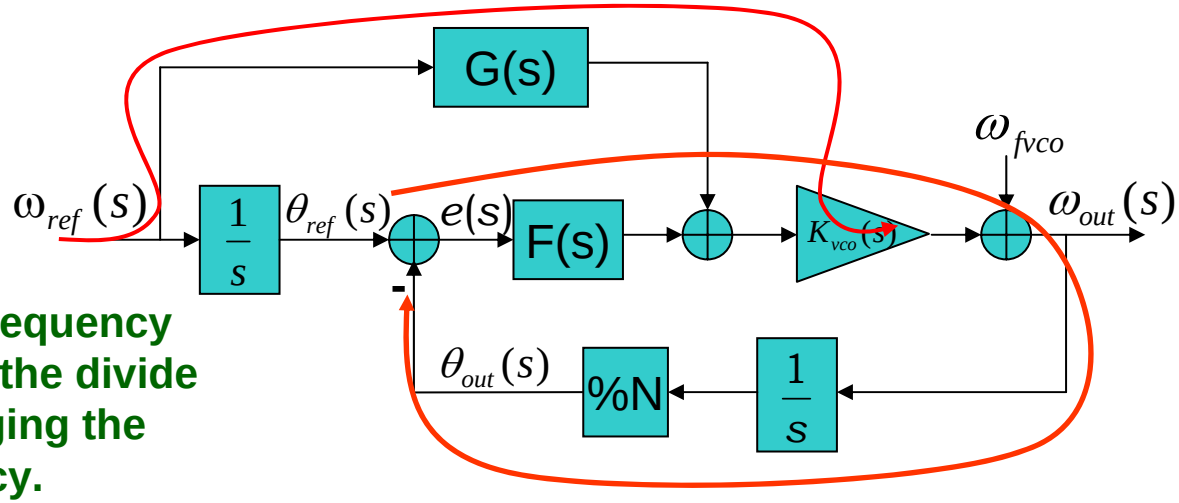
Speeding up the PLL's Settling speed Via Feed-Forward

Speeding up the ADPLL's settling speed:



Synthesizer Model

Synthesizer Model with Feed-Forward Path



Assume that the frequency is changed not by the divide ratio, but by changing the reference frequency.

Other PLL Feed-Forward Papers:
Benyong Zhung und Phillip Allen、FEED-FORWARD COMPENSATED HIGH SWITCHING SPEED DIGITAL PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER、1999

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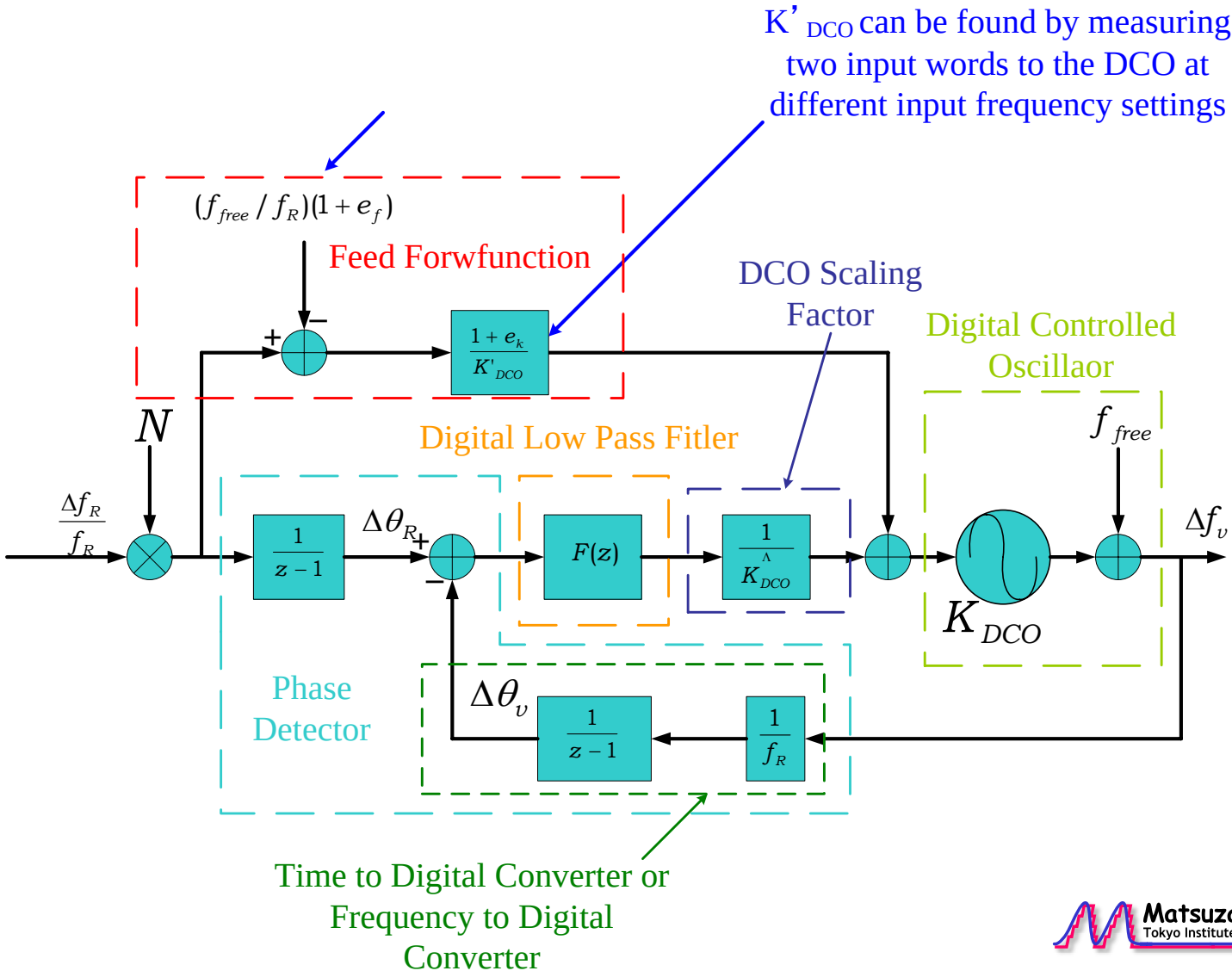
Direct Frequency Reference Feed-Forwarding



Perfect and Imperfect Reference Frequency Step Compensation

The output of the ADPLL without the feed-forward path can be shown to be related to the input by the following equation

$$\Delta f_v = \frac{(N \cdot F(z) \cdot K'_{DCO})}{f_R \cdot (z-1) + F(z) \cdot K'_{DCO}} \cdot \frac{\Delta f_R}{f_R} + \frac{f_{free} \cdot (z-1) \cdot f_R}{f_R \cdot (z-1) + F(z) \cdot K'_{DCO}}$$

With the Feed-Forward Path and setting the DCO scaling factor to the reference frequency fR and complete compensation by exact prediction of DCO gain and offset

$$\Delta f_v = N \cdot f_R \cdot \frac{\Delta f_R}{f_R}$$

In reality however, this is not possible due to the finite precision of the digital circuitry, and error in gain prediction. With prediction and precision error, the system's response then becomes

$$\Delta f_v = \frac{\Delta f_R}{f_R} \cdot N \cdot f_R + \frac{\Delta f_R}{f_R} \cdot N \cdot f_R \frac{e_k \cdot (z-1) \cdot f_R}{(z-1) \cdot f_R + F(z) \cdot K'_{DCO}} - \frac{(e_k + e_f + e_f \cdot e_k) \cdot (z-1) \cdot f_R}{(z-1) \cdot f_R + F(z) \cdot K'_{DCO}} f_{free}$$

Δf_v Output Expected Frequency

N Frequency Multiplication Factor

$\frac{\Delta f_R}{f_R}$ Input Frequency time step

$F(z)$ Low-Pass Filter Transfer Function

f_{free} DCO Free Running Frequency

e_K DCO gain prediction error

$K'_{DCO} = \frac{K_{DCO}}{\hat{K}_{DCO}}$ Output Expected Frequency

K_{DCO} DCO Gain

$\hat{K}_{DCO}$ DCO Scaling Factor

f_R Reference Frequency

e_f DCO Offset frequency prediction error

Win Chaivipas, Philipus Oh, and Akira Matsuzawa "Feed-Forward Compensation Technique for All Digital Phase Locked Loop Based Synthesizers" Proc. ISCAS 06

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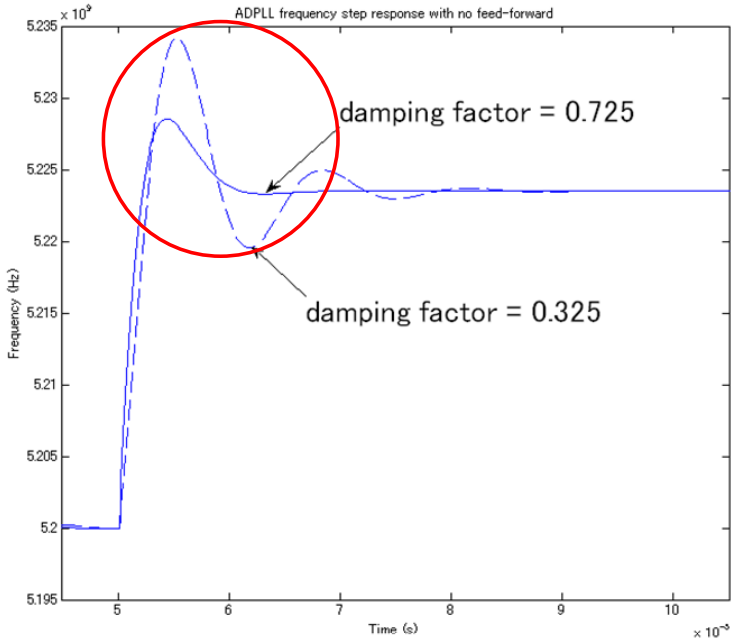
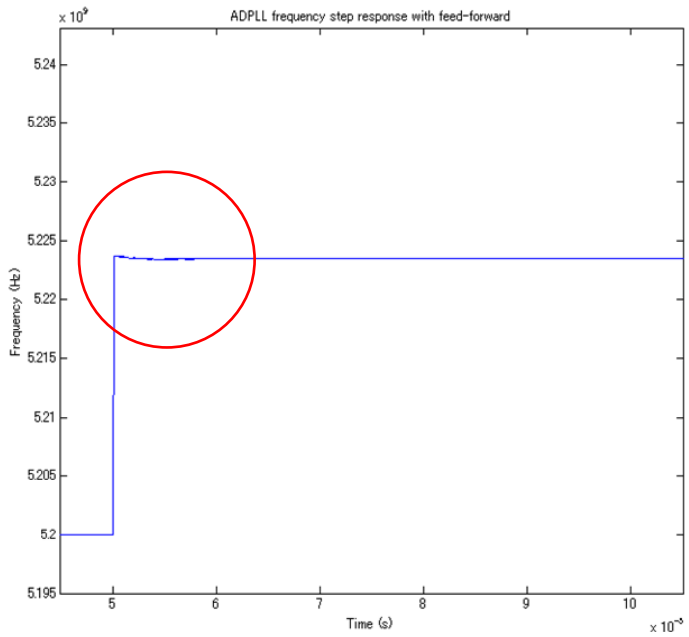
Simulation Results 1

ADPLL with no Feed-Forward

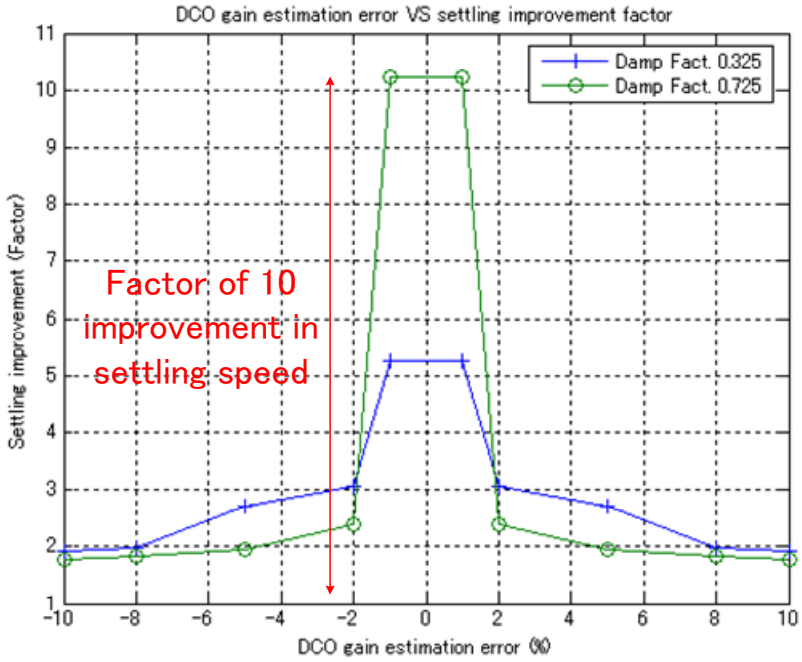


ADPLL with Feed-Forward

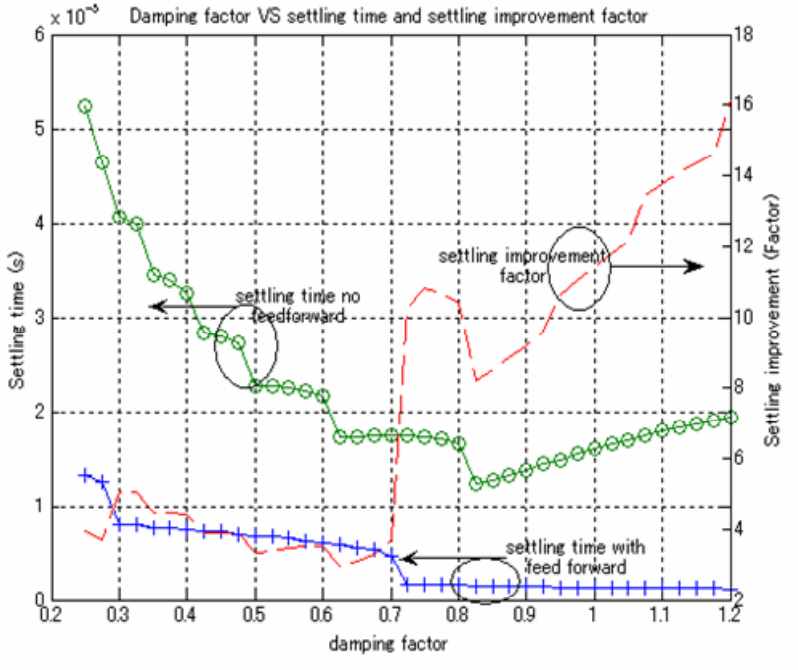


- System Results in Significantly Faster Settling
- Overshoot becomes less dependent on damping factor and is almost eliminated for good DCO gain prediction

Simulation Results 2



All Digital Phase-Locked Loop Settling time improvement VS DCO gain estimation error



All Digital Phase-Locked Loop Settling time and improvement factor VS damping factor at 1% DCO gain prediction error

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Advantages and Challenges of Feed-Forward Compensation

Advantages

- Feed-Forward Compensation does not affect the System's stability as it does not modify the loop's bandwidth or change loop parameters.
- Offset introduced into the system will be compensated for, even if the prediction is bad it does not affect system stability, it only affects settling time
- Feed-Forward can eliminate the system's overshoot's dependence on damping factor for a reasonable DCO gain estimation
- Feed-Forward compensation's settling improvement factor increases with damping factor as the damping factor approaches and exceeds 1 as this is the range for which PLLs are designed for stability

Challenges

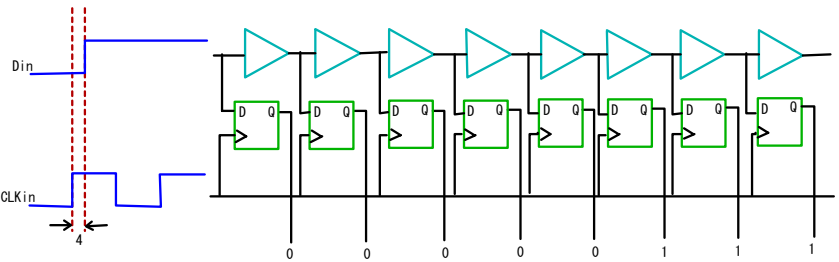
- The actual possible improvement factor is still unknown until a real prototype is designed
- Possibility to extend the feed-forward function from static to dynamic for increased settling improvement is possible, with the possible trade-off of the need for careful design as the stability may be compromised

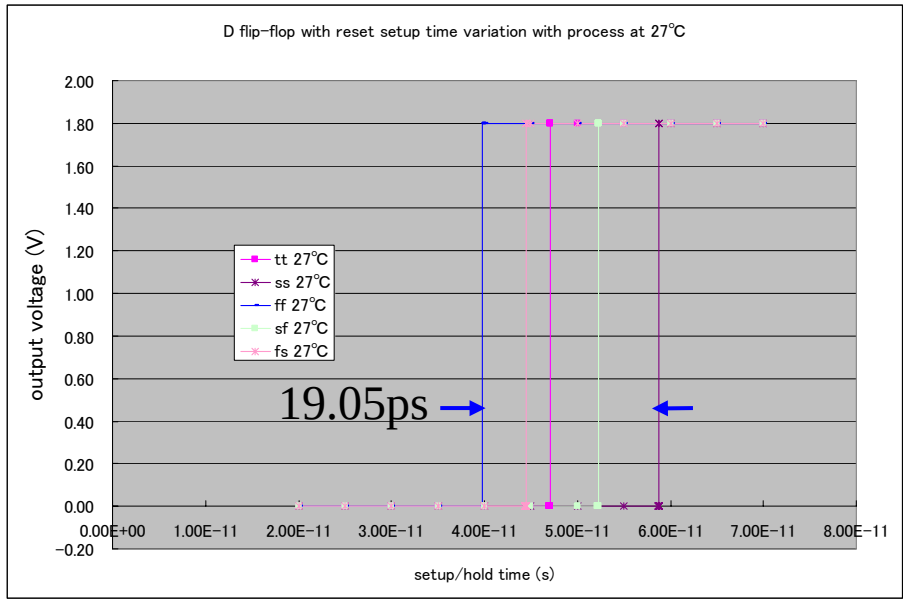
Limitations and Challenges remaining in ADPLL

- System is still fairly complex to design needing many signal processing blocks when compared to conventional PLL
- Major challenges remain in the Phase Detector and DCO
- TDC's resolution cannot be increased enough to support higher frequencies without migrating to more advanced processes
- TDC's accuracy is limited greatly by the process variation, which can degrade the system's phase noise
- DCO's design remain a major challenge with respect to achievable phase noise and tuning range

An example of a remaining challenge, TDC accuracy

In order to accurately know the phase of the feed back signal (DCO) running at GHz frequencies, it is necessary to know to measure the time accurately to within 10s of ps. This simulation shows the process variation of D-flip-flops used in the TDC for a 0.18um CMOS process. Process corners varying by 3 sigmas show the flip-flop's setup-hold time variation of nearly 20ps. This problem becomes greater for higher frequency PLLs.





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R. B. Staszewski and P. T. Balsar, "Phase-Domain All-Digital Phase-Locked Loop," IEEE Trans. Circuits and Systems II, Vol. 52, pp. 159-163, Mar. 2005.

Thank you for listening

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