All-Digital Phase-Locked Loops, its Advantages and Performance Limitations

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Abstract—The All-Digital Phase-Locked Loop has several advantages when compared with traditional charge-pump based PLL. We will introduce some of its advantages in this paper, showing how they can be used to improve the system's performance. In addition, performance limitations of the system will be discussed.

I. INTRODUCTION

Although ADPLLs are not new, only recently have they been used in frequency synthesizers capable of producing low enough phase noise, at high enough frequencies to be used with RF systems [1]. Figure 1 compares a charge-pump based PLL with all-digital PLLs (ADPLL).

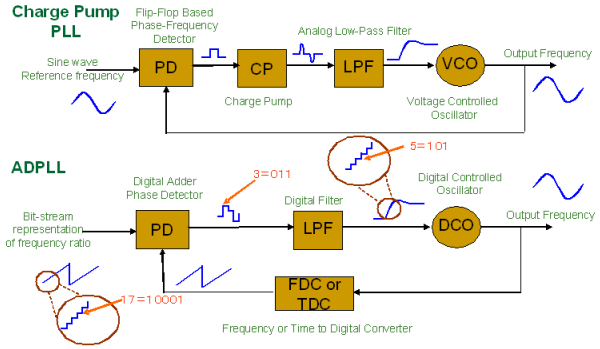

Fig. 1: Comparison between Charge-Pump PLL and ADPLL

High-Frequency ADPLLs are, however, are still not well understood, and its advantages and uses are still in development. In this paper we will introduce our research which focuses on the analysis of ADPLLs, their major advantages over traditional charge-pump PLLs and their performance limitations.

II. COMPARISON BETWEEN ADPLL AND TRADITIONAL CHARGE-PUMP BASED PLL

From Fig.1 the difference between charge-pump based PLL and ADPLL can be observed. Starting from the voltage-controlled oscillator which is replaced by the digital controlled oscillator (DCO), the flip-flop based phase-frequency detector and charge-pump of the charge-pump PLL is replaced by the time-to-digital converter or frequency-to-digital converter and adder. Finally the analog low-pass filter is replaced by a digital low pass filter. By comparing the charge-pump PLL with the ADPLL, it can also be seen that while the phase-frequency detector is created from digital components, its input and output is basically analog as is all other signals in the charge-pump PLL. On the contrary, in the ADPLL, all intermediate signals, except for the DCO's output are digital.

The advantages of having access to intermediate signals in digital form are significant. The system's loop bandwidth, for example, can be changed easily and on the fly during the PLL's locking enabling both fast frequency acquisitions and low phase noise. The intermediate signals can also be used to monitor the system in real time, and digital signal processing techniques can be used to take advantage of the system by, for example, performing direct frequency modulation on the PLL's output [2]. We have shown that the digital nature of the ADPLL can be exploited to improve its settling characteristics [3]. This technique will be briefly introduced in the next section.

III. DIRECT REFERENCE FEED-FORWARD COMPENSATION

The linear continuous time approximation model of the PLL with feed-forward is shown in Fig. 2 where $\omega_{ref}(s)$ represents the input reference frequency, θ_{ref} is the reference phase, e(s) is the error signal, F(s) represents the loop filter, $K_{vco}(s)$ is the voltage controlled oscillator (VCO) gain, ω_{fvco} is the free running VCO frequency, $\omega_{out}(s)$ is the output frequency, and $\theta_{out}(s)$ is the output phase.

Mathematically, it is possible to conceive a system which feed-forwards the input reference to the VCO's input bypassing the subtraction and loop filter as shown in Fig. 2. Such feed-forwarding techniques maybe used to speed-up the PLL's system's settling speed without increasing the bandwidth which will compromise the phase noise performance and stability.

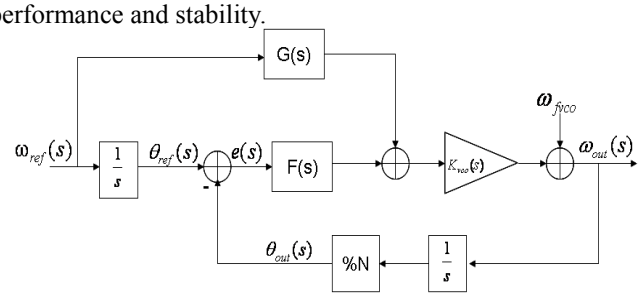

Fig. 2. Conception of the feed-forward PLL.

From Fig. 2 it is seen immediately that the feed-

forward compensation system is difficult to implement in an analog system as the function G(s) requires the conversion of the input frequency to output voltage. Although it has been shown to be possible to create such a system with charge pump based PLLs [4], in practice it is difficult to realize such a system in analog domain as digital-to-analog converters and a complex digital signal processor is necessary. In addition, prefabrication of the VCO is necessary to measure it's gain which is used in the system.

In the ADPLL type system, this feed-forwarding can be accomplished much more easily. As both the input reference and the DCO's input are in digital format, translating the input frequency representation value, to the DCO's input control value is accomplished by a simple mathematical conversion. It has been shown in [3] that the conversion values needed for this feed-forwarding can be found by simply stimulating the ADPLL and measuring the necessary values by tapping the correct nodes of the ADPLL. Our Matlab simulation results have shown that the ADPLL's settling speed can be improved significantly depending on the ability to predict the DCO's gain. The settling improvement factor is shown in Fig. 3.

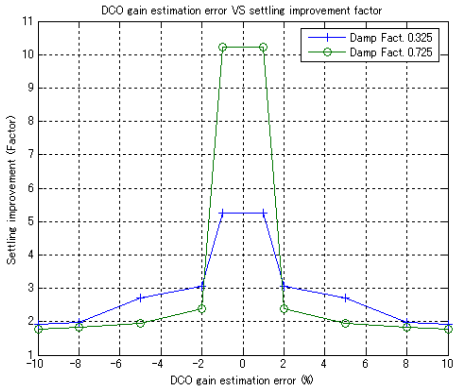

Fig. 3. PLL settling improvement factor VS DCO gain estimation error

The settling factor improvement depends on the damping factor as shown in Fig.3. We have shown [3] that in our example system, the ADPLL with feed-forward is able to settle in $1/8^{th}$ the time of a system without feed-forwarding. Greater improvements are possible in real systems in which the damping factor is close to 1. As shown in Fig.3 the settling time can be improved by a factor of 10 for damping factor of 0.725.

IV. LIMITATIONS OF ADPLL SYSTEM'S ACCURACY

A major problem in the ADPLL relates to the accuracy of the system which depends on the resolution of the time to digital converter (TDC). It can be shown that the accuracy of the time resolution measured by the TDC directly affects the system's incremental frequency step.

$$\Delta f = f_{\max}^{2} \cdot t_{step} \qquad (1)$$

Where Δf is the incremental frequency step, f_{max} is the maximum oscillating frequency, and t_{step} refers to the frequency step resolution of the TDC. To achieve an acceptable level of incremental frequency needed in a PLL, with GHz range oscillating DCO, pico-second order level accuracy of the TDC is necessary.

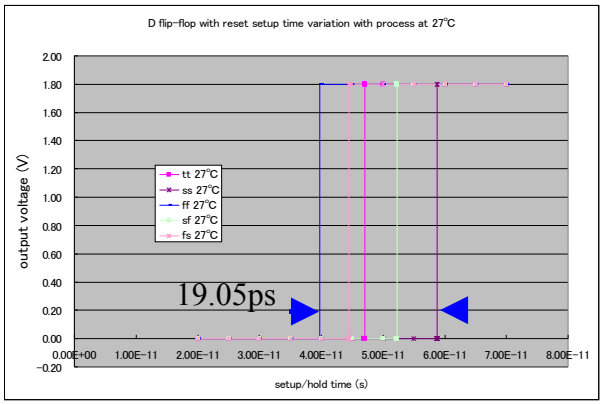

Fig.4 Flip-flop setup time with process corner.

From our study we have observed that the delay elements used inside the digital TDC as used in [1], can experience process variations in excess of 30% over 3 sigma, while the flip-flop's setup time can vary by more than 30% for 0.18um CMOS process. This greatly decreases the accuracy of the system, which will intern degrade the phase noise of the ADPLL system.

V. CONCLUSION

ADPLL systems have many advantages over the traditional charge-pump PLLs. The ability to use digital signal processing to improve the system's performance is significant and can make the system much more adaptive. However, serious issues with the TDC's accuracy still limits the ADPLL's performance which must be further studied.

REFERENCE

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