Introduction to Embedded Data Converters

Akira Matsuzawa

Tokyo Institute of Technology

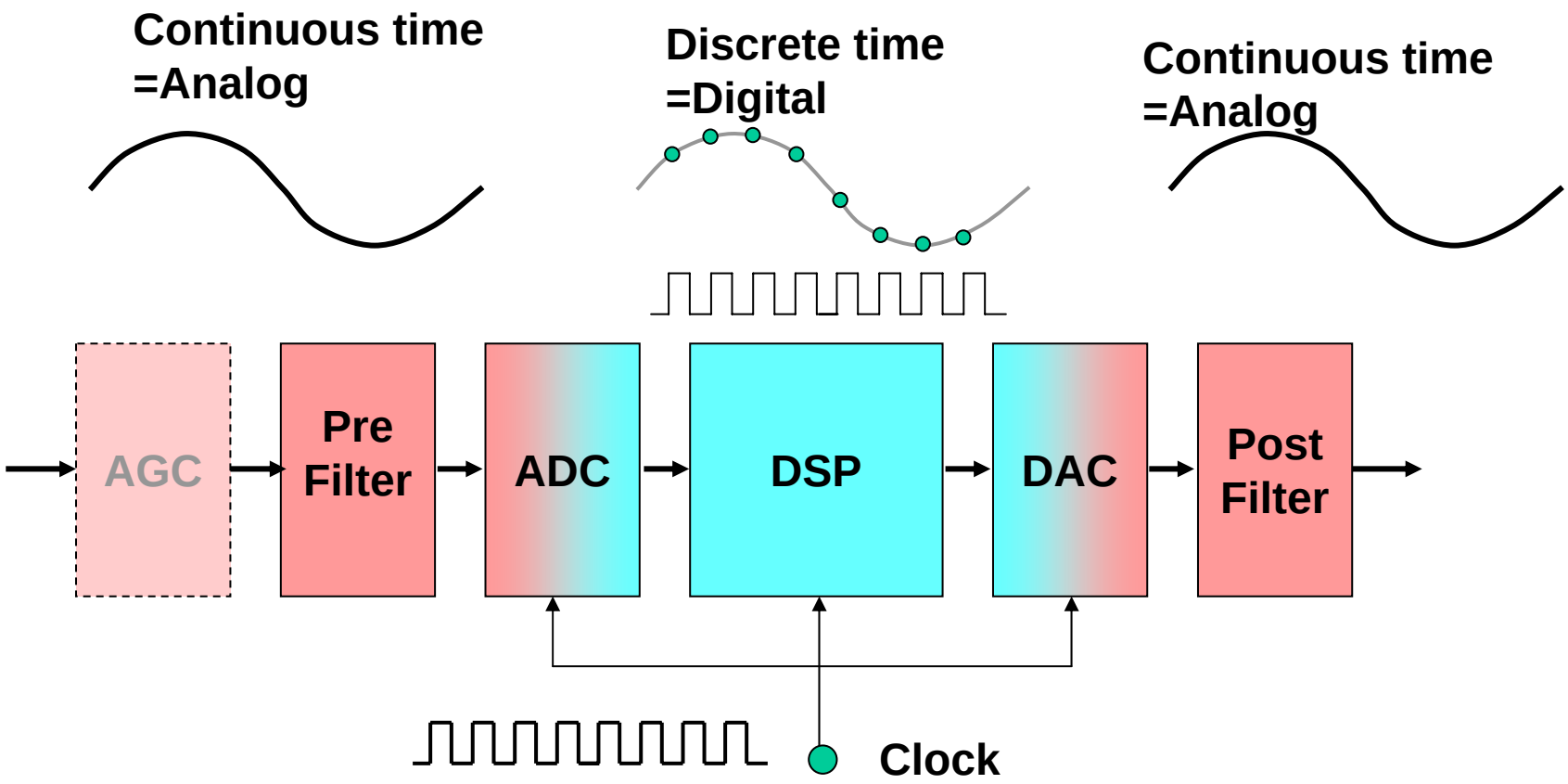
Contents

1. Introduction

- **Mixed signal systems**
  - **Software defined radio**
  - **Digital read channel**
  - **Mixed Signal SoC**
- **Progress of ADC and DAC**
  - **Power and area**
  - **Embedding**

Basic mixed signal system

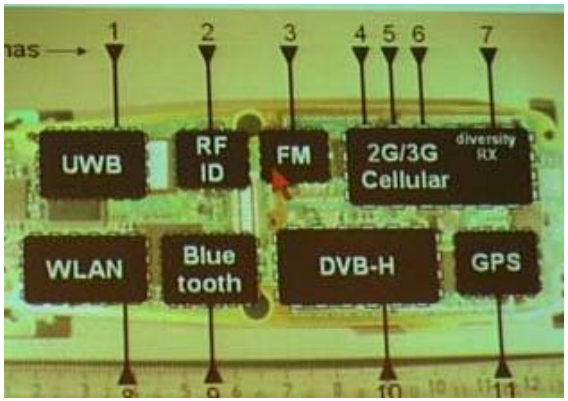
Mixed signal systems basically consist of DSP, ADC, DAC, and pre/post filters. The signals are converted between continuous time and discrete time.



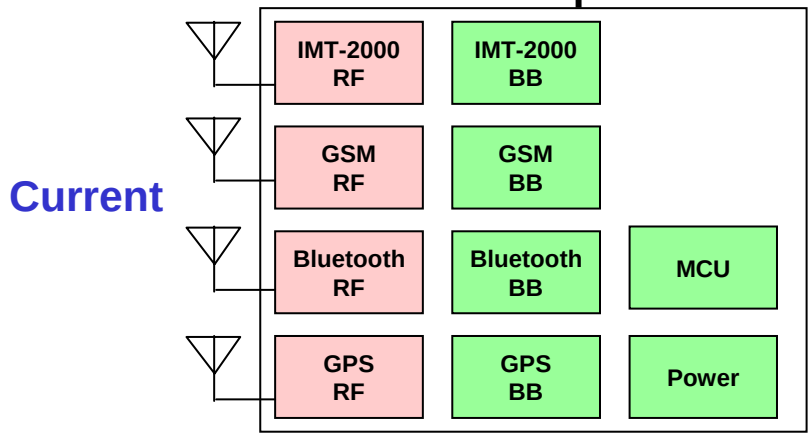
Software defined radio

Future wireless systems need powerful ADC and DAC for software defined radio.

Future cellular phone needs 11 wireless standards!!

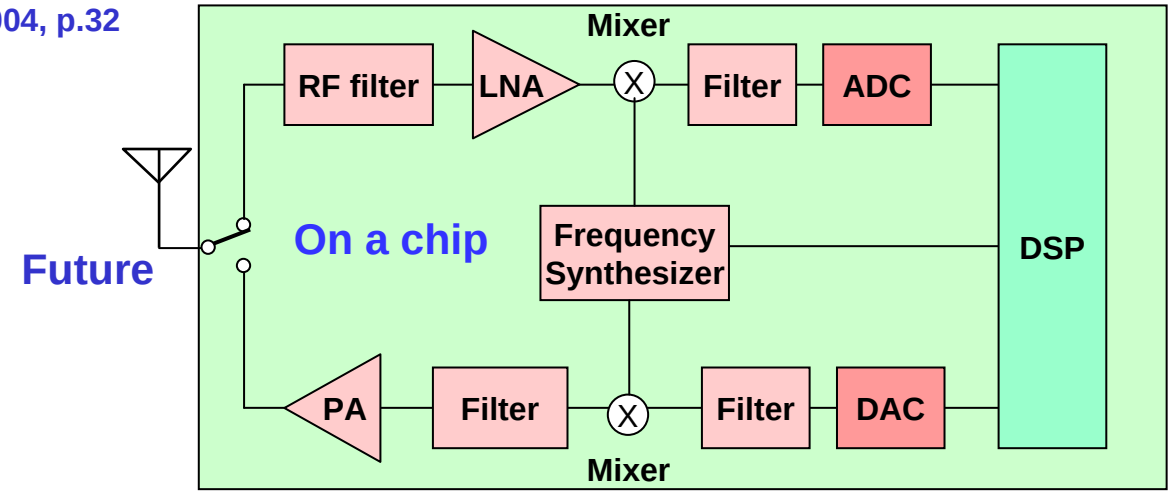


Multi-standards and multi chips



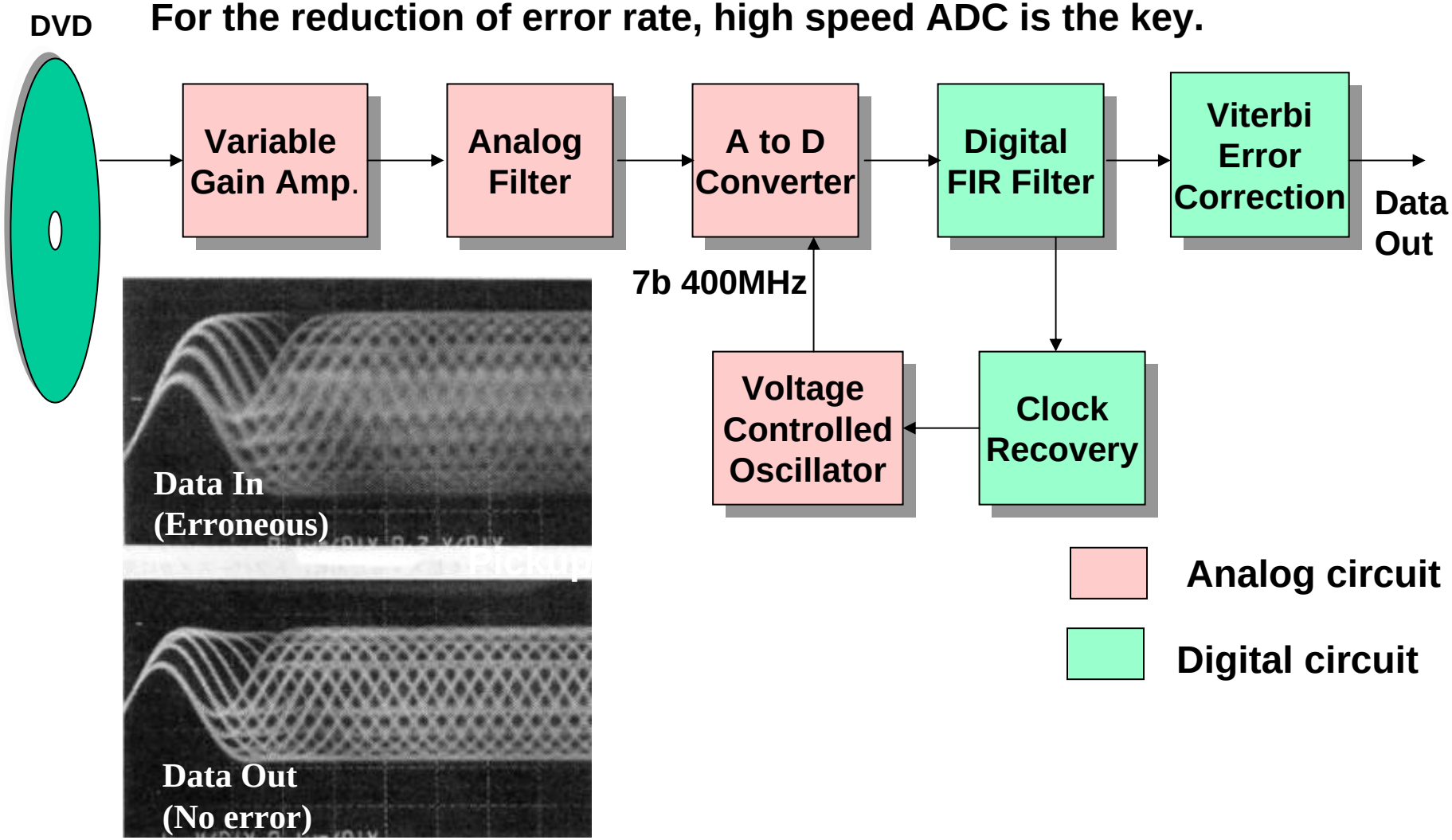
Multi-bands and Multi-standards on a single chip

Yrjo Neuvo, ISSCC 2004, p.32



Mixed signal tech. ; Digital read channel

Digital storage needs high speed mixed signal technologies.
For the reduction of error rate, high speed ADC is the key.

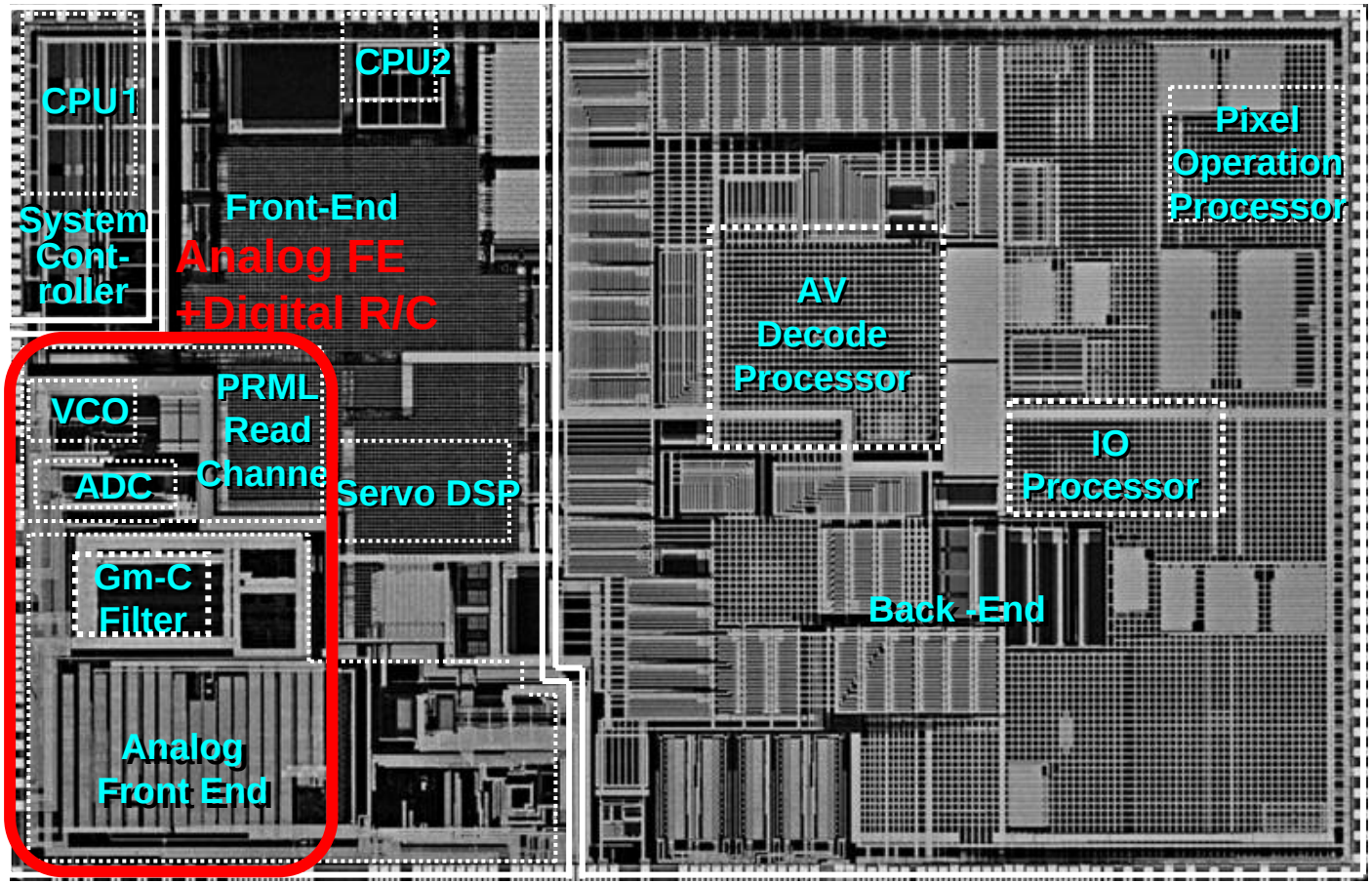


Mixed signal SoC

Mixed signal SoC can realize full system integration for DVD application.

Embedded analog is the key.

0.13um, Cu 6Layer, 24MTr

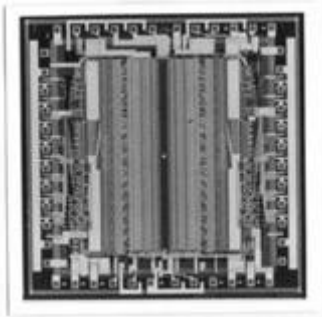


Okamoto, et al., ISSCC 2003

Progress of high-speed ADC

High speed ADC can be embedded in CMOS resulting in power reduction.

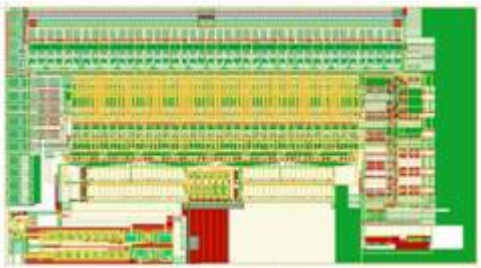
ISSCC 1991



6b, 1GHz ADC
2W,
1.5um Bipolar

Matsuzawa, ISSCC 1991

ISSCC 2000



6b, 800MHz ADC
400mW, 2mm^2
0.25umCMOS

Sushihara, et al, ISSCC 2000

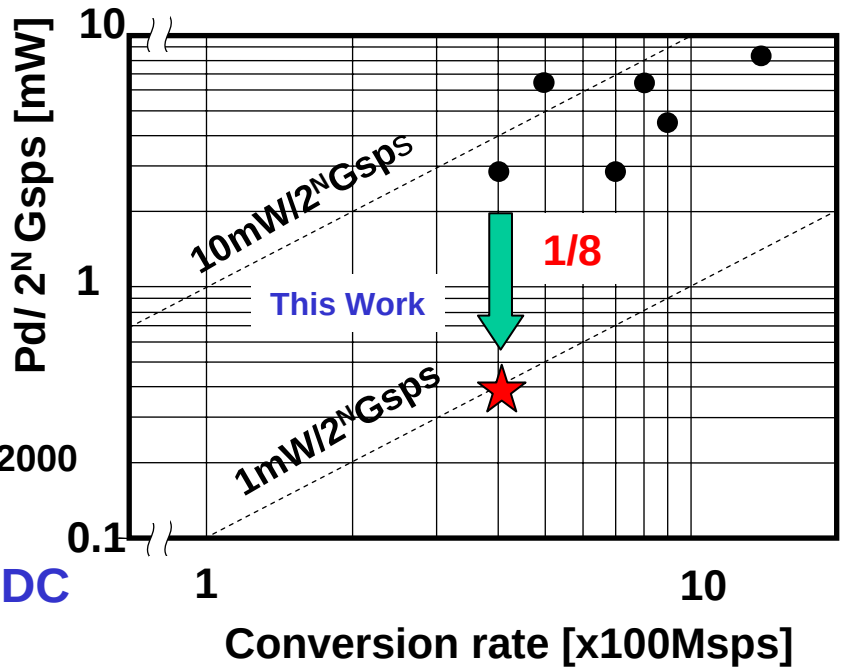
ISSCC 2002

World lowest Pd HS ADC

7b, 400MHz ADC
50mW, 0.3mm^2
0.18umCMOS

Sushihara and Matsuzawa, ISSCC 2002

Pd of high speed CMOS ADCs

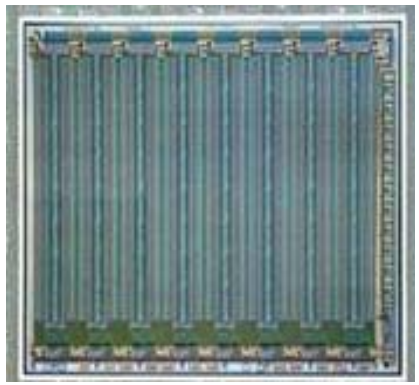


Progress of A/D converter; video-rate 10b ADC

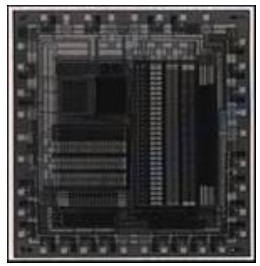
1/2000 in Power and 1/200,000 in cost during past 20 years

ADC was the bottle-neck for the digital TV and Video systems
Technology progress has solved this problem.

1980	1982	1993	Now
Conventional product	World 1st Monolithic	World lowest power	SoC Core
Board Level (Disc.+Bip) 20W $ 8,000	Bipolar (3um) 2W $ 800	CMOS (1.2um) 30mW $ 2.00	CMOS (0.15um) 10mW $0.04



T. Takemoto and A. Matsuzawa,
JSC, pp.1133-1138, 1982.

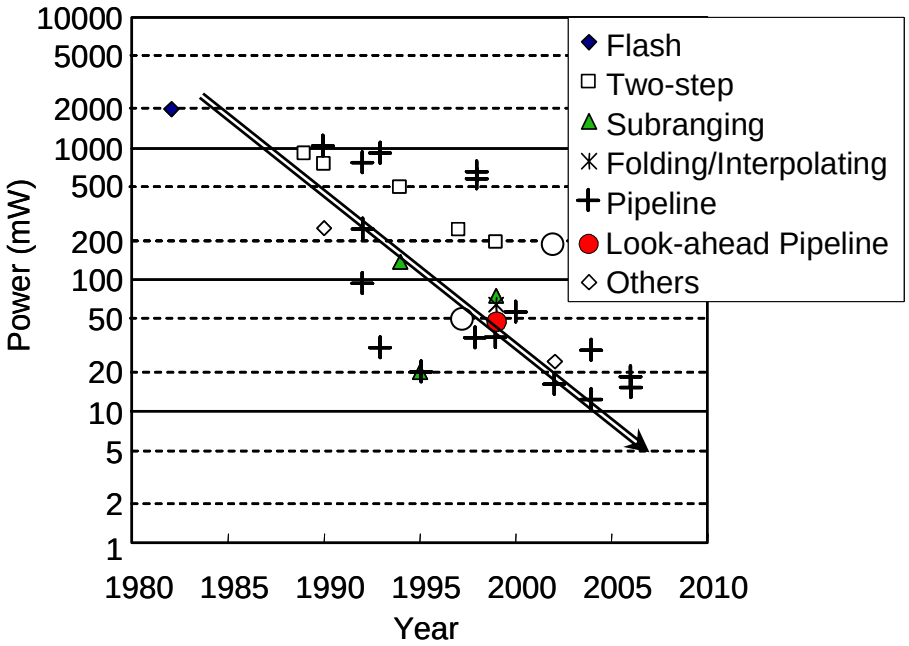


K. Kusumoto and A. Matsuzawa,
ISSCC 1993.

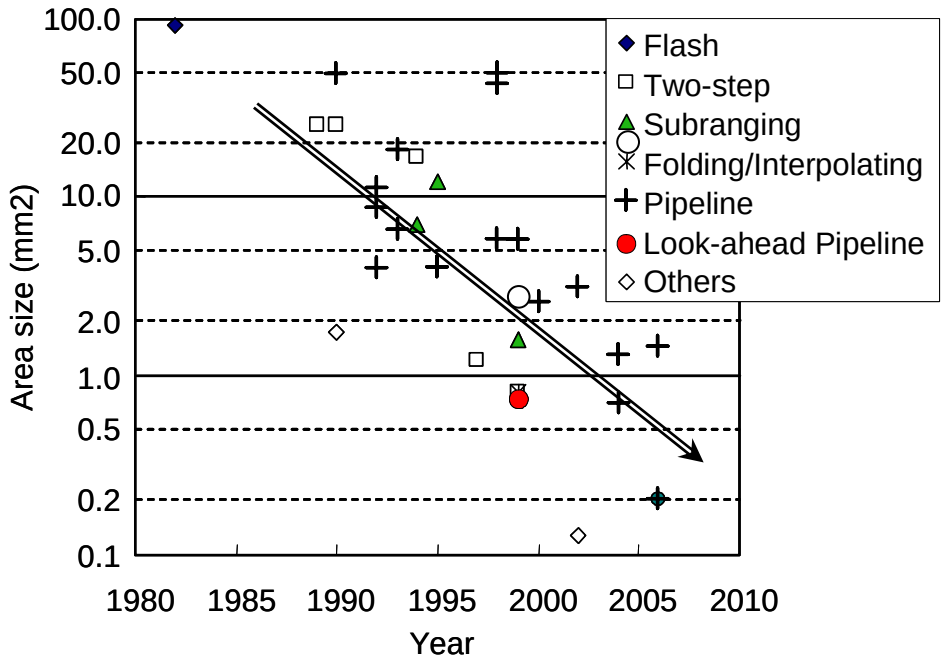
Power and area reduction of video-rate 10b ADCs

Power and area of ADC have been reducing continuously.
Currently, ADC can be embedded on a chip

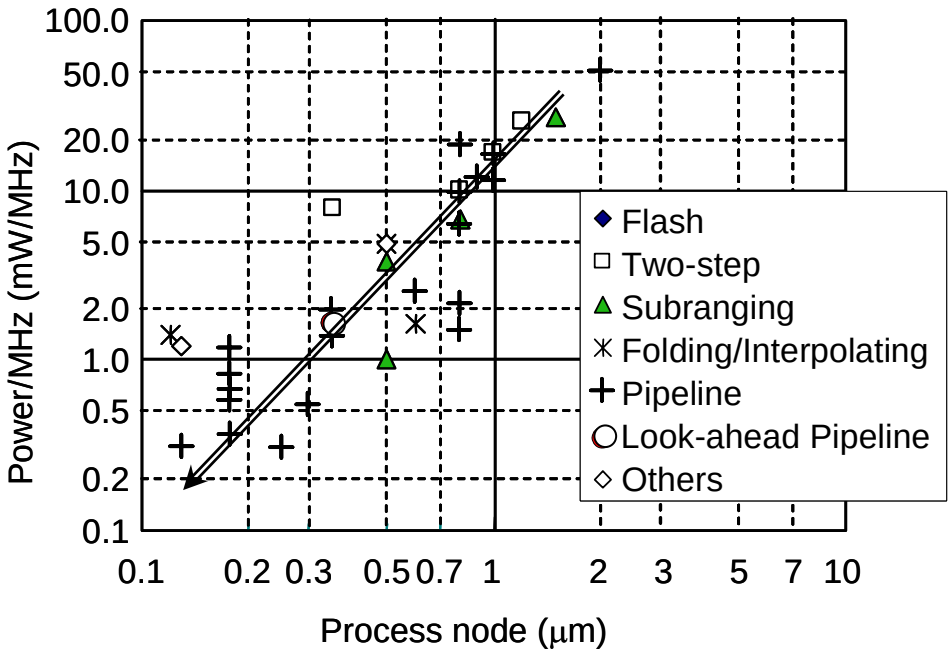
Power reduction

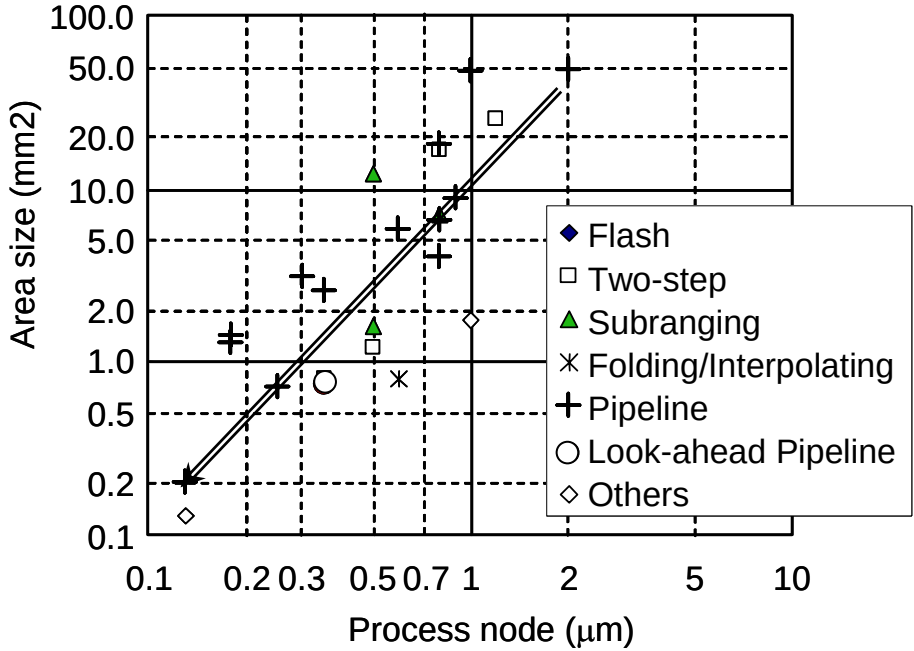


Area reduction



Power and area reduction of video-rate 10b ADCs





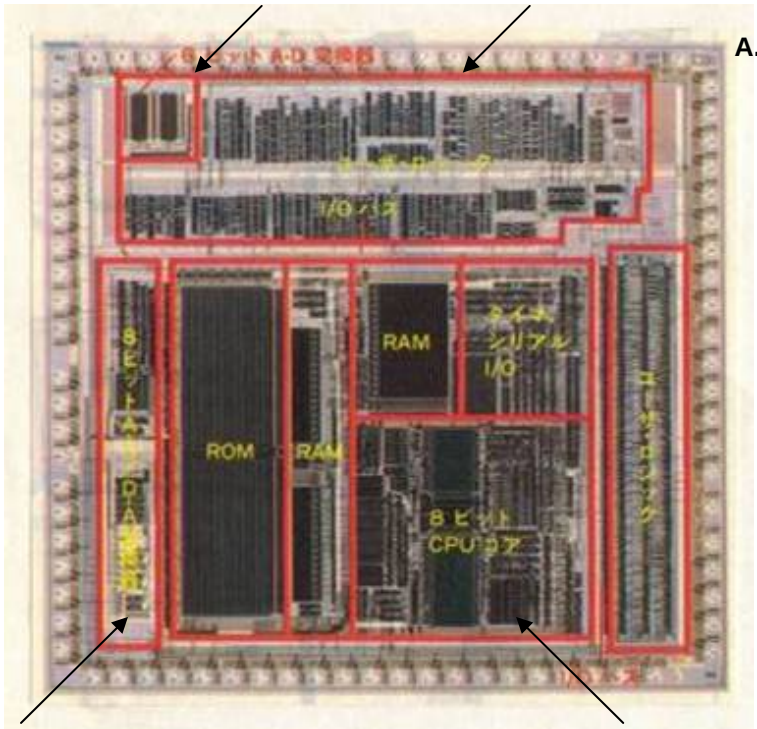
M. Hotta et al. IEICE 2006. June

Embedding ADC on a CMOS chip

CMOS ADC and DAC has been embedded on a CMOS chip.
This has realized low cost and low power digital portable AV products.

1993 Model: Portable VCR with digital image stabilizing

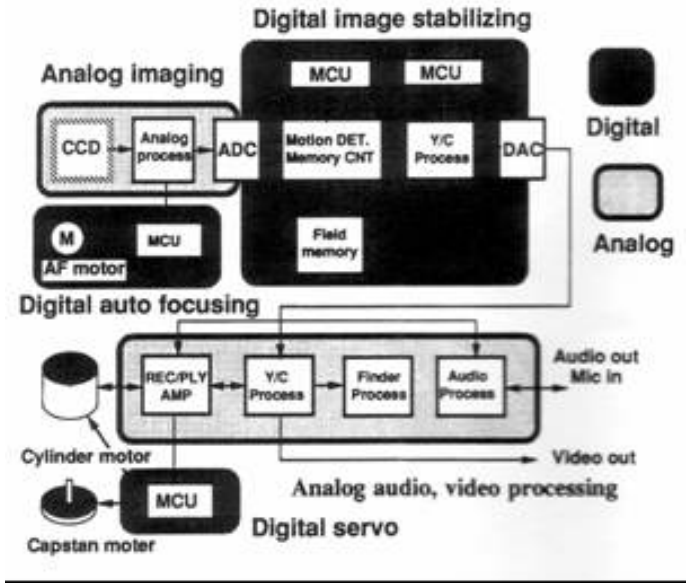
6b Video ADC **Digital Video filter**



8b low speed ADC;DAC **8b CPU**

A. Matsuzawa, JSC, pp. 470-480, 1993.

System block diagram

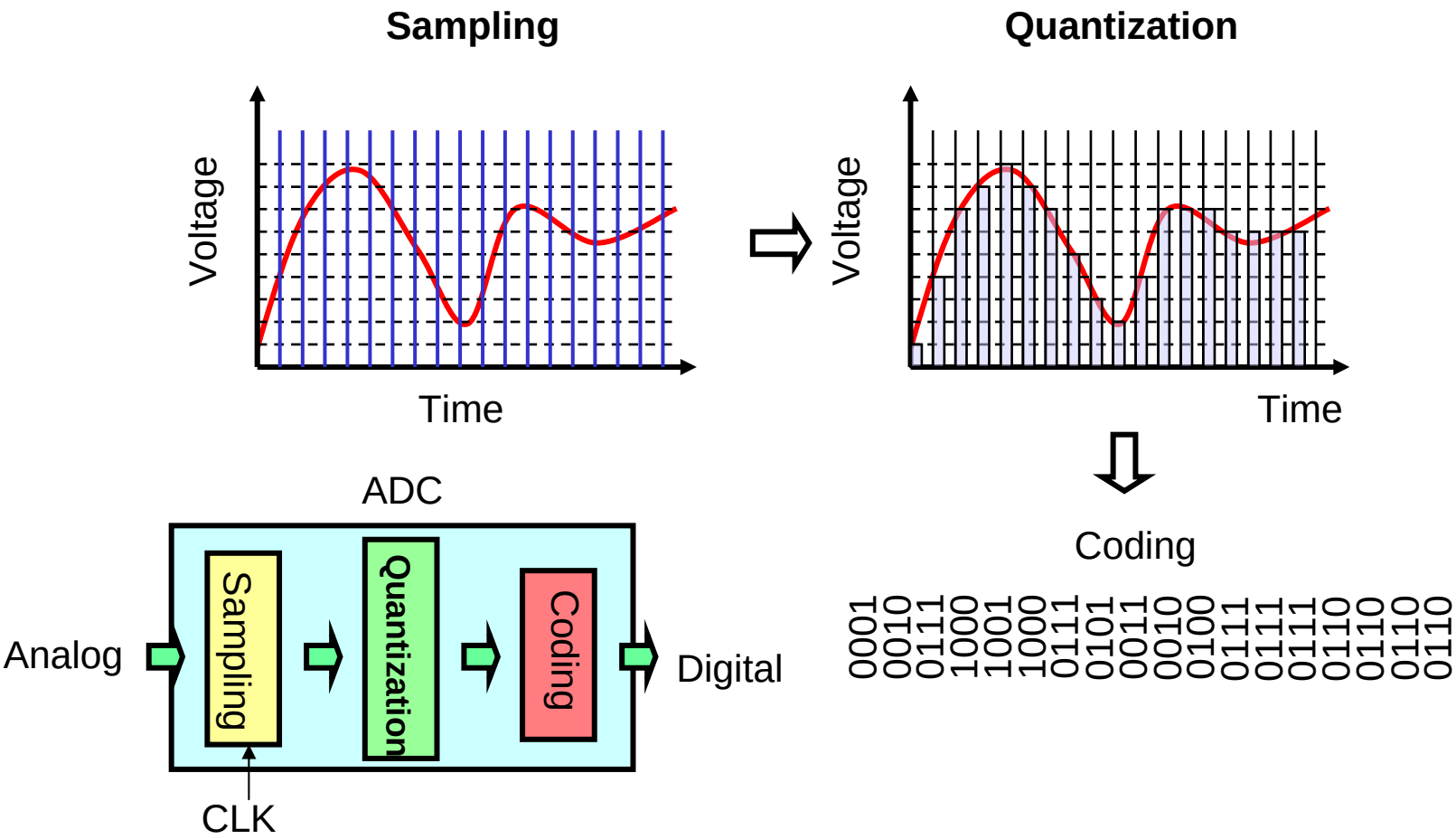


2. Characterization of data converters

- **Basic functions of ADC and DAC**
- **Static performance**
  - **INL, DNL, monotonicity**
  - **Quantization noise**
- **Dynamic performance**
  - **SNR, SFDR, THD, SNDR, ENOB**
  - **Sampling Jitter**
  - **ERB**
  - **Glitch**
- **Figure Of Merit**
- **Performances and applications**
  - **Needed performances for wireless systems**

Basic functions of ADC

Sampling: Sampling the analog signal with accurate timing.
Quantization: Express the converted data with certain accuracy.



Static performance

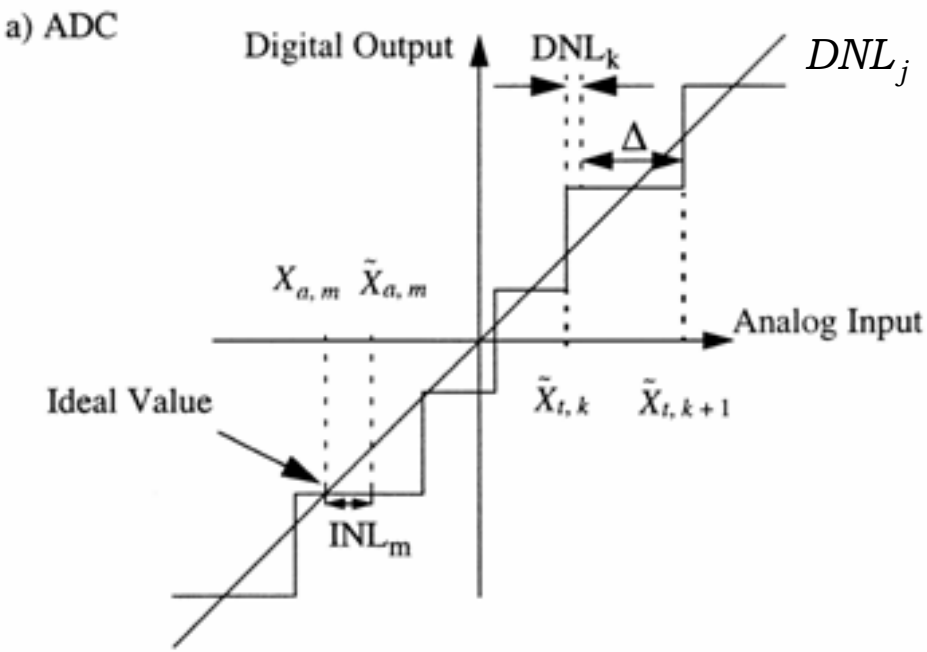
INL and DNL are the major static performance indicators of ADC and DAC.

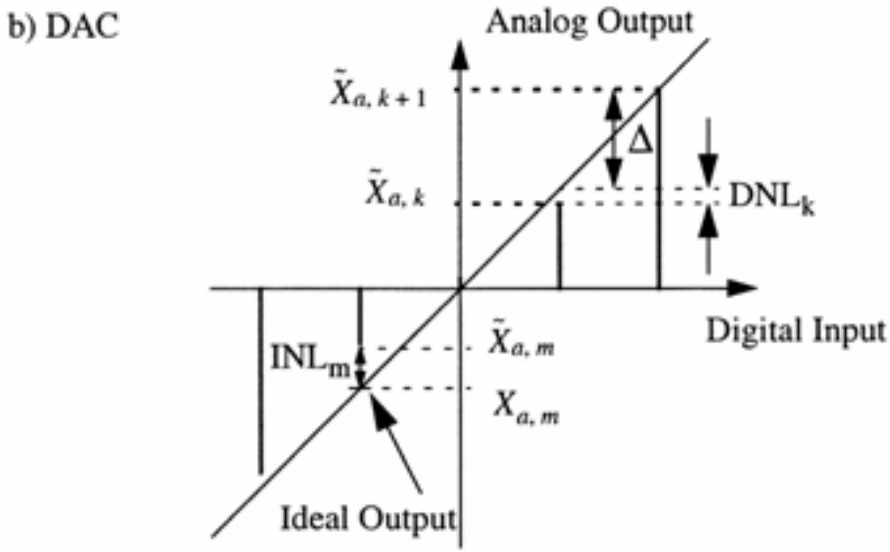
DNL: Differential Non-Linearity $DNL_j \equiv \frac{Width_{ACTUAL,j} - Width_{IDEAL}}{Width_{IDEAL}}$

INL: Integrated Non-Linearity $INL_j \equiv Transfer\ function_{ACTUAL,j} - Transfer\ fuction_{IDEAL,j}$

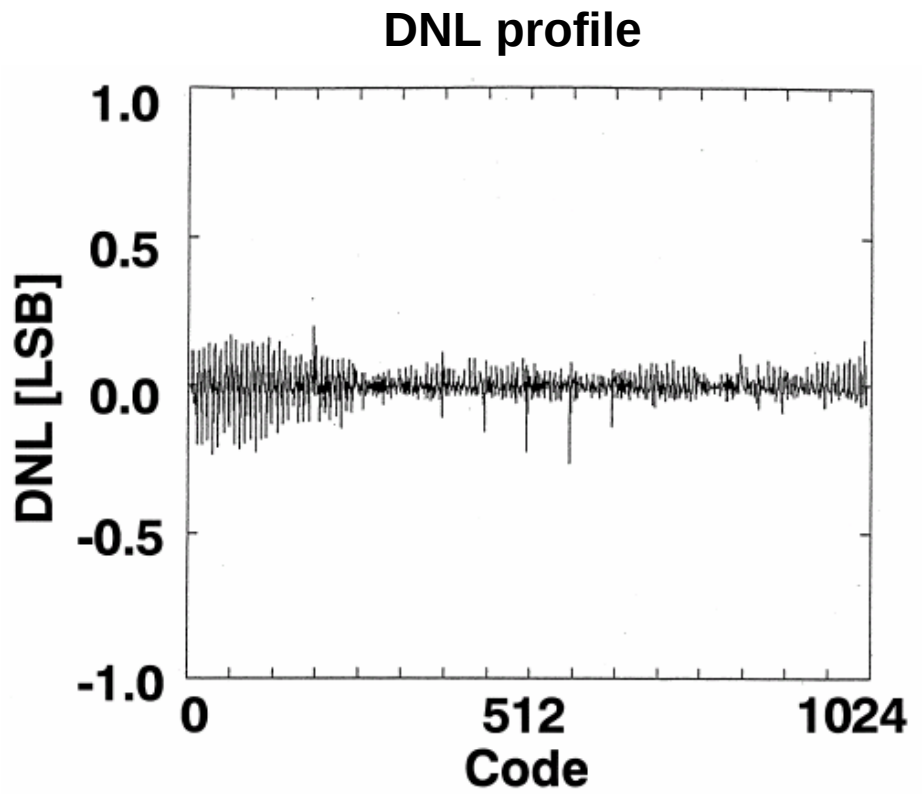
$$INL_j = \sum_{k=0}^{k=j} DNL_k$$

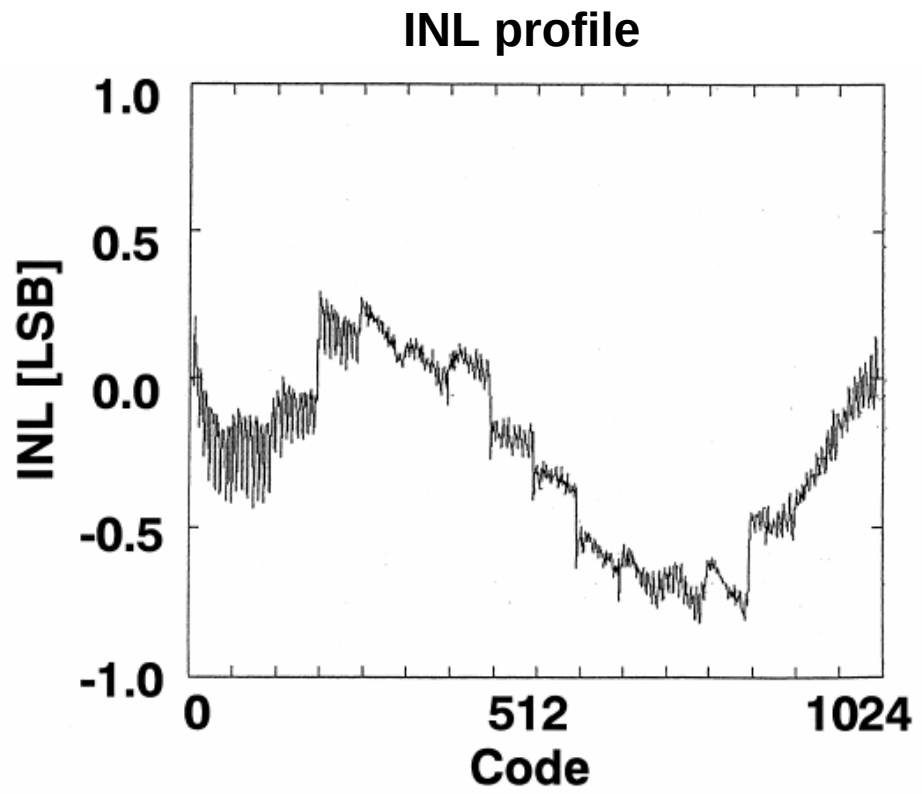
$$DNL_j = INL_{j+1} - INL_j$$





DNL and INL


DNL profile
1.0
0.5
0.0
-0.5
-1.0
DNL [LSB]
0
512
1024
Code


INL profile
1.0
0.5
0.0
-0.5
-1.0
INL [LSB]
0
512
1024
Code

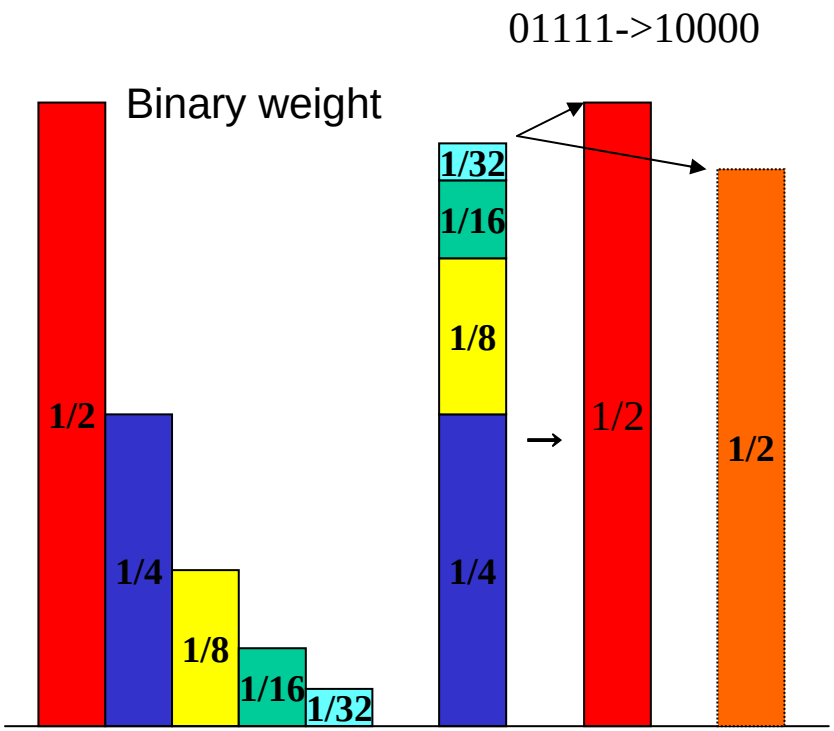
Monotonicity in DAC

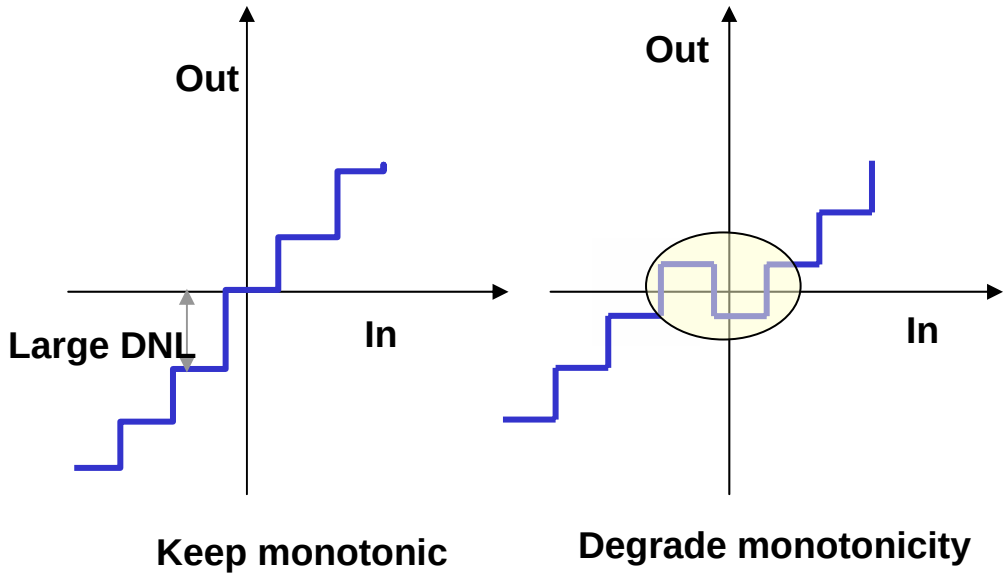
Binary coded DAC often degrades monotonicity.

The monotonicity stands for the qualitative characteristics of data converters of which transfer function keep the monotonic increase or decrease.

At the change of MSB bit

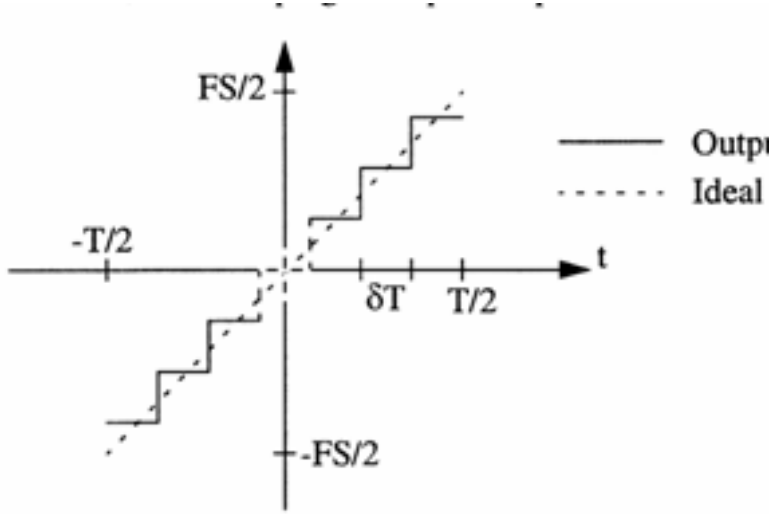
If the converter can not guarantee the monotonicity, The feedback loop doesn't work properly and results in backrush.





Quantization noise

Quantization causes noise

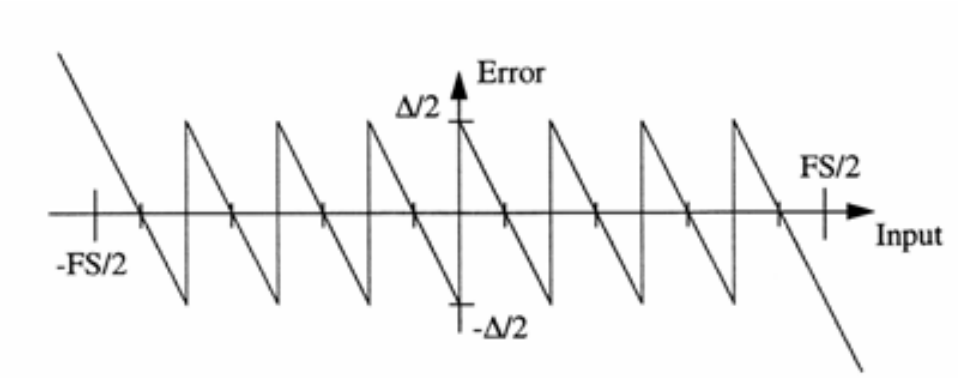


Transfer characteristics

$$P_n = \int_{-\Delta/2}^{\Delta/2} e^2 P(e)de = \int_{-\Delta/2}^{\Delta/2} e^2 \frac{1}{\Delta} de = \frac{\Delta^2}{12}$$

$$\because P(e) = \begin{cases} \frac{1}{\Delta}, & |e| < \frac{\Delta}{2} \\ 0, & all\ other\ e \end{cases}$$

Higher SNR needs higher resolution



Quantization noise

$$P_s = \frac{\left(\Delta \cdot 2^{N-1}\right)^2}{2}$$

$$SNR \equiv \frac{P_s}{P_n} = \frac{\left(\Delta \cdot 2^{N-1}\right)^2}{2} \cdot \frac{12}{\Delta^2} = 1.5 \cdot 2^{2N}$$

$$SNR_{dB} = 10\,log\left(\frac{P_s}{P_n}\right) = 6.02 \cdot N + 1.76$$

Dynamic performance

Dynamic performance indicates the ratio between signal and noise or distortion.

We should use the suitable terms depending upon the type of application.

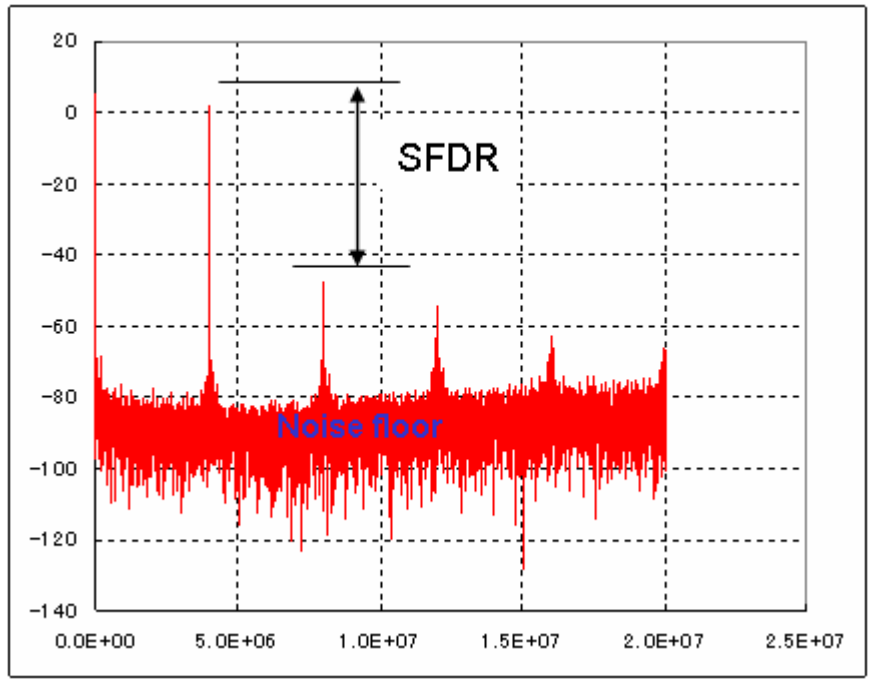
$$SNR = 10\log\frac{Signal\ power}{Total\ noisefloor\ power}$$

$$SFDR = 10\log\frac{Signal\ power}{Largest\ spurious\ power}$$

$$THD = 10\log\frac{Total\ harmonic\ distortion\ power}{Signal\ power}$$

$$SNDR = 10\log\frac{Signal\ power}{Noise\ and\ distortion\ power}$$

$$ENOB = \frac{SNDR - 1.76}{6.02}$$

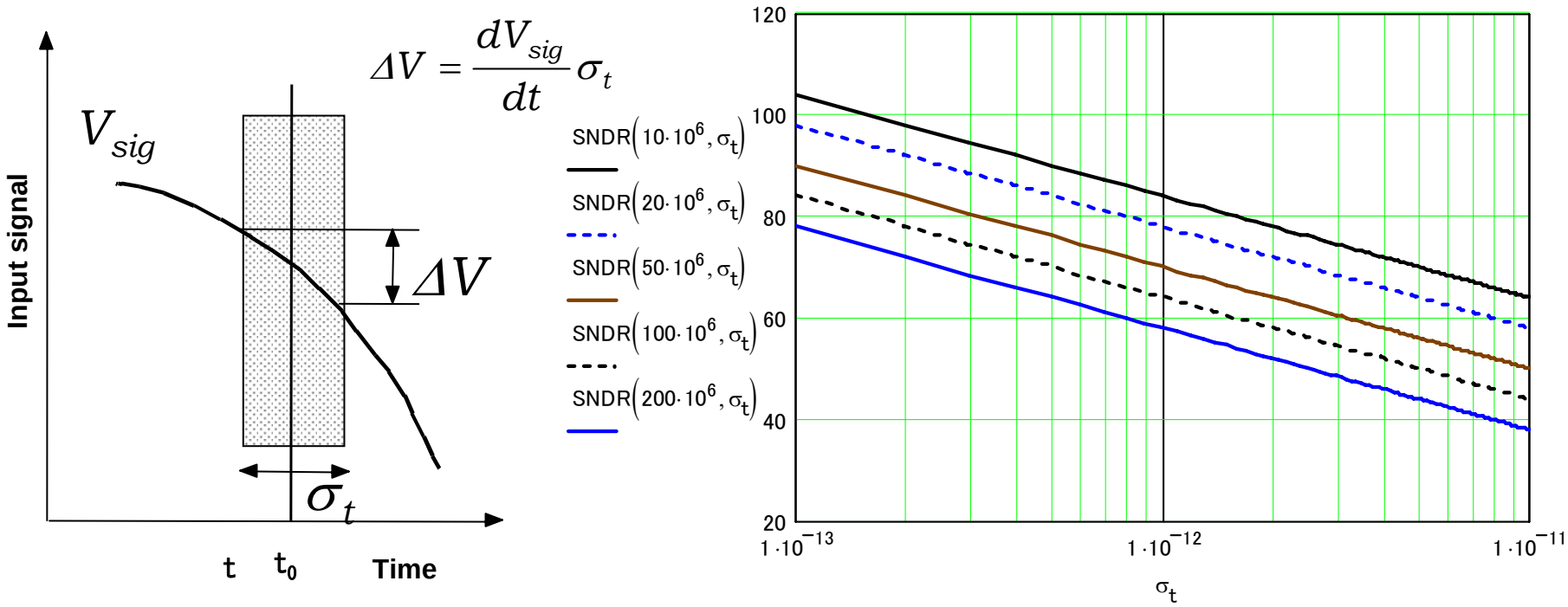


F_c=40MHz, f_{in}=4MHz
SFDR=49.8dB
SNDR=44.9dB, ENOB=7.17-bit
2ndHD=-49.8dB, 3rdHD=-56.7dB

Sampling jitter effect

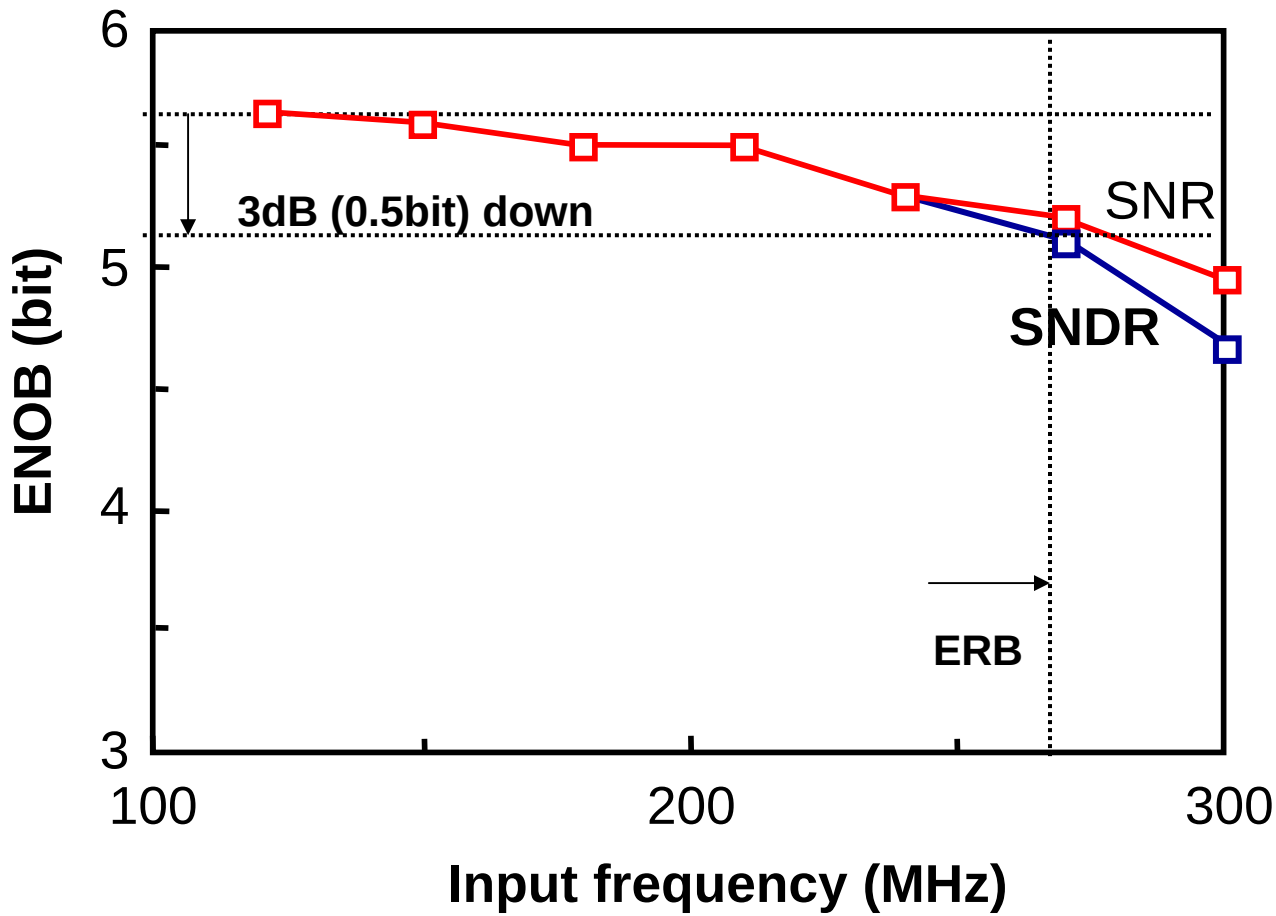
Sampling jitter is converted to noise.
When the input frequency becomes higher, the SNR becomes lower.

$$SNDR(dB) = -10\log\frac{1}{(2\pi f_{in}\sigma_t)^2}$$



Effective Resolution Bandwidth

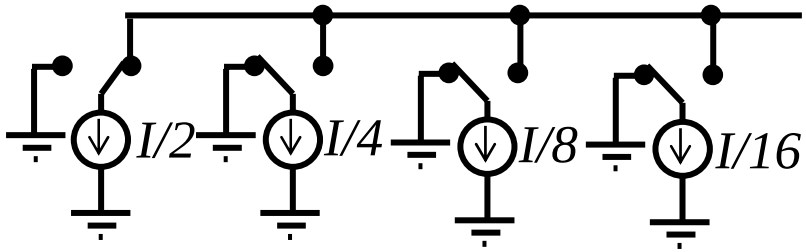
ERB is the input frequency where the SNDR has dropped 3dB (or ENOB 0.5 bit)



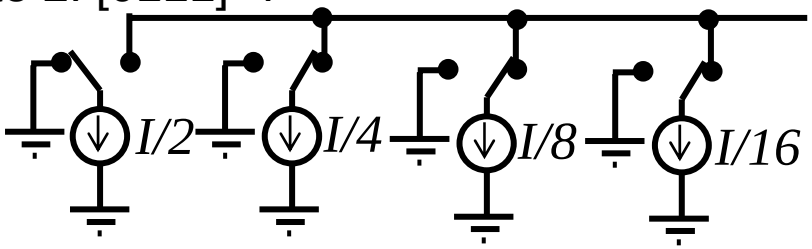
Glitch

Glitch is the spiky signal at code transition.

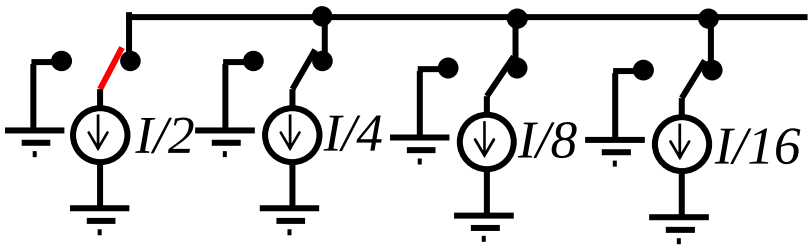
State 1: [1000]=8



State 2: [0111]=7



Intermediate: [1111]=15



Caused by overlapping of signals
This appears within a few psec,
However, energy is not negligible.
Glitch causes the distortion of signal

$$P_{g,max} = 2^{2N-2} \cdot \Delta^2 \cdot \frac{T_g}{T_s}$$

$$P_{g,max} < P_{QN} = \frac{\Delta^2}{12}$$

$$\therefore T_g < \frac{T_s}{3 \cdot 2^{2N}}$$

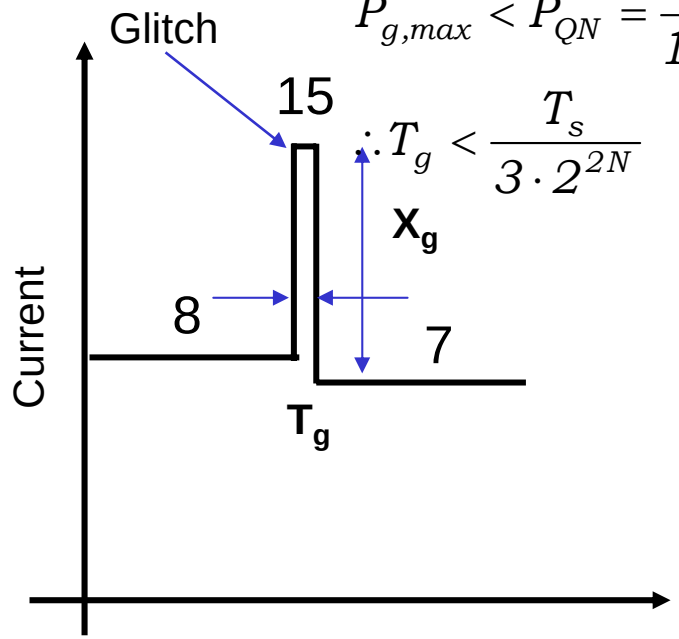


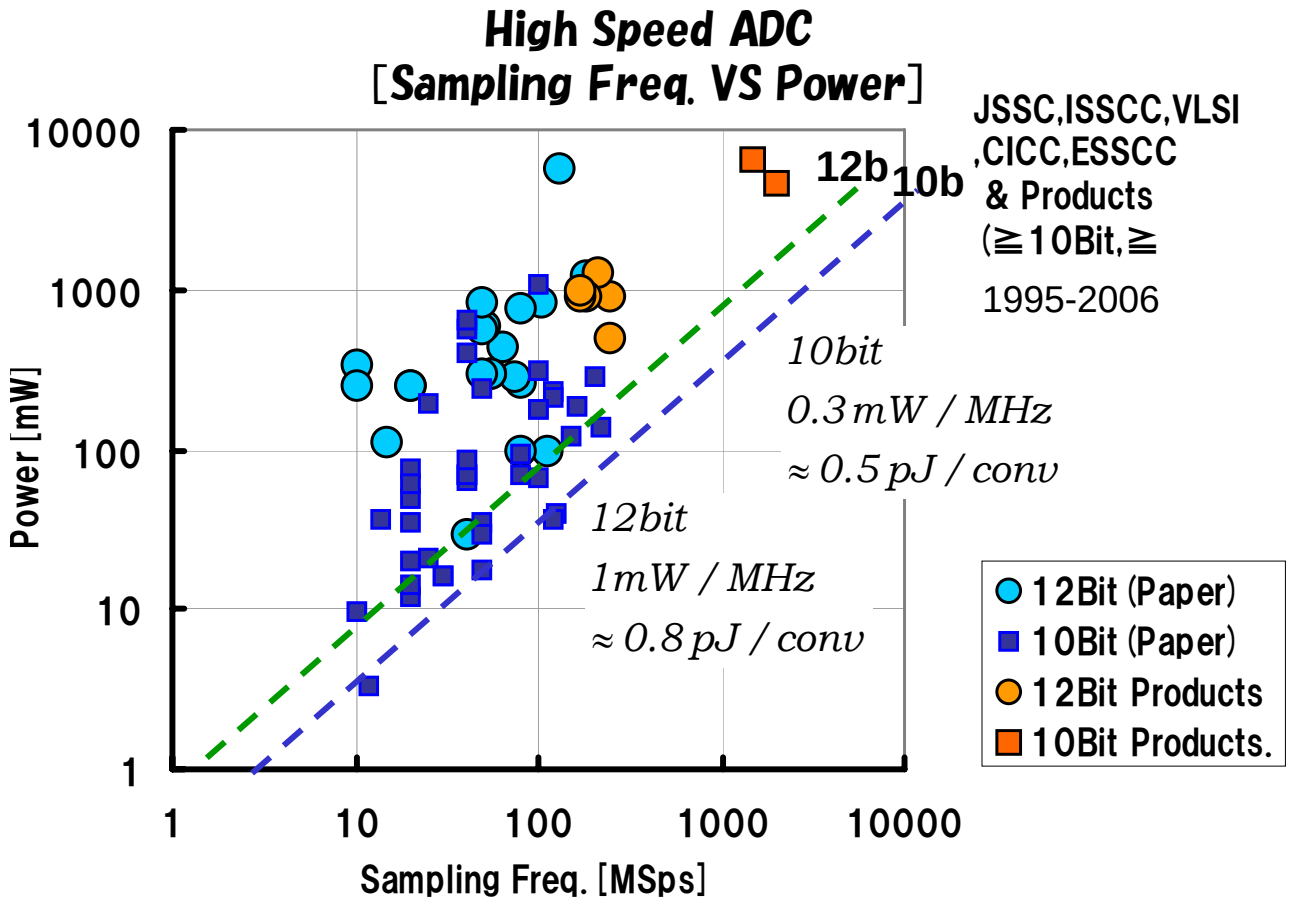
Figure Of Merit

Figure of merit shows energy efficiency for data conversion.

$$FOM = \frac{Energy}{Conversion\ step}$$

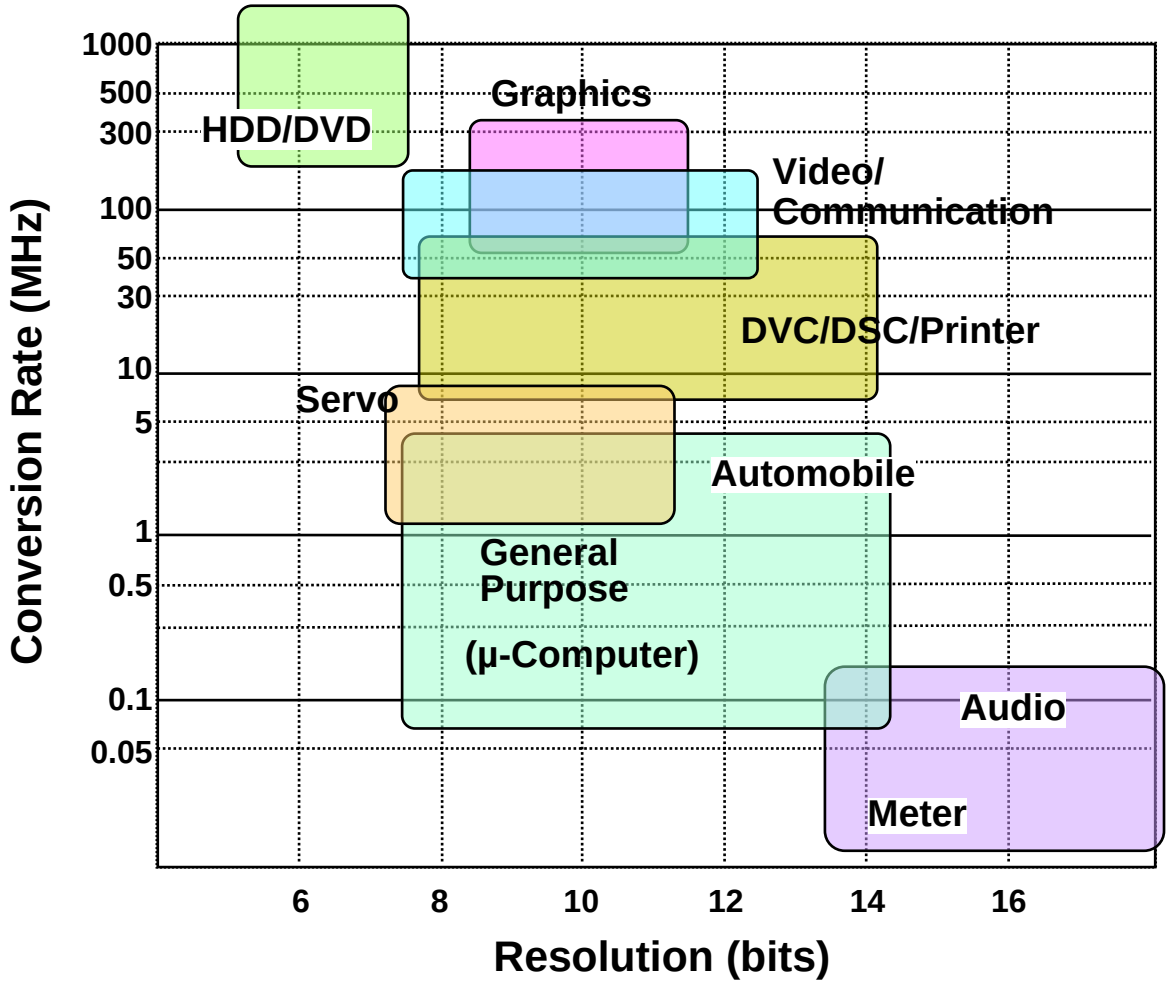
$$= \frac{Power}{2^{ENOB} \times f_s}$$

$$or \ = \frac{Power}{2^{ENOB} \times 2BW}$$



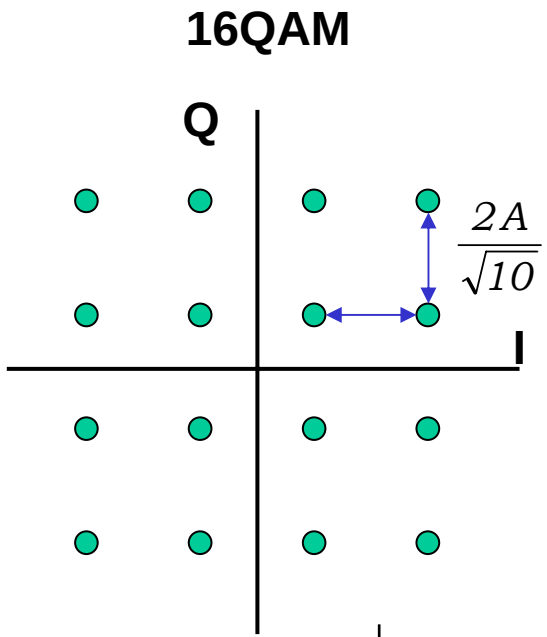
Performance and application

Needed resolution and conversion rate depending upon the application.



Needed SNR for certain BER in wireless system

Lower Bit Error Rate in the digital modulation needs higher SNR.

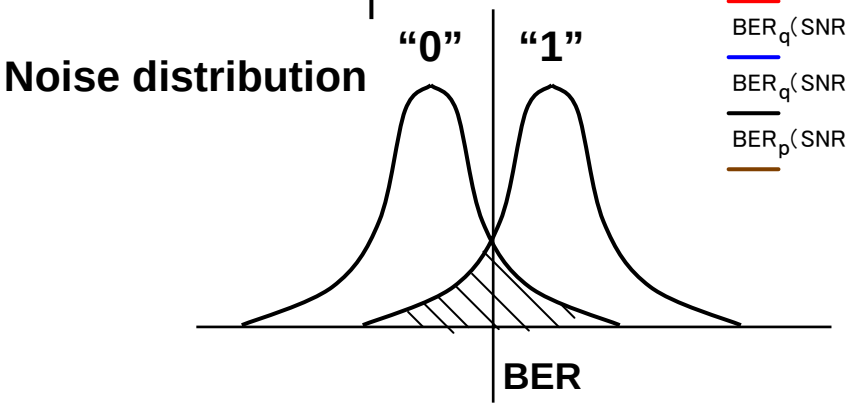


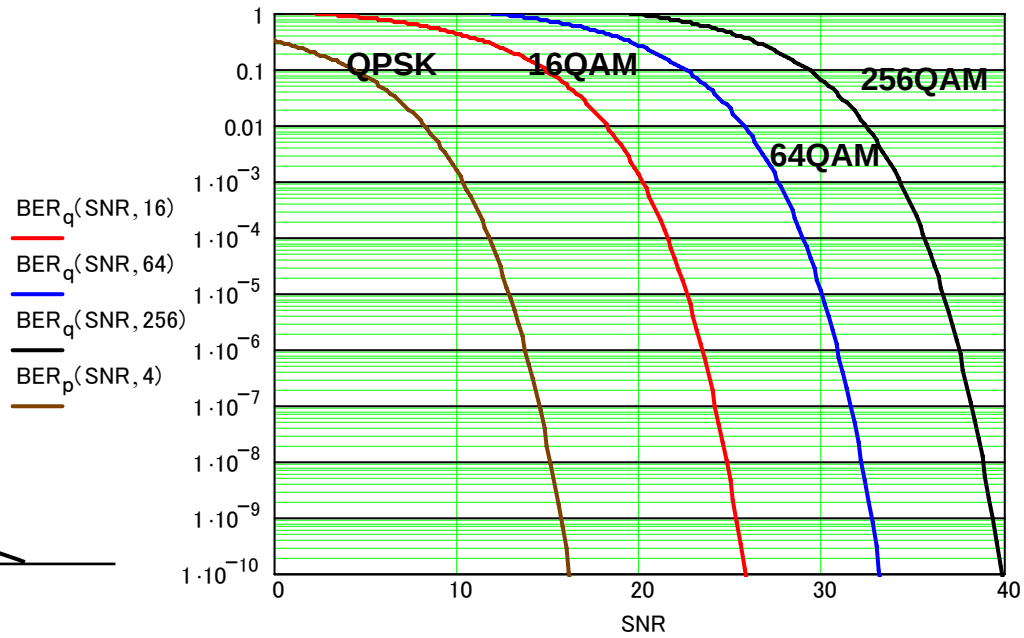
n-PSK

$$BER \approx erfc\left(\sqrt{SNR}\,\sin\frac{\pi}{n}\right)$$

n-QAM

$$BER \approx 2\left(1-\frac{1}{\sqrt{n}}\right)erfc\left(\frac{\sqrt{2\cdot SNR}}{2\left(\sqrt{n}-1\right)}\right)$$

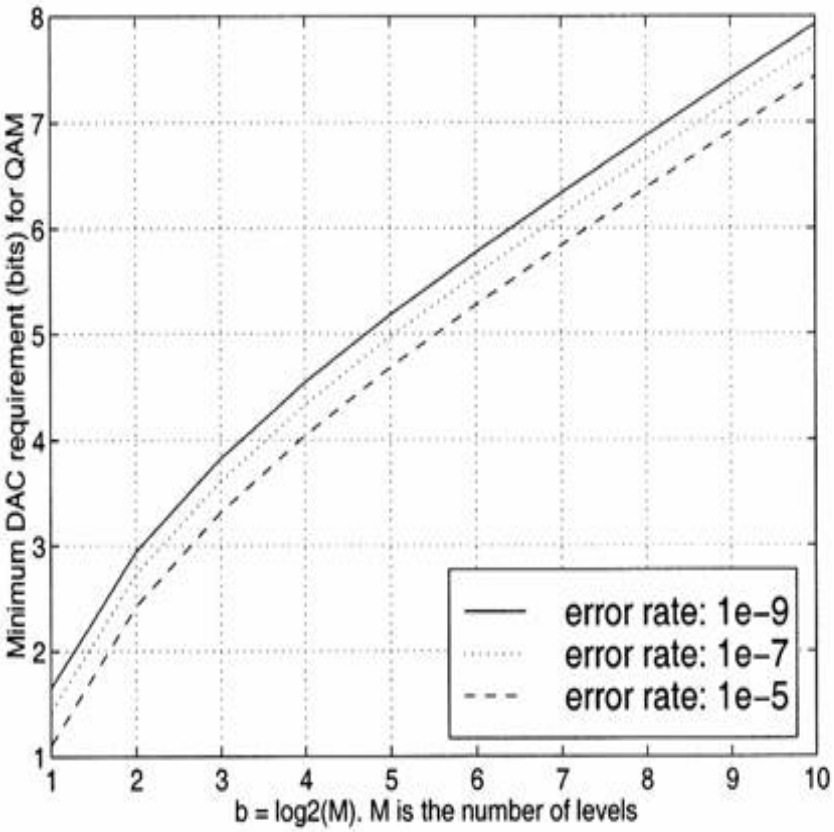




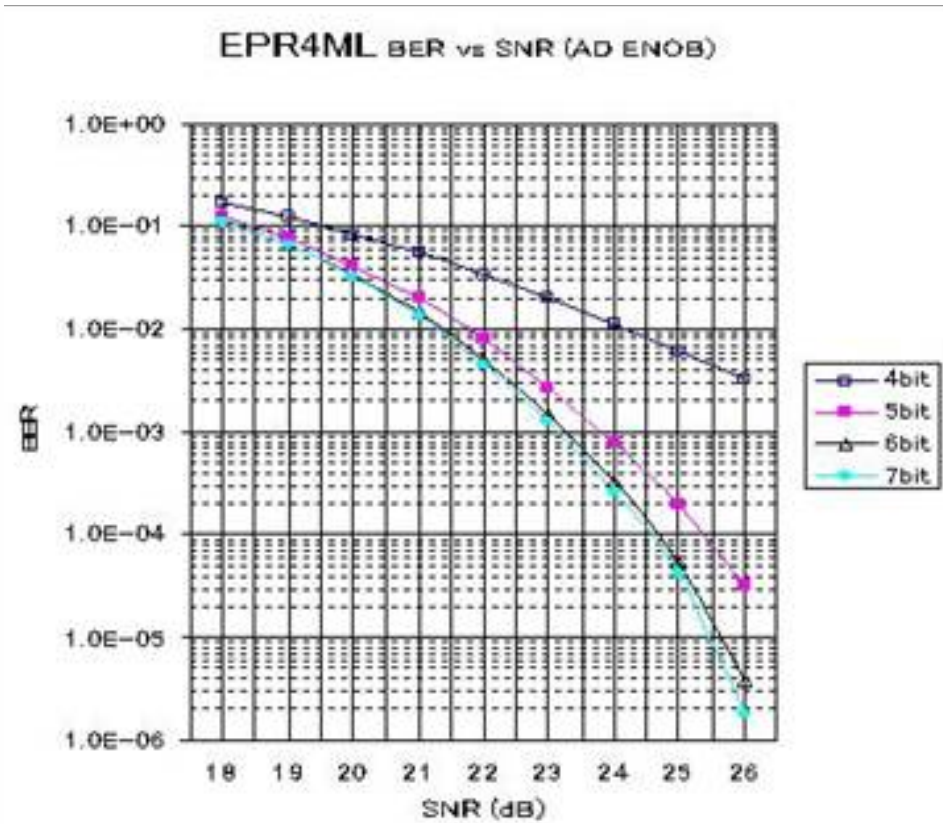
BER requirement

The lower the bit error rate the higher the required ADC/DAC resolution.

Resolution (quantization noise) affects BER.



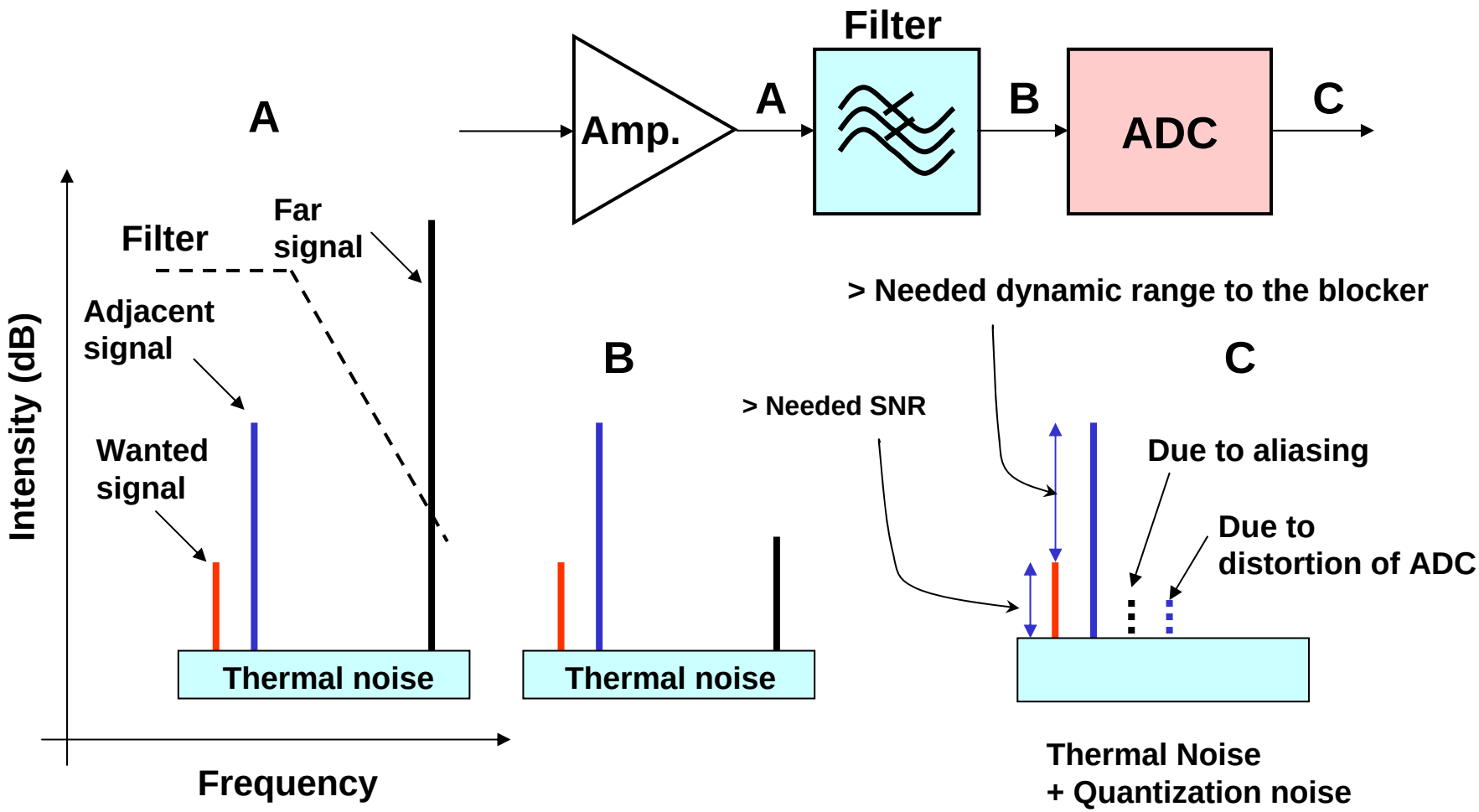
DAC requirement for QAM



ADC requirement for digital read-channel

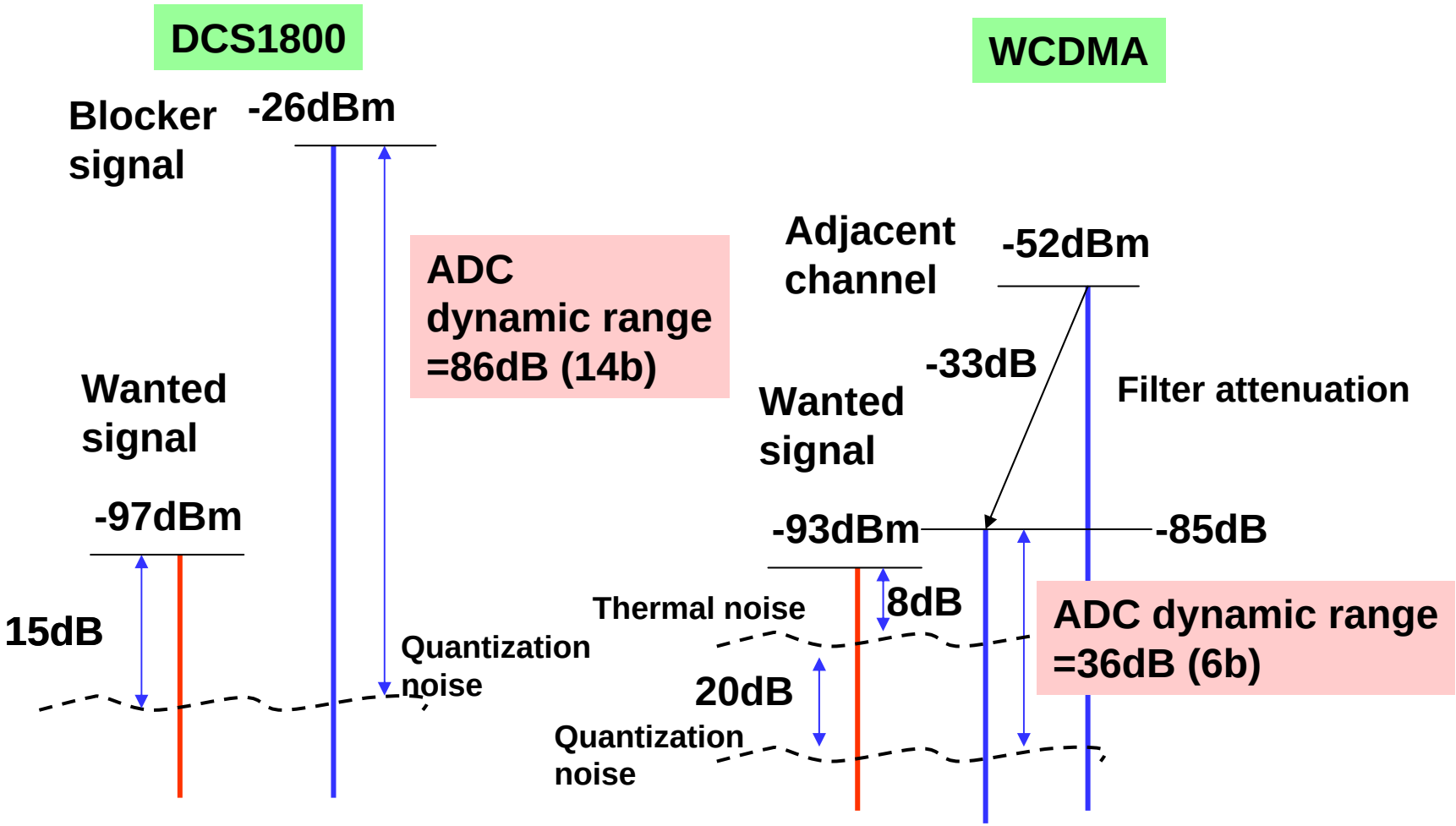
Signal intensity in wireless system

Wireless system has strong unwanted signals.
Also, electric circuits generate distortion and noise.



Needed ADC dynamic range

Existence of strong blockers results in the need for high dynamic range ADC.

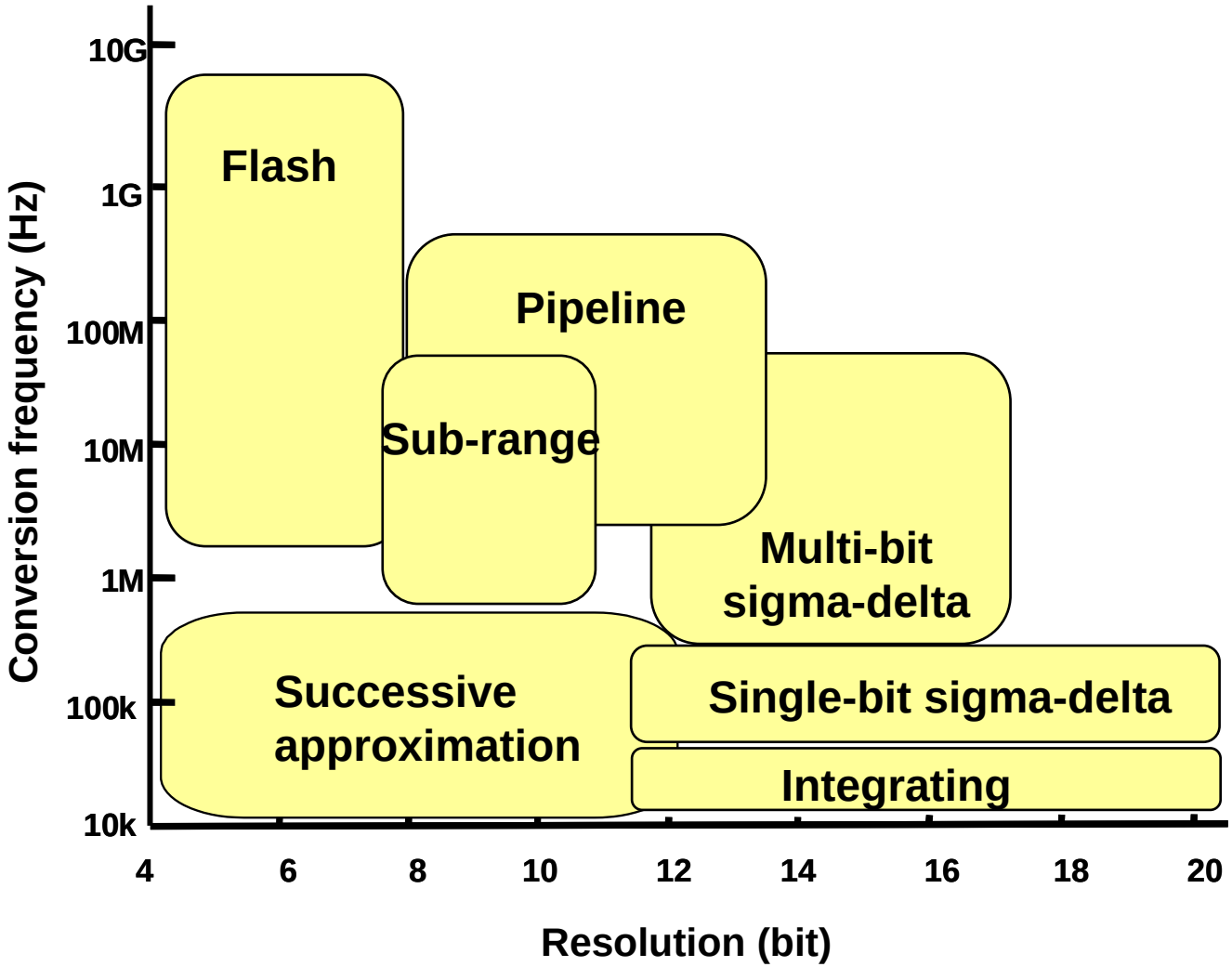


3. Overview of high-speed A/D converters

- **Performance and ADC architecture**
- **Integrating ADC**
- **Successive approximation ADC**
- **Flash ADC**
- **Sub-ranging ADC**
- **Interpolation method**
- **Folding ADC**
- **Pipelined ADC**

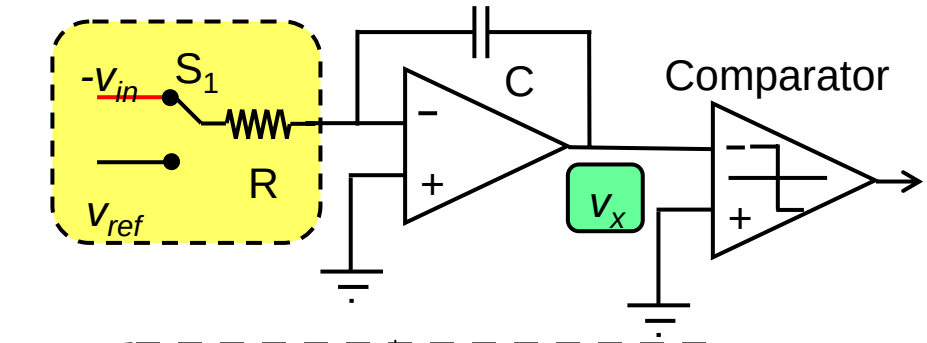
ADC performance and architectures

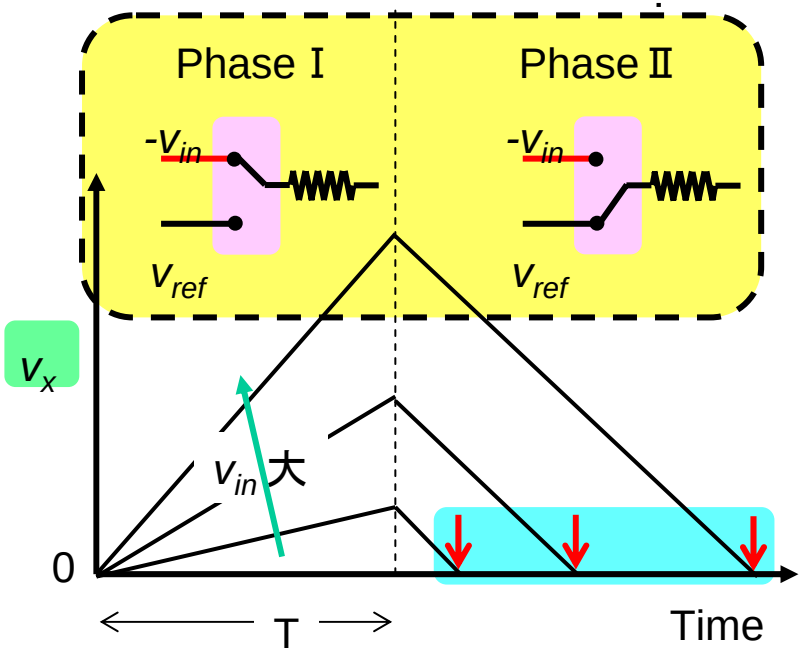
There are many conversion architectures with varying performance parameters.



Integrating ADC

Integrating ADC achieves high resolution, but at low speed.
Recently it has been used as column-ADC in CMOS imager.





Water clock

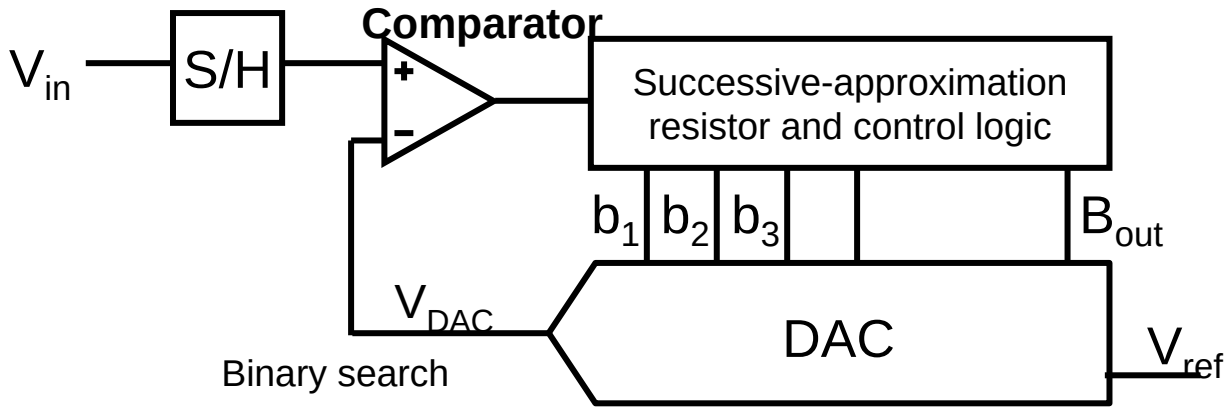
- **High resolution（20bit and more）**
- **Very low speed（DC measurement）**
- **Small DNL**
- **Can realize zero offset voltage**
- **Small analog elements and area**

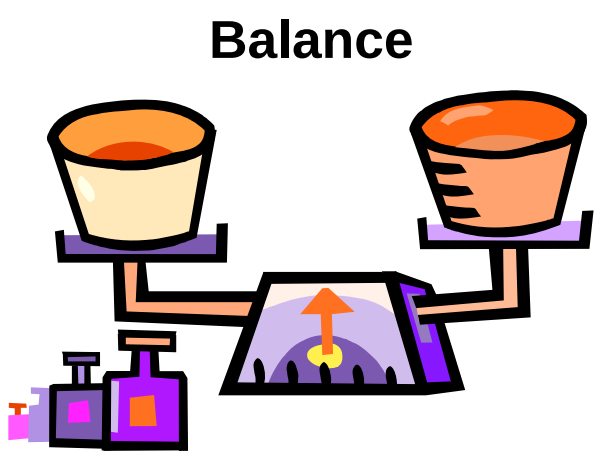
Going to 0 -> 1, when V_x becomes negative.

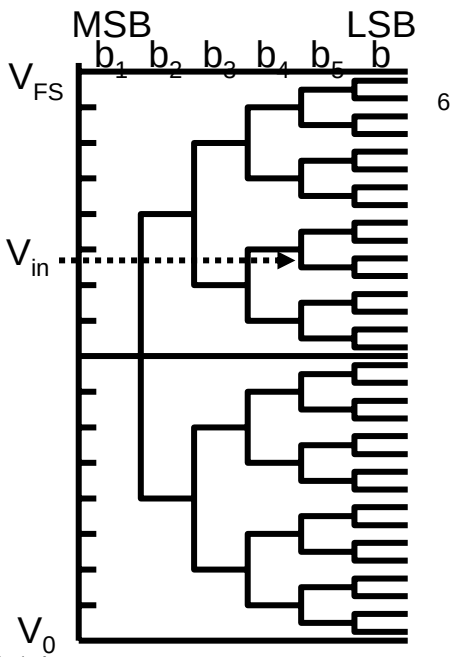
$$v_x(T) = -\int_0^T \frac{(-v_{in})}{RC} d\tau = \frac{v_{in}}{RC} T$$

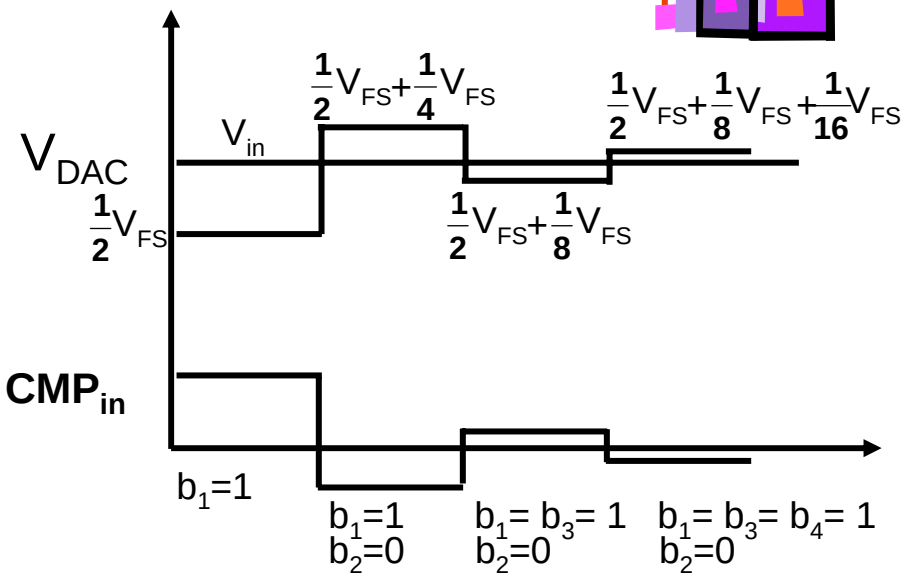
Successive-approximation ADC

Successive-approximation method is based on a binary search.





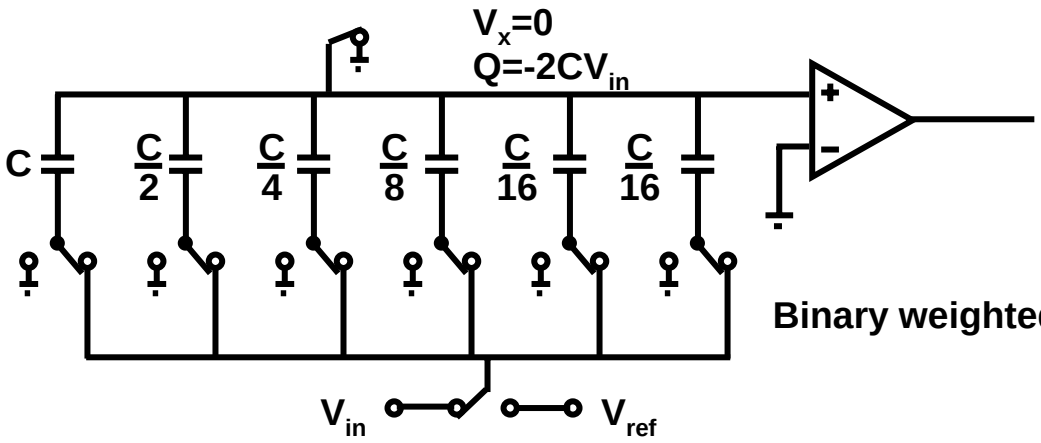




Charge-redistribution ADC

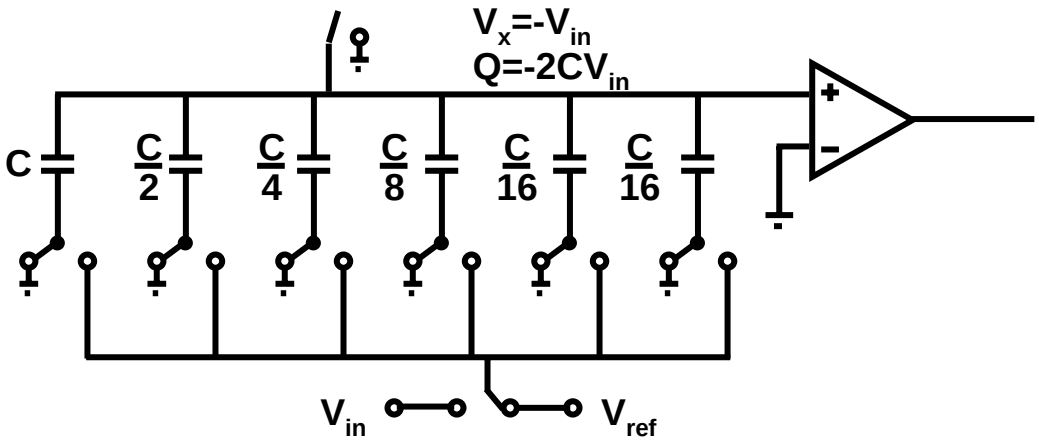
Charge-redistribution ADC draws attention as a suitable ADC in the nano-meter CMOS era. Because it needs no OP-Amp, but just needs capacitors and comparator.

1) Sampling



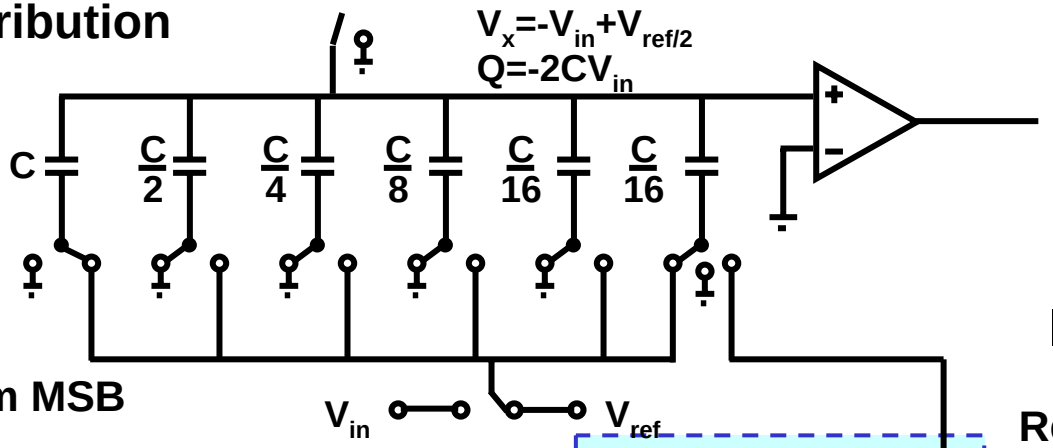
Binary weighted Capacitor array

2) Hold



Charge-redistribution ADC

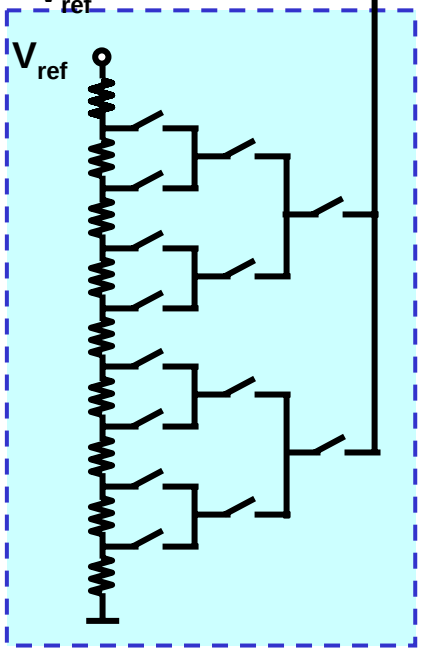
3) Charge redistribution



Determine from MSB

If needed

Resistor ladder for higher resolution

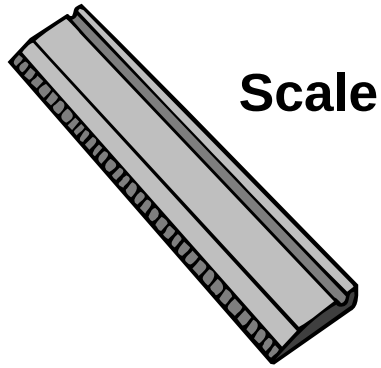


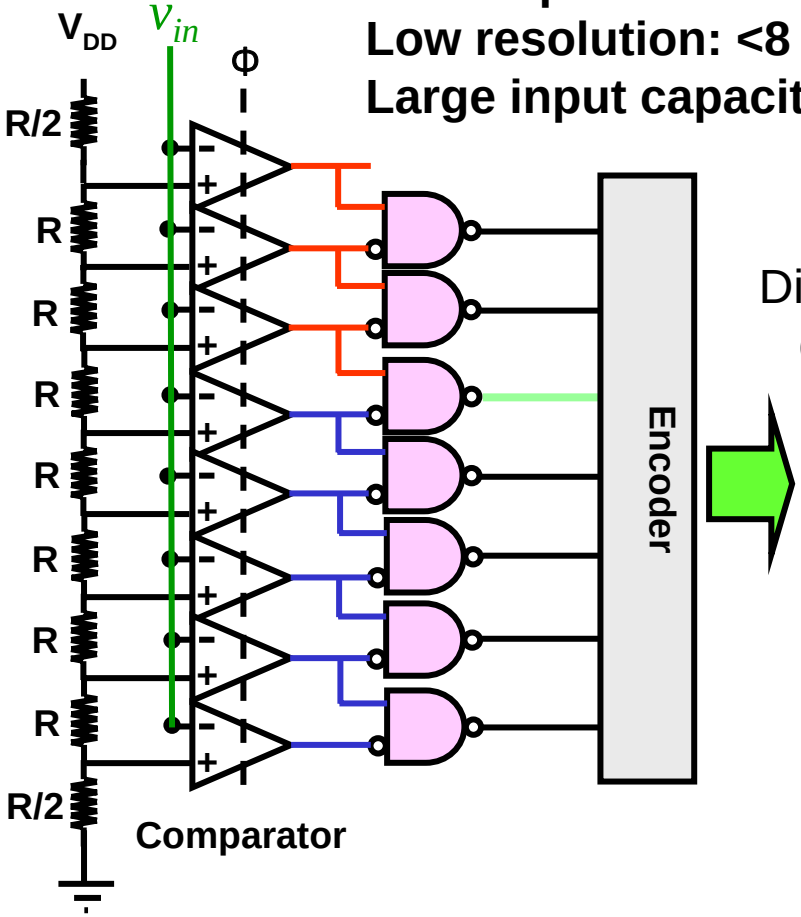
Higher resolution	**Easy calibration**
Ultra low power	**No OP amp**
Low conversion rate	**Needs multi clock**

Flash ADC

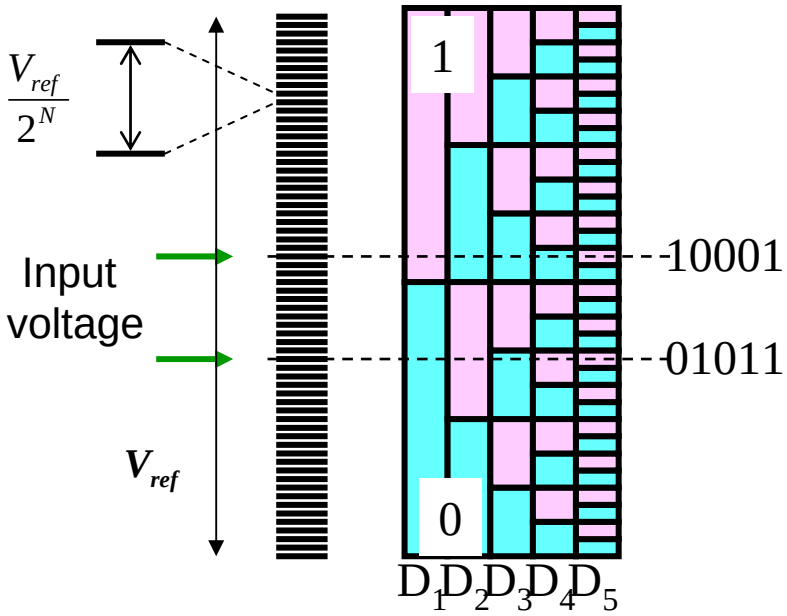
Flash ADC is very fast, but area and power increase exponentially with resolution.

Ultra fast operation: Several GHz
No sample and hold
Low resolution: <8 bit
Large input capacitance → difficult to drive





Digital out

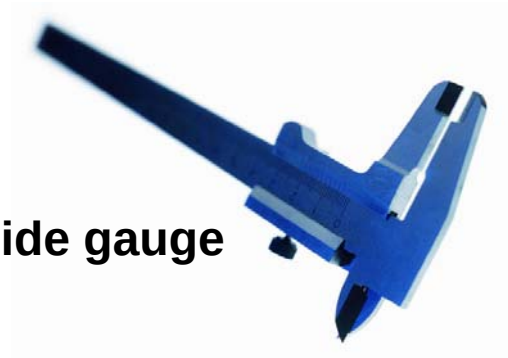


Sub-ranging ADC

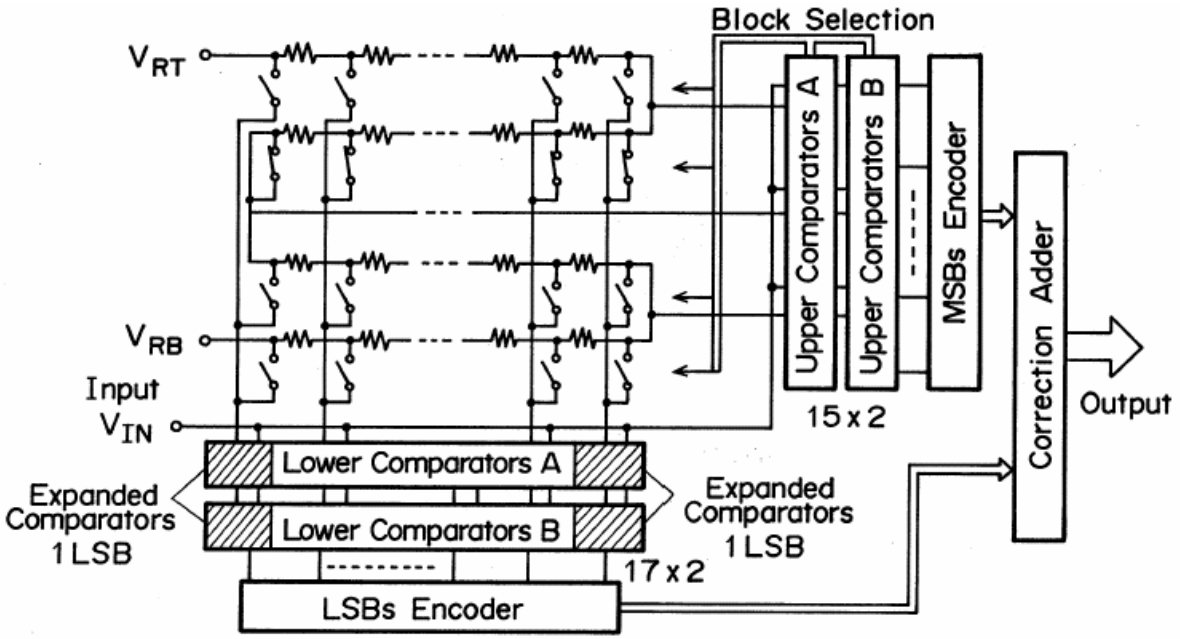
Multi-step conversion can reduce the # of comparators.
However, it needs high precision comparators.
As a result, small power and area.

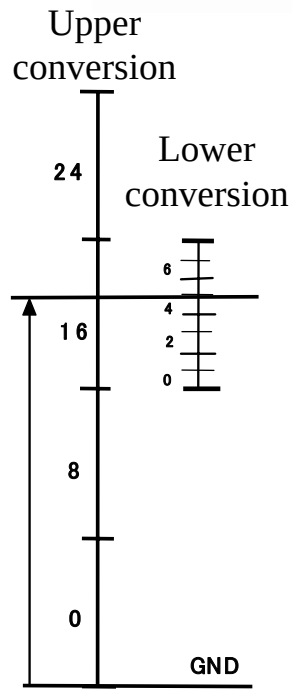
$$10bits:\ Flash;\ 2^N - 1 = 1023$$

$$two\,step;\ 2\left(2^{\frac{N}{2}} - 1\right) = 62$$



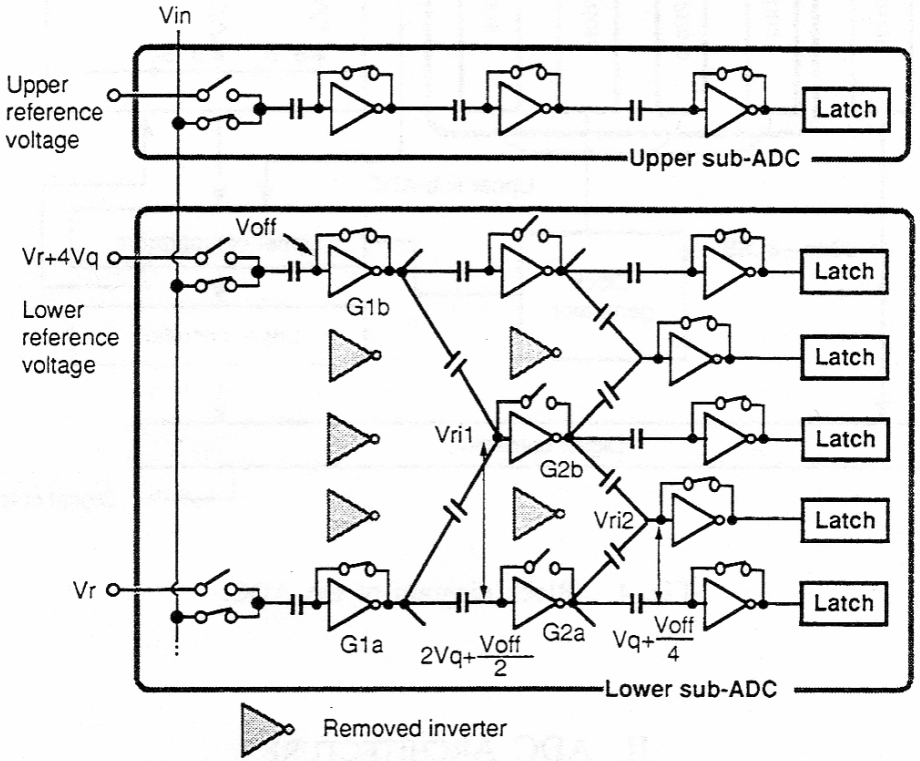
Slide gauge



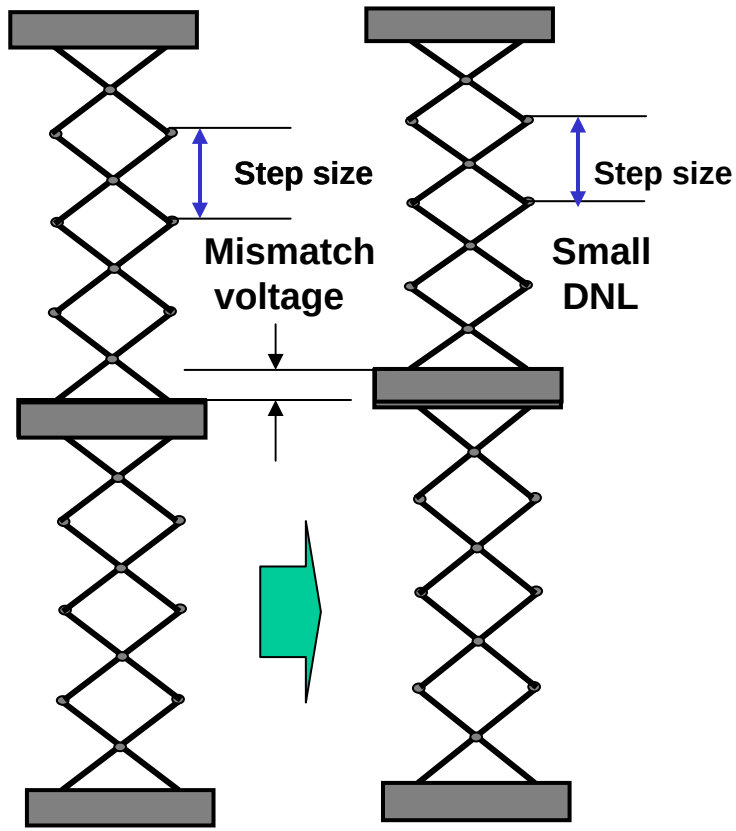


Interpolation method

Interpolation can generate accurate intermediate references which are between two references. Thus step sizes are almost equal, even though mismatch voltages are large.



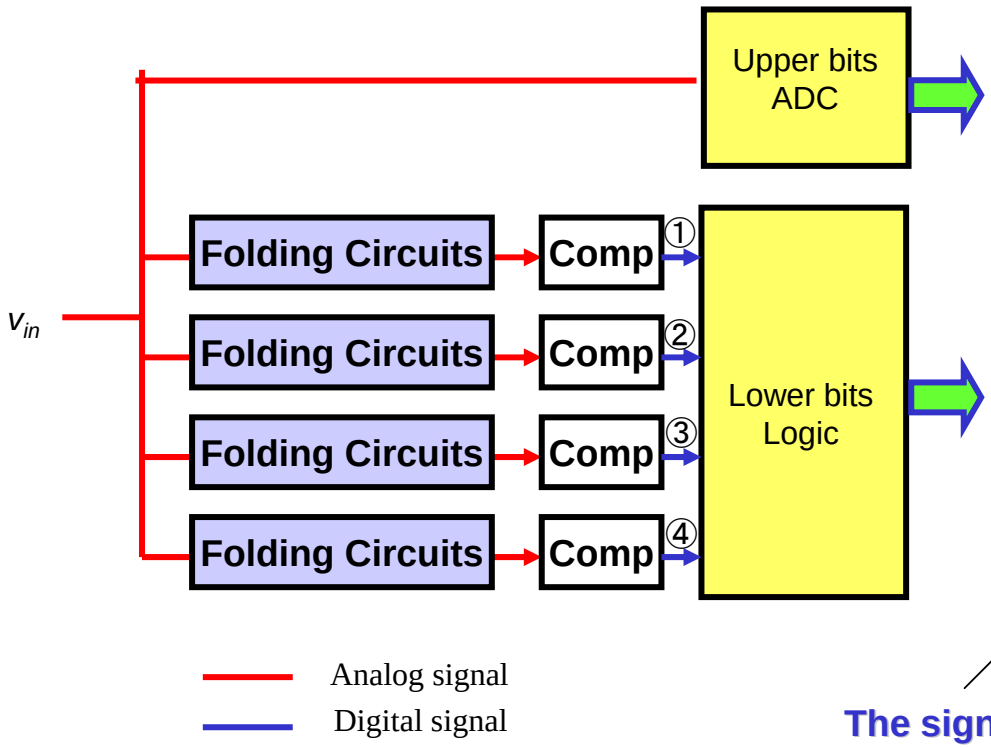
K. Kusumoto and A. Matsuzawa
JSC, pp. 1200-1206, 1993.

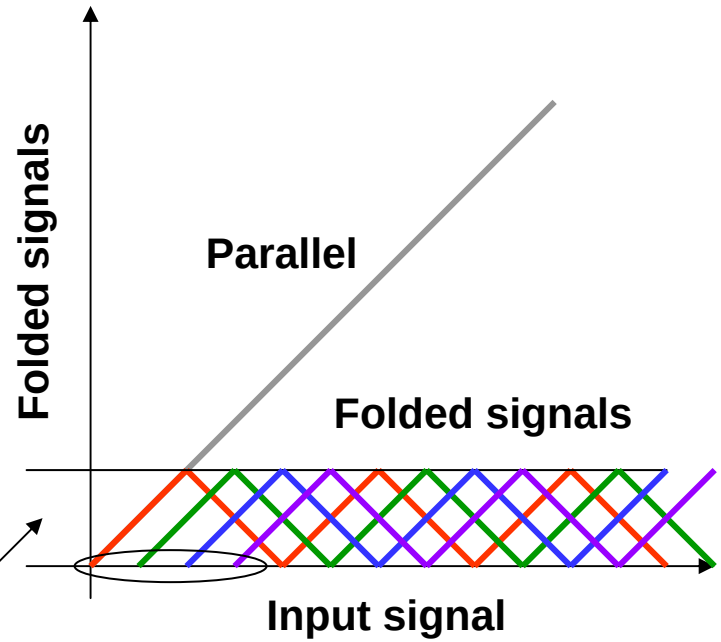


Folding ADC

Input signal is folded to the compressed signals of which phases are different.
Lower bits are obtained by comparing between these folded signals.

Low power and small size, yet still high speed.
However, not suitable for higher resolution. <10bit

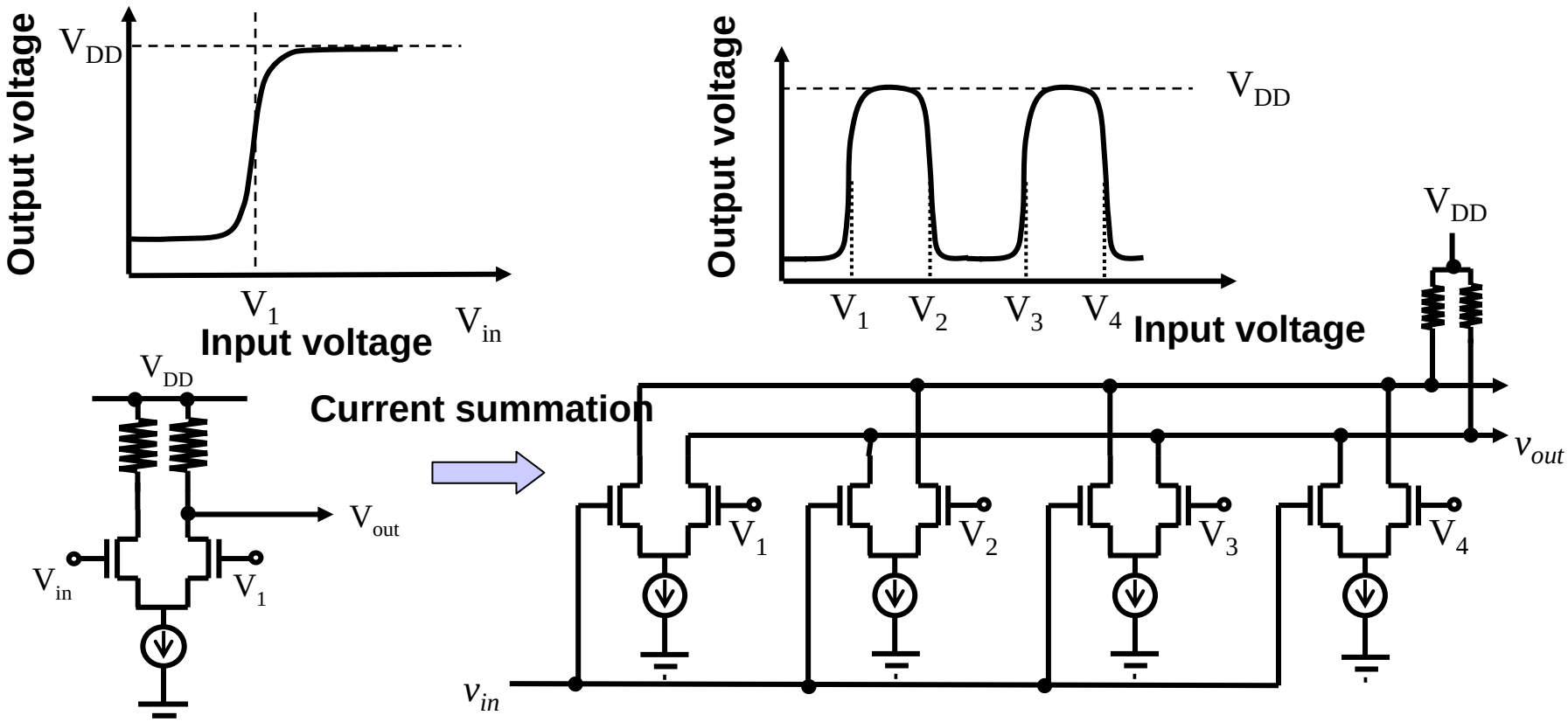




The signal is compressed
→The # of comparators can be reduced

Folding circuits

Composing the folding characteristics by the summation of currents from differential transistor pairs.



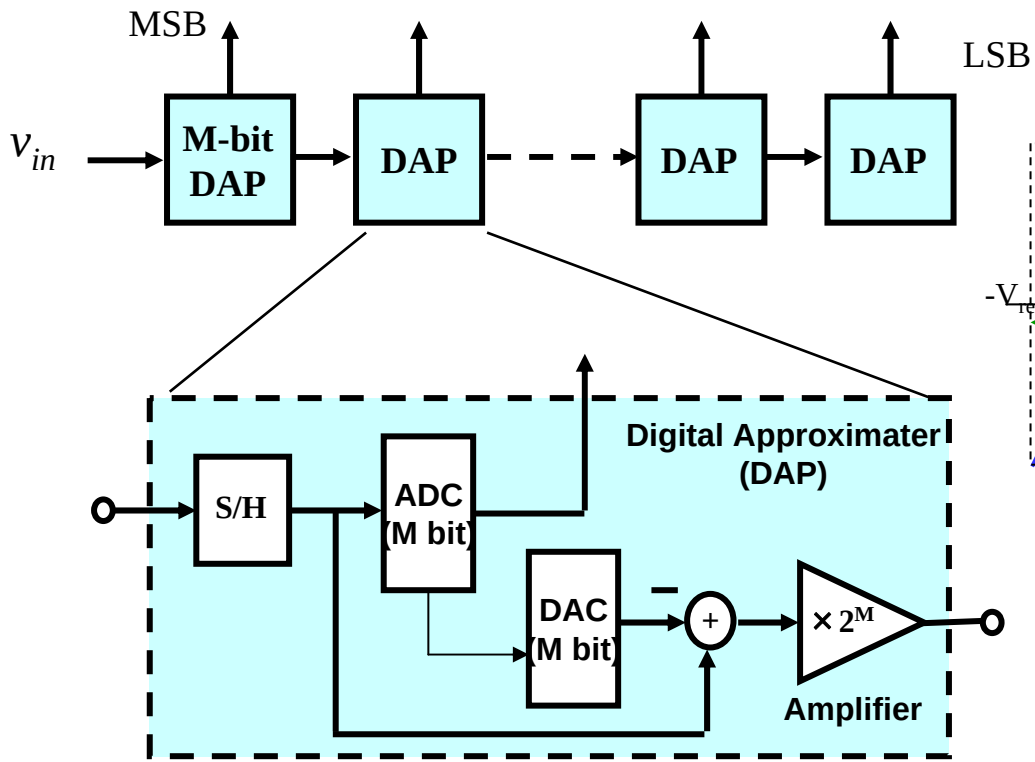
Pipelined ADC

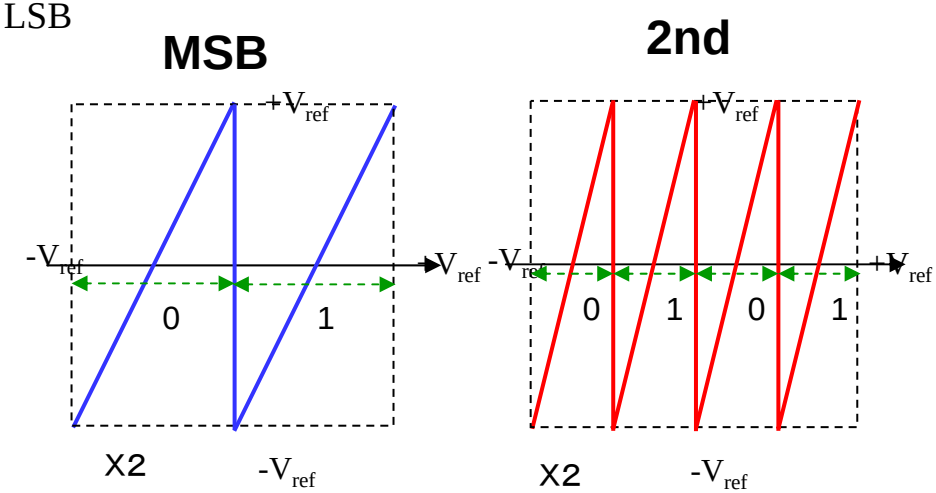
Pipelined ADC is the centerpiece of embedded ADCs for many applications, such as digital cameras, digital TVs, ADSLs, VDSLs, and wireless LANs.

Suitable for CMOS

Switched capacitor operation

High resolution(<15bit)
Moderate speed(<200MHz)
Low power consumption

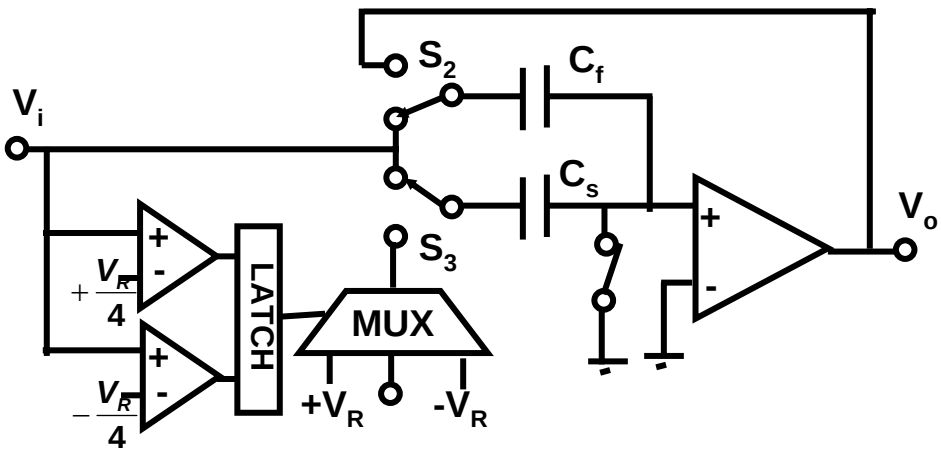




Conventional M is 1 or 1.5

1.5-bit/stage Pipeline ADC

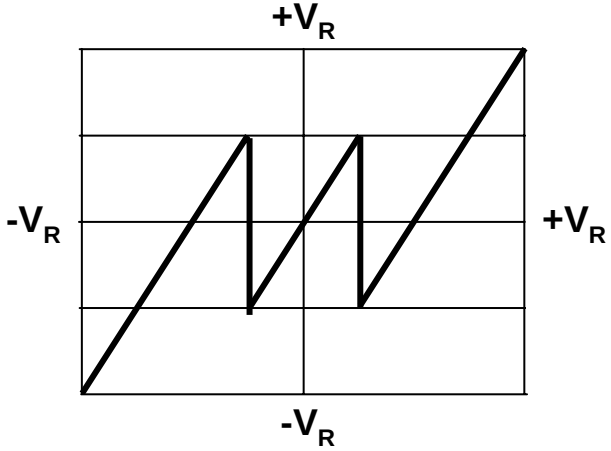
Amplification at each stage reduces the input referred thermal noise.
1.5b/stage architecture reduces the requirement for the comparator offset drastically.



SUB-ADC **DAC** **2X GAIN**

Unit conversion stage for 1.5-bit/stage pipeline ADC

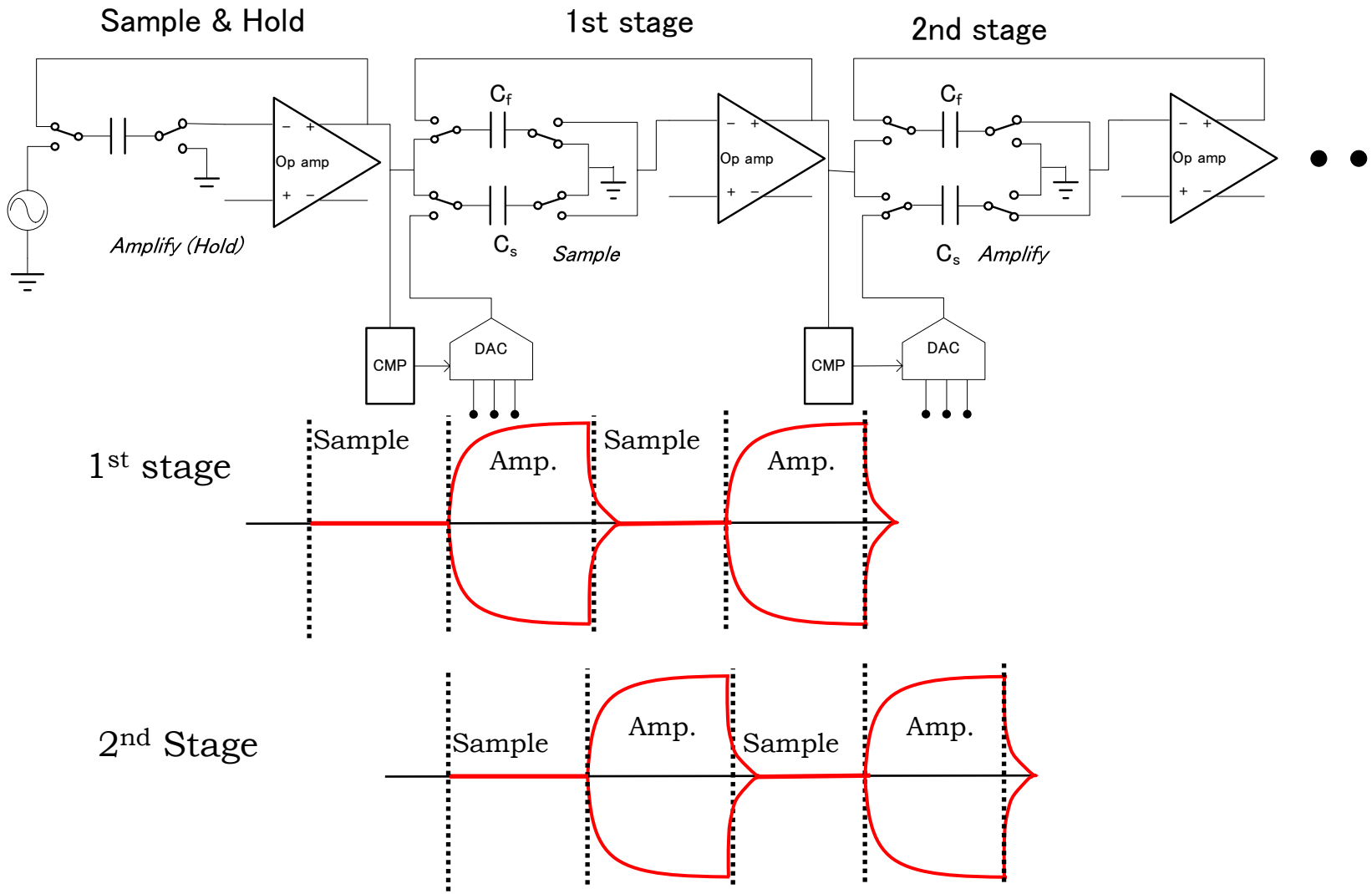
Transfer characteristics



$$V_o = \begin{cases} \left(1+\frac{C_s}{C_f}\right)V_i + \frac{C_i}{C_f}V_{ref} & \text{if} \quad Vi < -\frac{V_{ref}}{4} \\ \left(1+\frac{C_s}{C_f}\right)V_i & \text{if} \quad -\frac{V_{ref}}{4} \le V_i \le \frac{V_{ref}}{4} \\ \left(1+\frac{C_s}{C_f}\right)V_i - \frac{C_i}{C_f}V_{ref} & \text{if} \quad V_i > \frac{V_{ref}}{4} \end{cases}$$

Pipelining

Pipeline action relaxes settling time requirement.



4. Overview of high-speed D/A converters

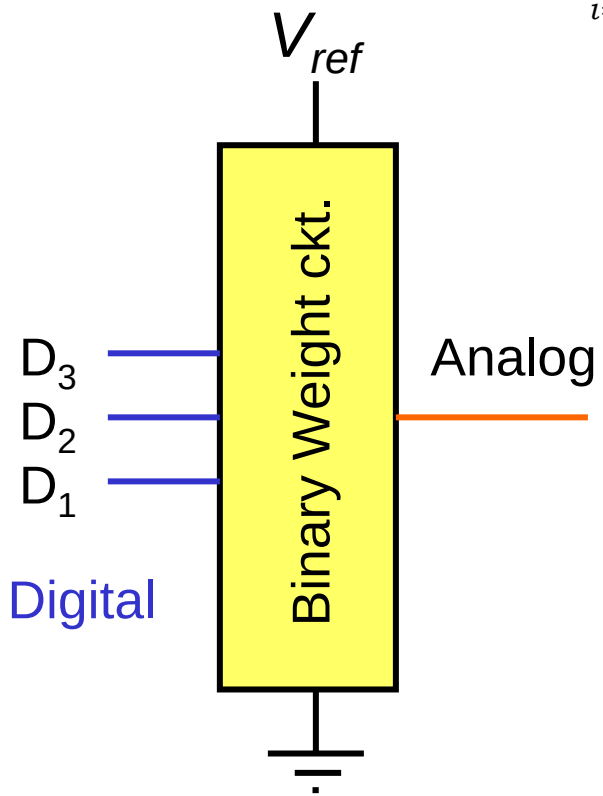
- **Basic two concepts of DAC**
- **Binary method**
  - **R-2R based DAC**
  - **Capacitor array DAC**
- **Decoder method**
  - **Resistor string DAC**
  - **Current steering DAC**

Basic two concepts of DAC

1. Binary method

Not small DNL
Large glitch
Small area

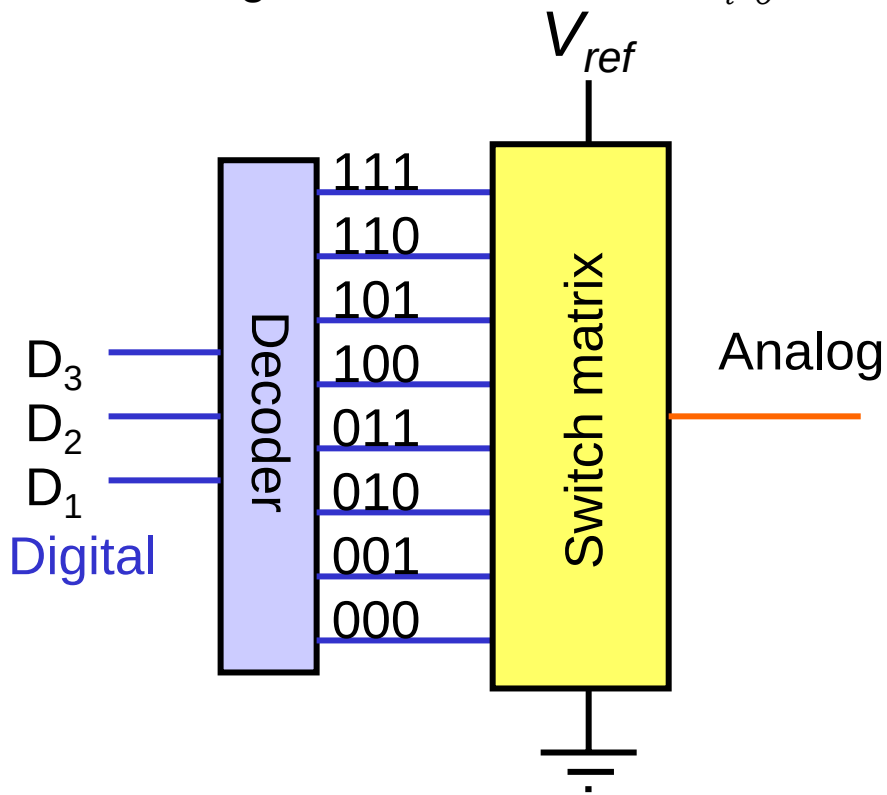
$$V_{analg} = V_{ref} \sum_{i=1}^{N} \frac{1}{2^i} \cdot D_i$$



2. Decoder method

Small DNL
Small glitch
Large area

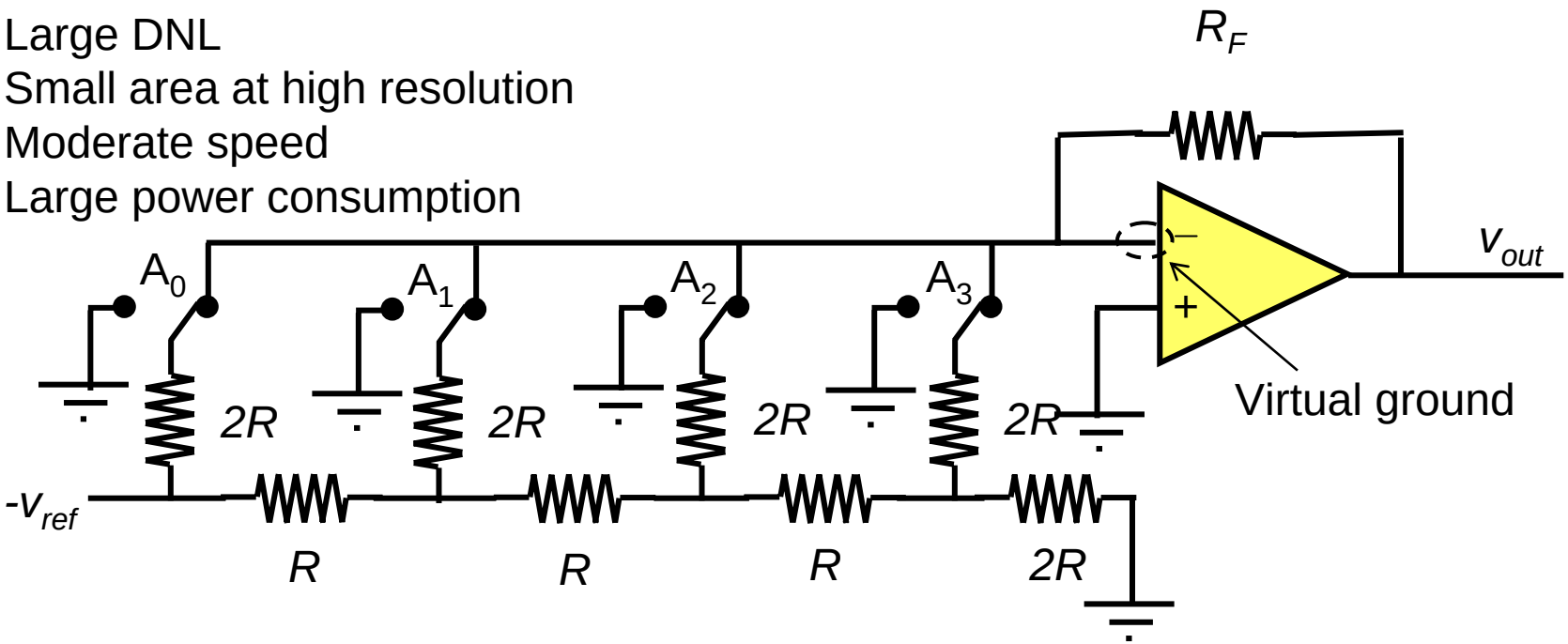
$$V_{analg} = V_q \cdot \sum_{i=0}^{N-1} 2^i \cdot D_i$$



R-2R based DAC

R-2R resistor ladder can generate binary weighted current easily.

Resolution: 12b
Large DNL
Small area at high resolution
Moderate speed
Large power consumption



$$v_{out} = R_F\left(I_r \cdot A_0 + \frac{I_r}{2} \cdot A_1 + \frac{I_r}{2^2} \cdot A_1 + \frac{I_r}{2^3} \cdot A_1 \right)$$

$$I_r = \frac{v_{ref}}{2R}$$

Capacitor array DAC

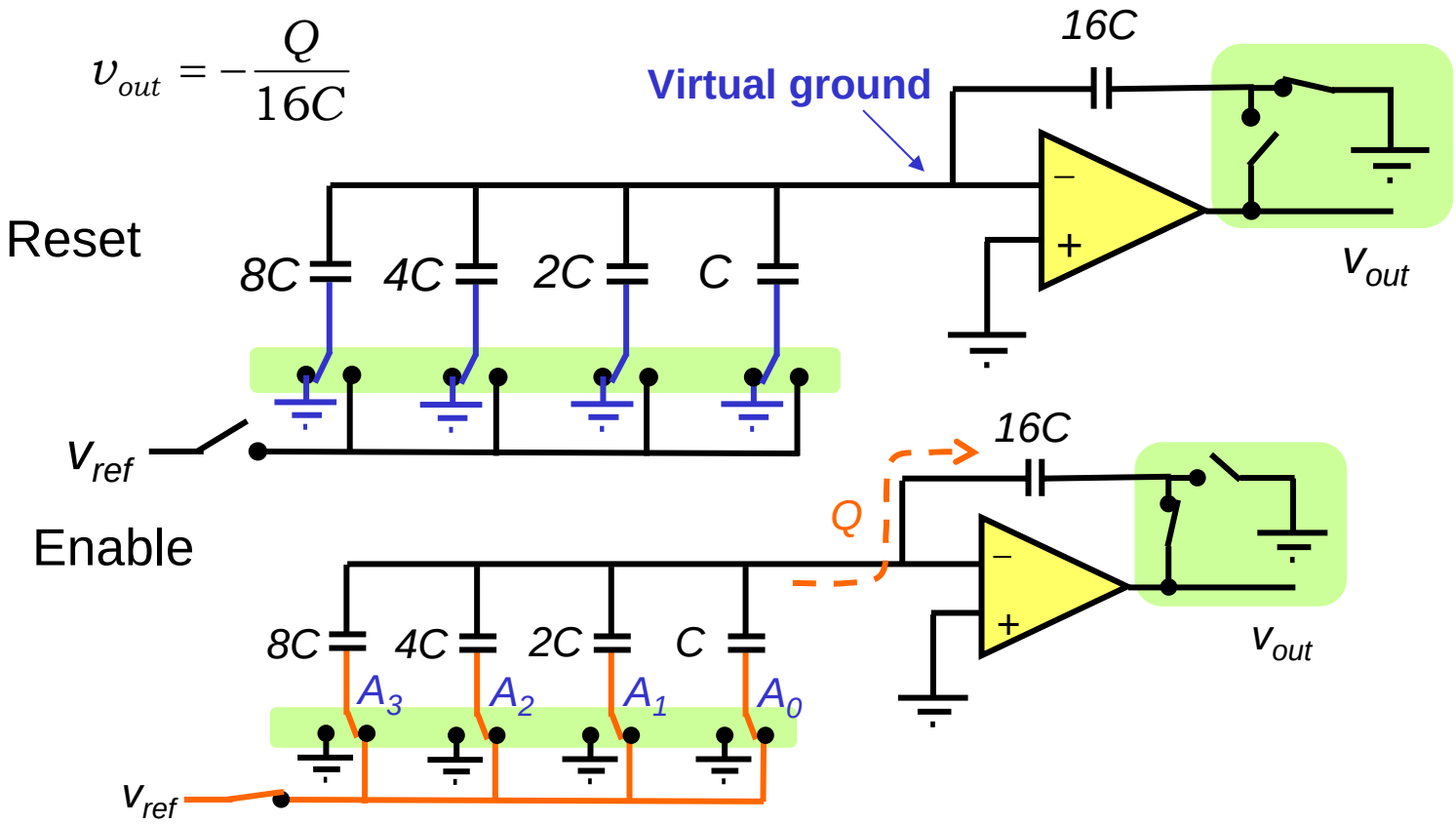
Capacitor array DAC is widely used in CMOS technology.

Low power and no sample & Hold

$$Q = v_{ref}\left[C \cdot A_0 + 2C \cdot A_1 + 4C \cdot A_2 + 8C \cdot A_3\right]$$

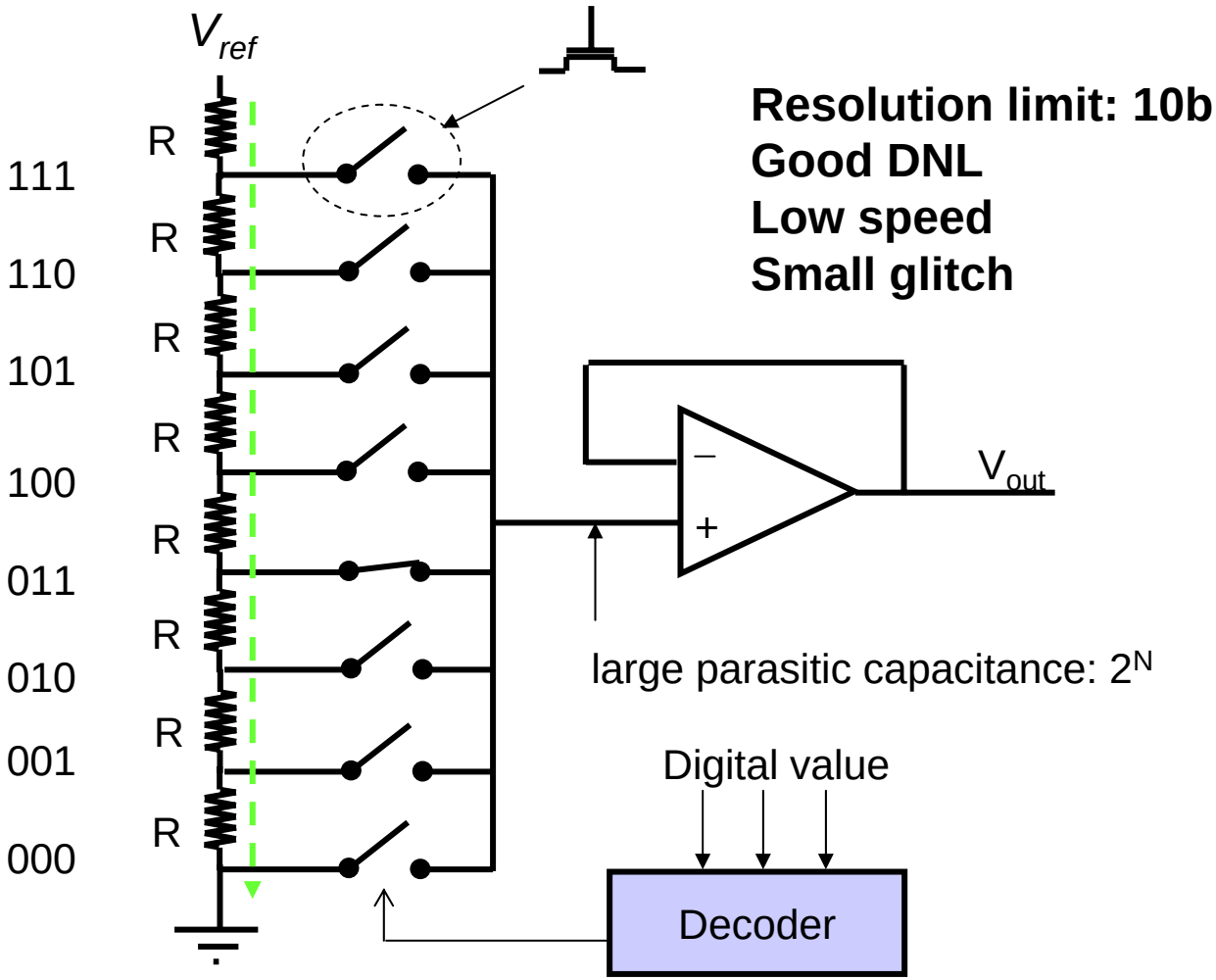
A_i= 0 or 1

$$v_{out} = -\frac{Q}{16C}$$



Resistor string DAC

Decoder method can realizes small DNL, however needs large area at high resolution.



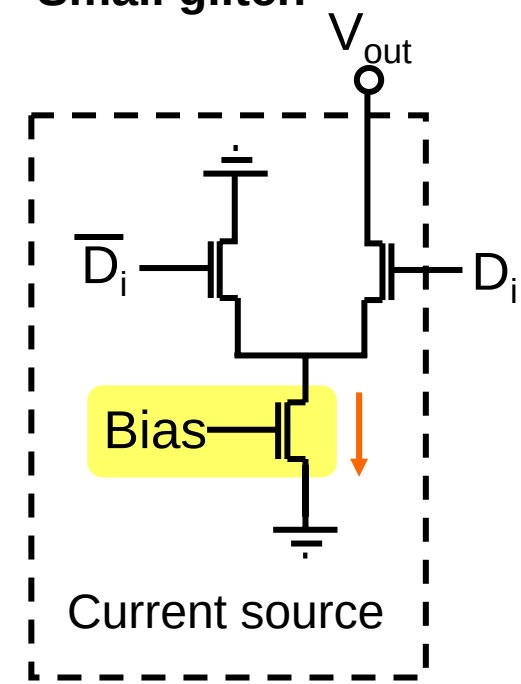
Resolution limit: 10b
Good DNL
Low speed
Small glitch

Current steering DAC

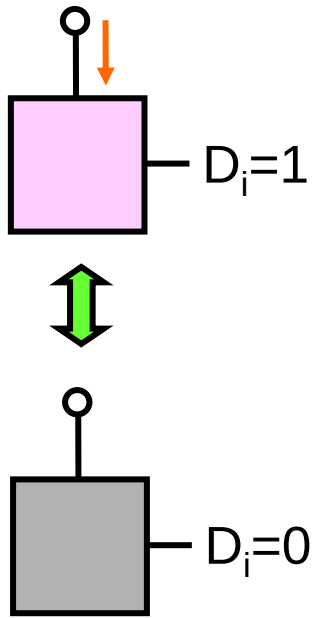
Widely used for high speed DAC. **Graphics, communications, etc.**

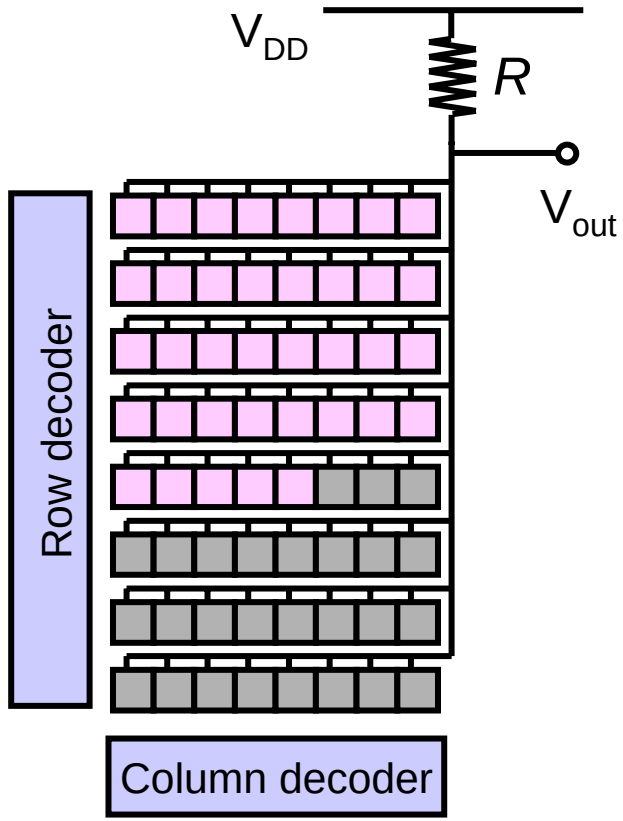
High speed, -- 1 GHz
Resolution – 14 b
Small DNL
Small glitch

Conventionally large area



Current cell with switch



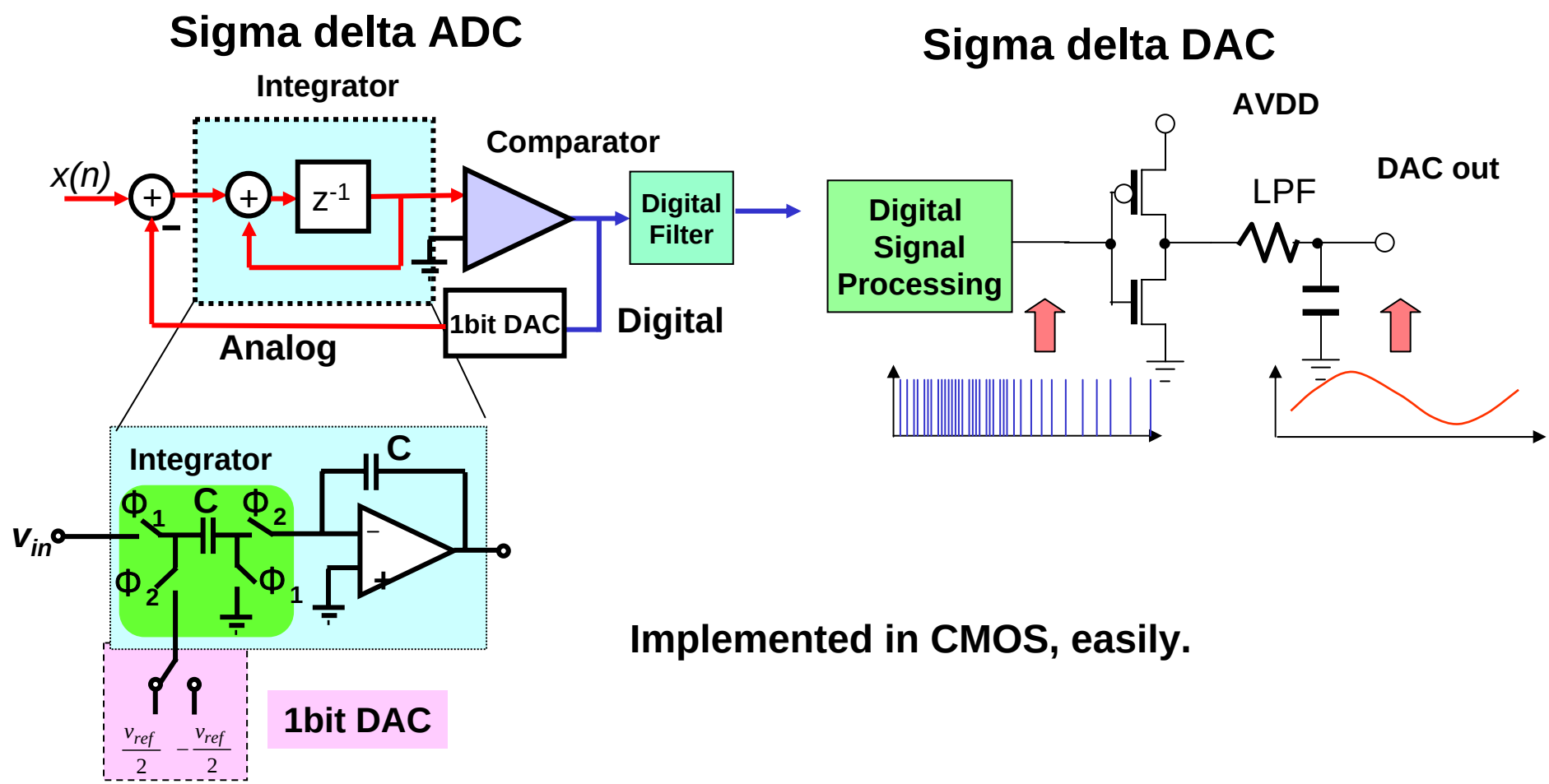


5. Overview of over-sampling sigma-delta data converters

- **Sigma-delta modulation method**
  - **Over sampling**
  - **Noise shaping**
  - **Sigma-delta modulator**
  - **SNR**
  - **Higher order system**
  - **Feed forward and feed back compensation**
  - **MASH (Multi-stage noise shaping)**

Sigma-delta ADC, DAC

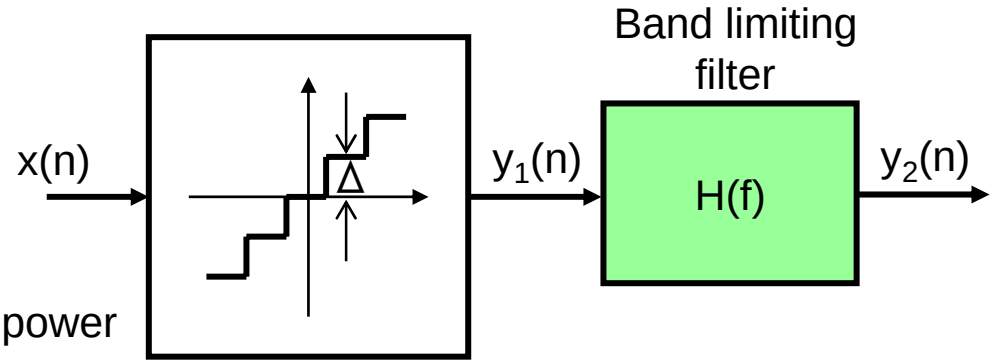
Sigma delta ADC and DAC are widely used in high resolution (14b-24b) and not high speed (<1MHz) applications.



Implemented in CMOS, easily.

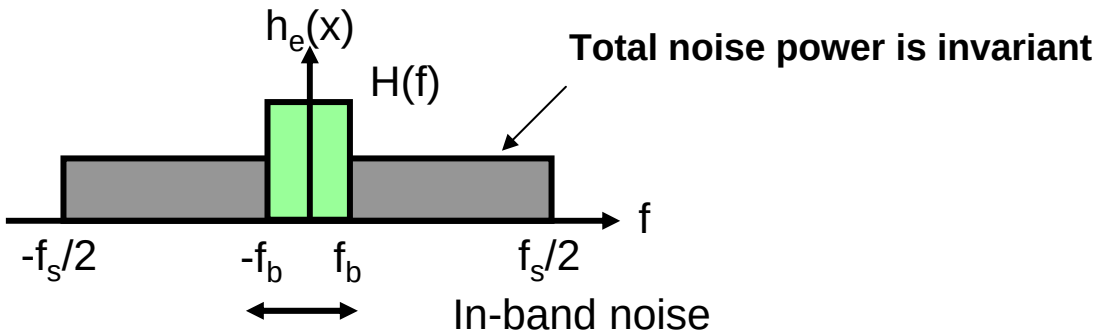
Over sampling

Over sampling can reduce effective quantization noise.



Quantization noise power

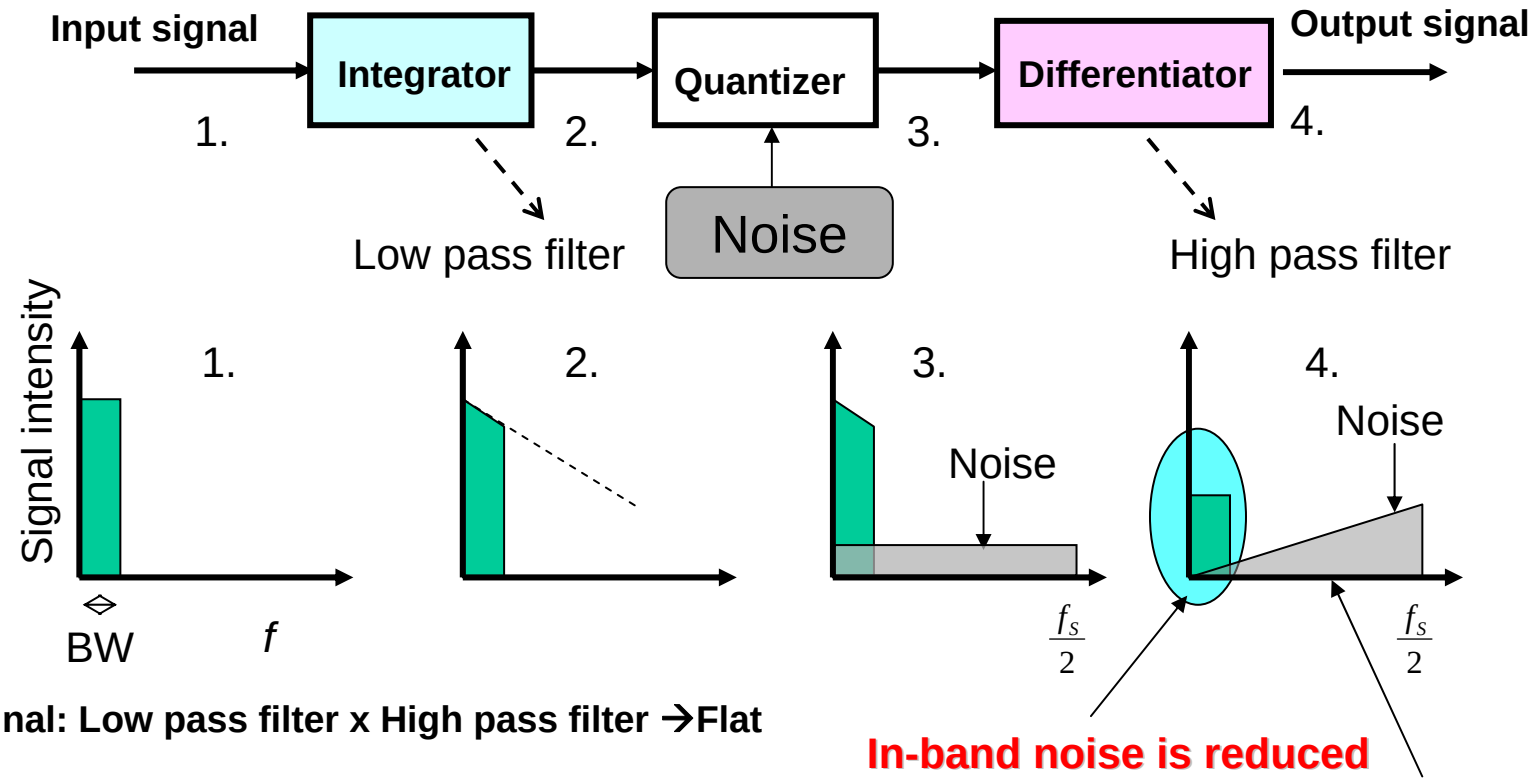
$$P_e = \int_{-f_s/2}^{f_s/2} S_e^2(f)\left|H(f)\right|^2 df = \int_{-f_b}^{f_b} \frac{\Delta^2}{12}\cdot\frac{1}{f_s}\,df = \frac{\Delta^2}{12}\cdot\left(\frac{2f_b}{f_s}\right) = \frac{\Delta^2}{12}\cdot\frac{1}{OSR} \qquad OSR \equiv \frac{f_s}{2f_b}$$



Reduction of bandwidth by filter → Reduction of effective noise power

Noise shaping

Spectrum of quantization noise is shaped by differentiator.
In-band noise can be reduced.



Signal: Low pass filter x High pass filter →Flat

In-band noise is reduced

Quantization noise: High pass filter→ Lower in low frequency

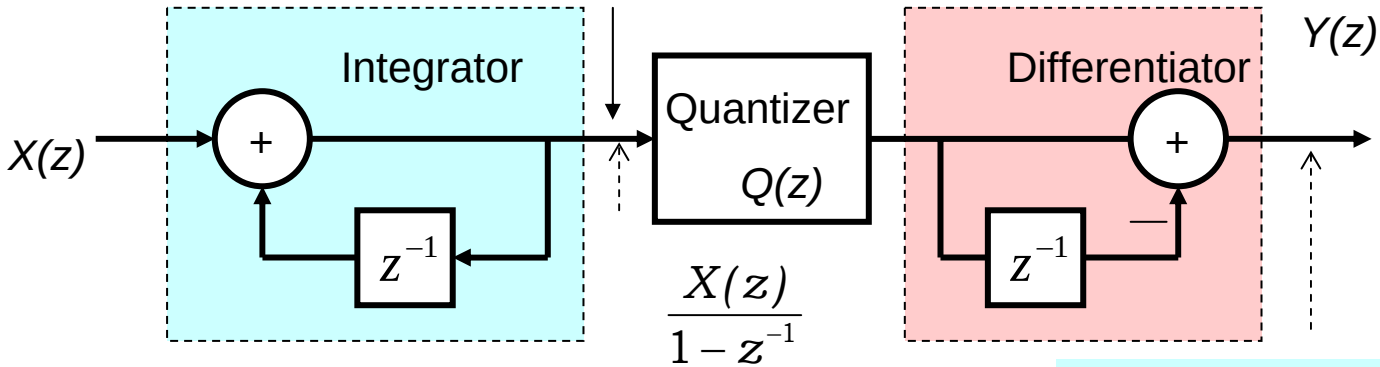
The spectrum of the quantization noise increases with frequency increase.

Only quantization noise is shaped in frequency characteristics

Sigma-delta modulator

Sigma-delta modulator shapes the frequency characteristics of the quantization noise

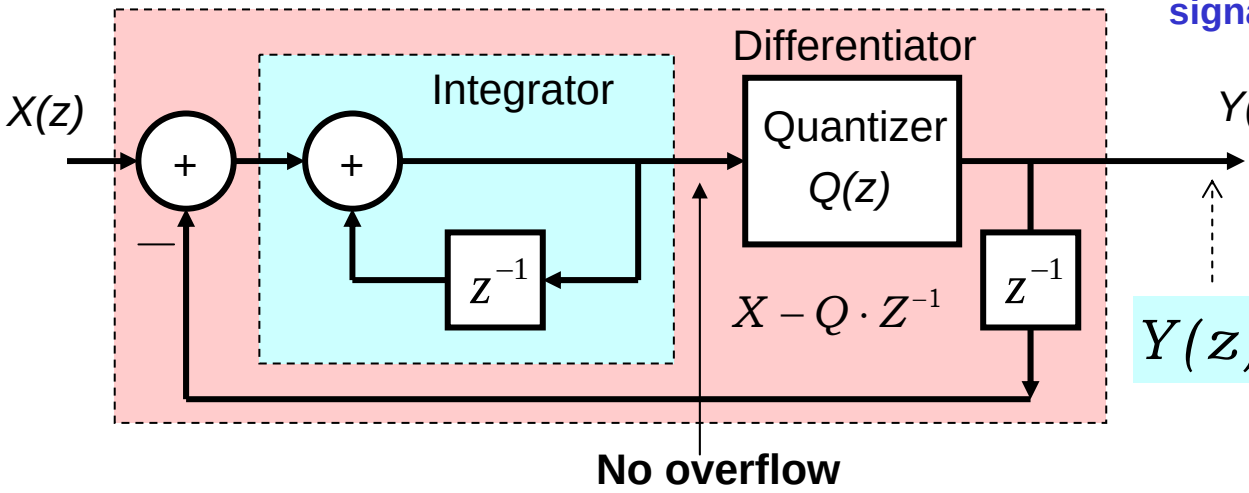
The signal will overflow



Equivalent transform

$$Y(z) = X(z) + (1 - z^{-1})Q(z)$$

Output signal **Input signal** **Quantization noise**



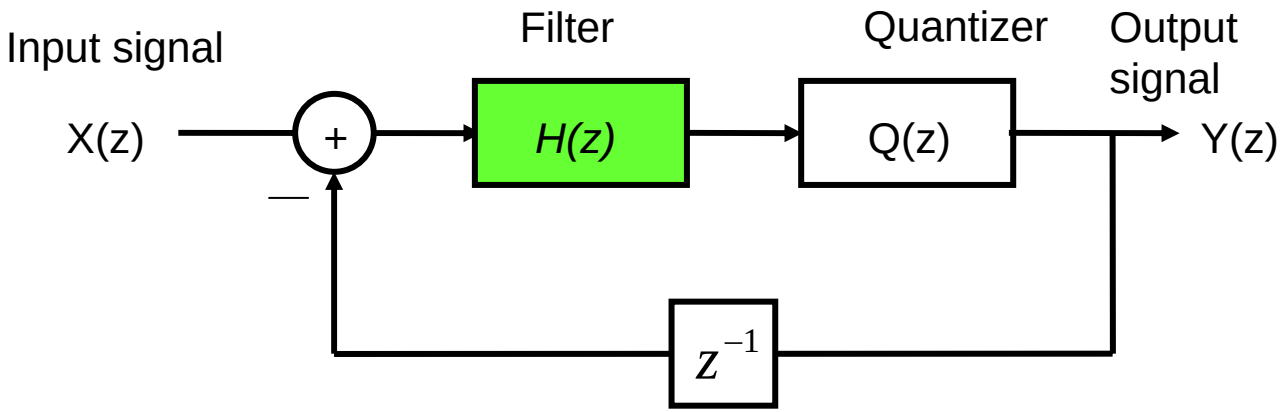
Differentiator (High pass filter)

$$Y(z) = X(z) + (1 - z^{-1})Q(z)$$

No overflow

Generic expression of sigma-delta modulator

We can use not only LPF but also BPF and complex BPF.
This gives us an excellent opportunity for wireless applications.



$$Y(z) = \frac{H(z)}{1 + H(z)z^{-1}} X(z) + \frac{1}{1 + H(z)z^{-1}} Q(z)$$

STF (Signal Transfer) **NTF (Noise transfer)**

Ex. $H(z) = \frac{1}{1 - z^{-1}}$ $STF(z) = 1,$ $NTF(z) = 1 - z^{-1}$

No filter **High pass filter**

Noise power in sigma-delta modulator

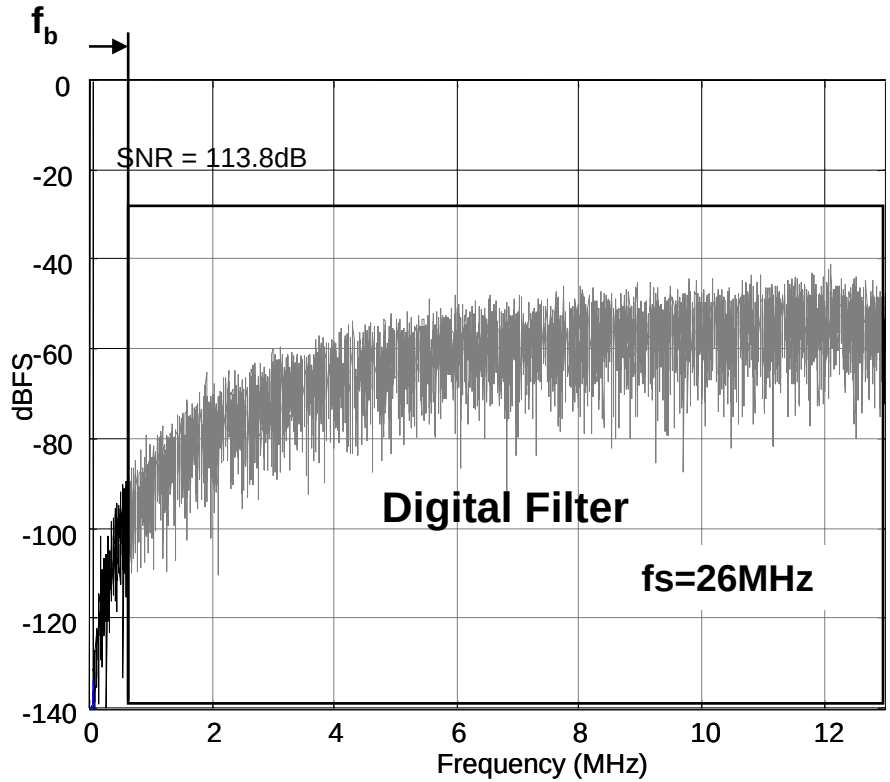
L^{th} order filter

$$Y(z) = X(z) + \left(1 - z^{-1}\right)^{L} Q(z)$$

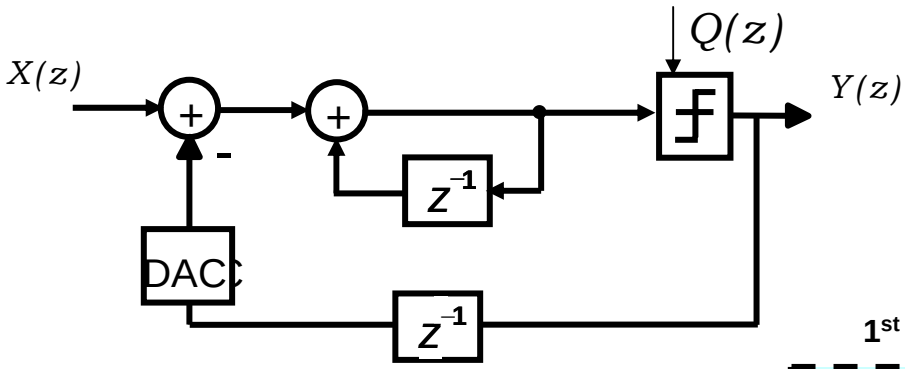
$$h_q^2(f) = \frac{\Delta^2}{12 f_s}$$

$$N_q = \int_{-f_b}^{+f_b} h_q^2(f) \left|1 - z^{-1}\right|^{2L}_{z=e^{j2\pi f/fs}}$$

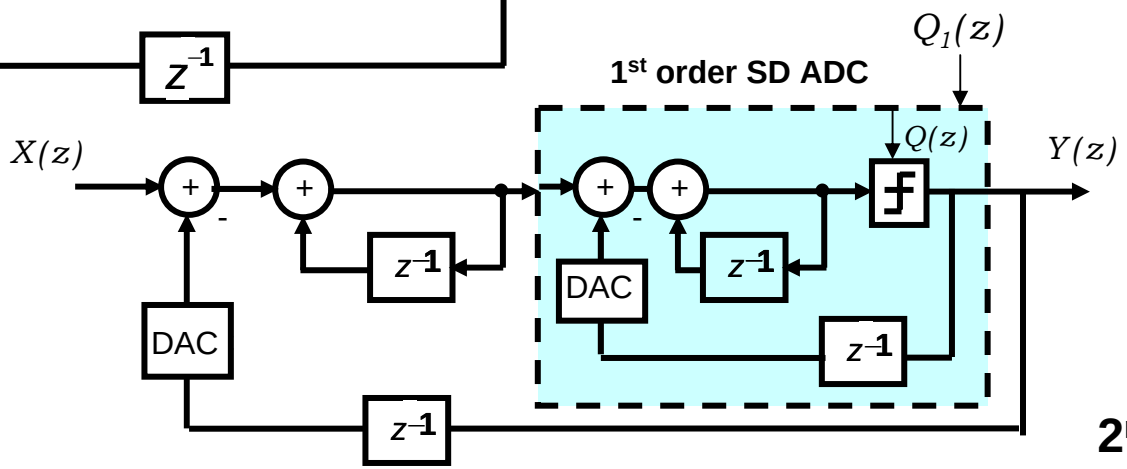
$$\approx \int_{-f_b}^{+f_b} \frac{\Delta^2}{12 f_s} \left|\frac{j2\pi f}{f_s}\right|^{2L} df = \left(\frac{\Delta}{2}\right)^2 \frac{1}{3\pi(2L+1)} \left(\frac{\pi}{OSR}\right)^{2L+1}$$



2nd order sigma-delta ADC



1st order SD ADC



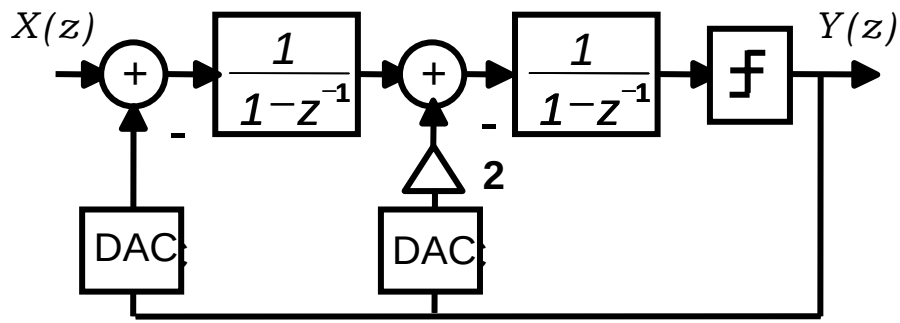
Quantizer is replaced by 1st order SD ADC

2nd order SD ADC

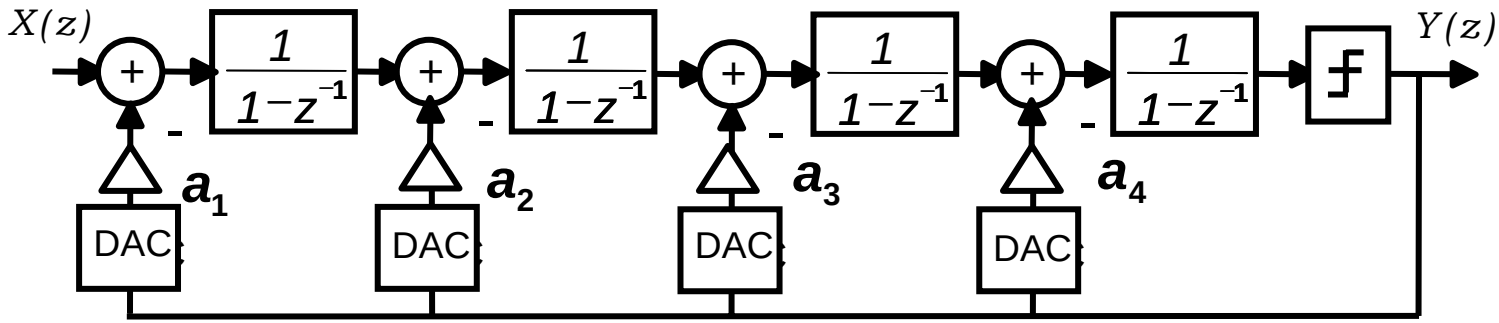
$$Y(z) = X(z) + \left(1 - z^{-1}\right) Q_1(z)$$

$$Q_1(z) = \left(1 - z^{-1}\right) Q(z)$$

$$Y(z) = X(z) + \left(1 - z^{-1}\right)^2 Q(z)$$

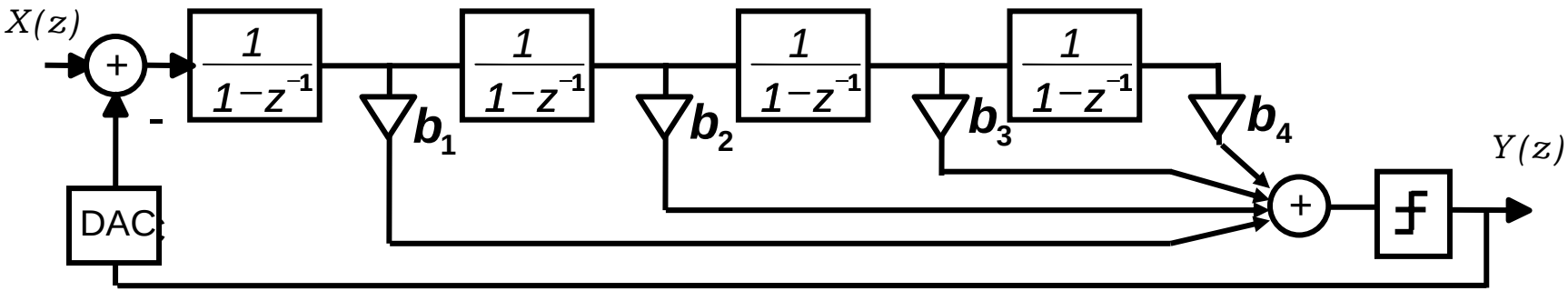


Multi bit sigma-delta ADC



Feedback type

$$NTF(z) = (1 - z^{-1})^4$$

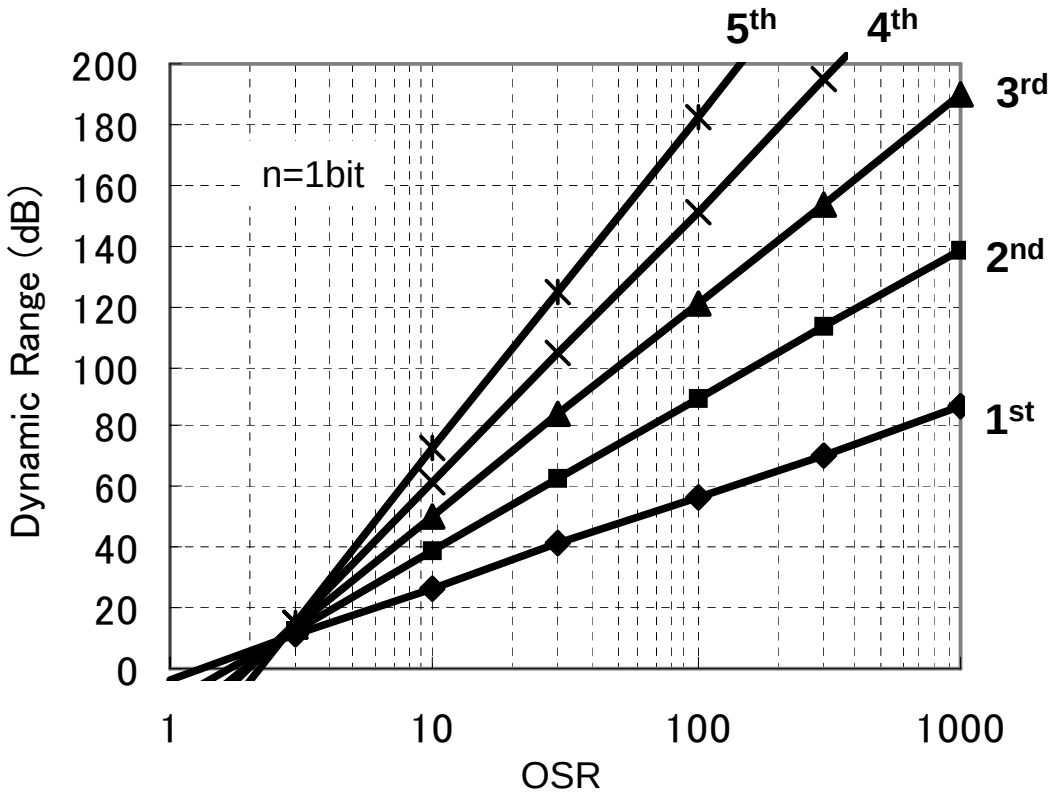


Feedforward type

Dynamic range of sigma-delta ADC

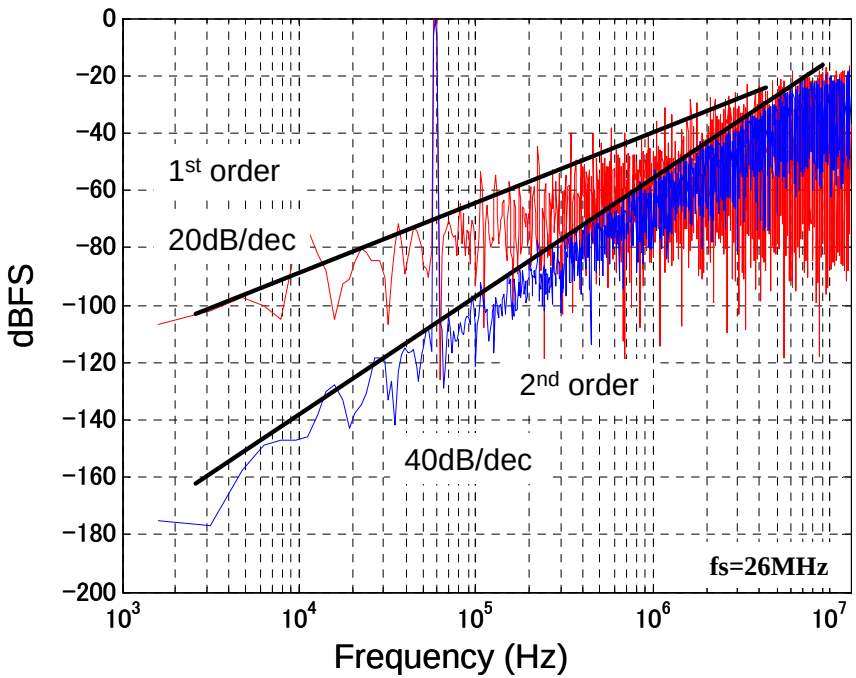
Higher order SD modulator seems effective to increase the dynamic range.
However it is not easy, because of instability, signal saturation, and thermal noise.

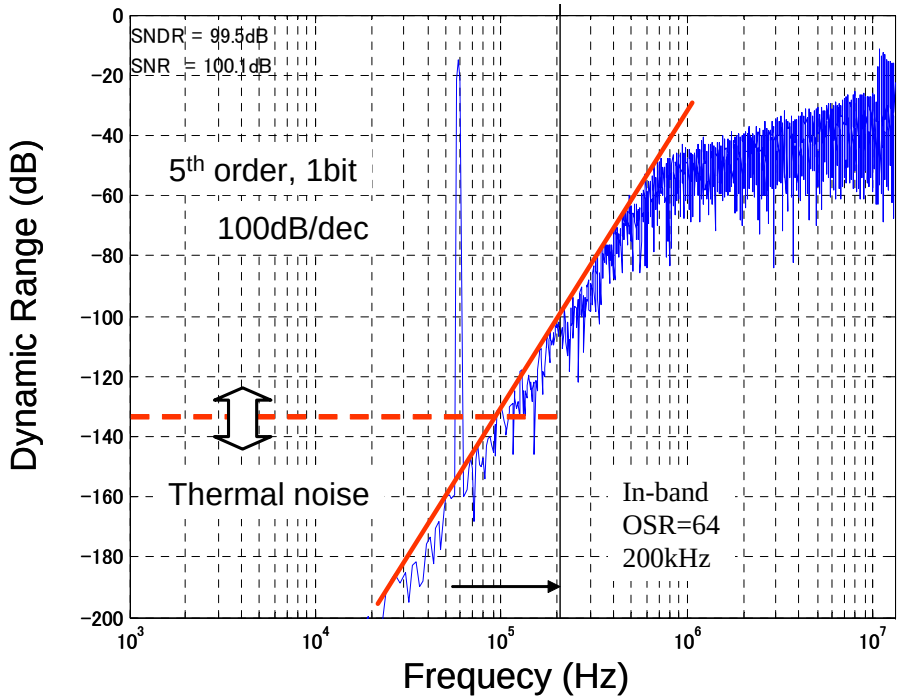
$$DR = \frac{3\pi}{2}\left(2^N - 1\right)^2 (2L+1)\left(\frac{OSR}{\pi}\right)^{2L+1}$$



Noise-shaping characteristics

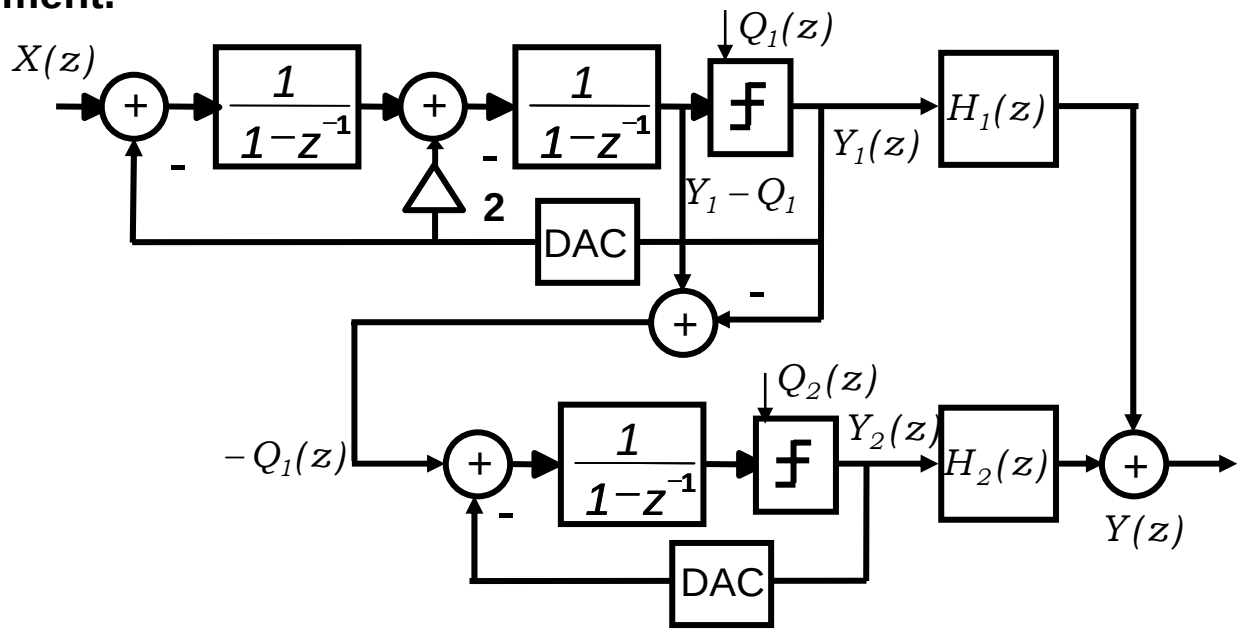
Higher order sigma-delta modulator can realize higher dynamic range, theoretically





Cascade (MASH) sigma-delta modulator

Cascaded SD modulator can realize higher order noise shaping without stability issues. However, high dynamic range is difficult, due to severe mismatch requirement.



$$Y_1(z) = X(z) + \left(1 - z^{-1}\right)^2 Q_1(z) \qquad H_1(z) = 1$$

$$Y_2(z) = -Q_1(z) + \left(1 - z^{-1}\right) Q_2(z) \qquad H_2(z) = \left(1 - z^{-1}\right)^2$$

$$Y(z) = Y_1 H_1 + Y_2 H_2 = X(z) + \left(1 - z^{-1}\right)^2 Q_1(z) - \left(1 - z^{-1}\right)^2 Q_1(z) + \left(1 - z^{-1}\right)^3 Q_2(z)$$

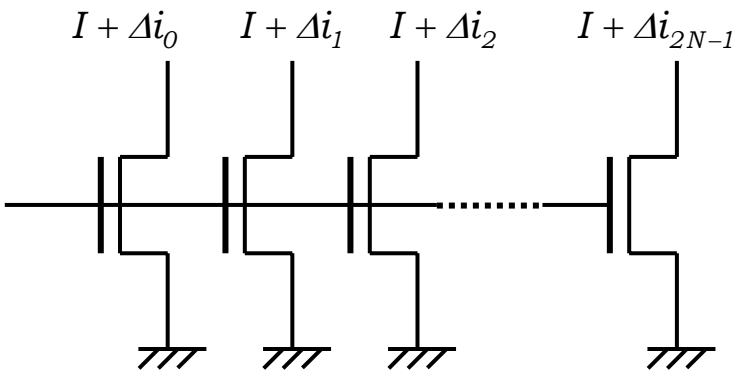
$$Y(z) = X(z) + \left(1 - z^{-1}\right)^3 Q_2(z)$$

6. Basic design considerations

- **Accuracy**
  - **Current mismatch and DAC accuracy**
  - **V_T mismatch**
  - **Capacitor mismatch**
- **Comparator**
  - **Offset compensation**
- **Op-Amp**
  - **Gain and GBW**
  - **kT/C noise**

Current mismatch and DAC accuracy

Larger resolution requires smaller mismatch.



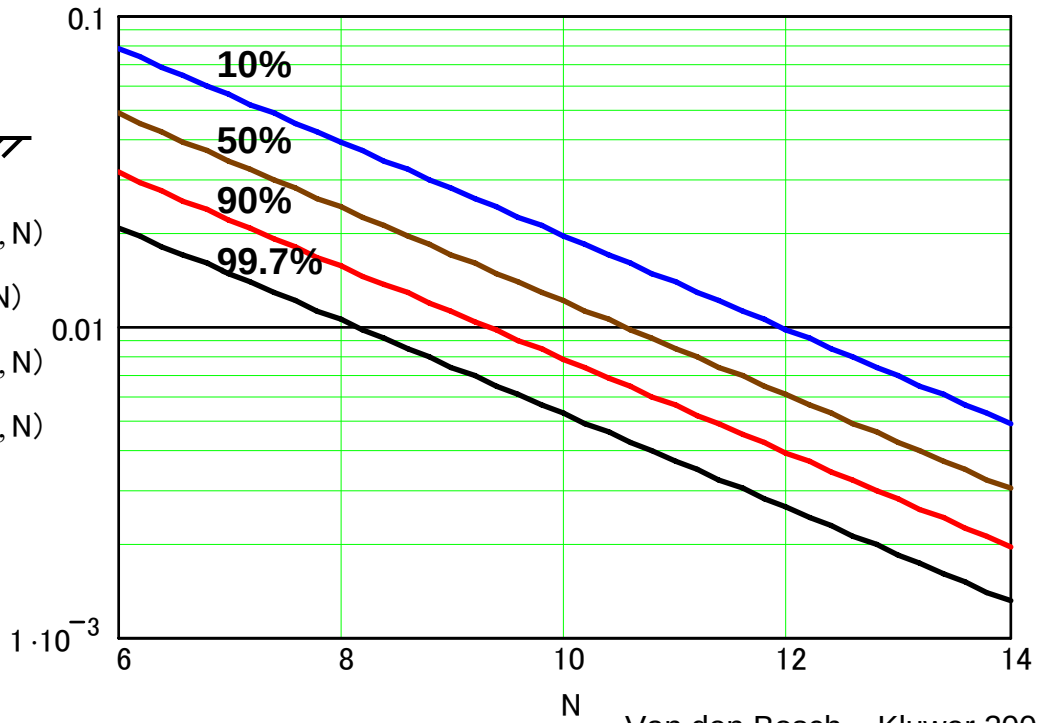
$$\frac{\sigma(I)}{I} \approx \frac{1}{2C\sqrt{2^N}}$$

sigma(3.0, N)
sigma(2, N)
sigma(1.3, N)
sigma(0.8, N)

N: resolution

C: constant determined by INL yield

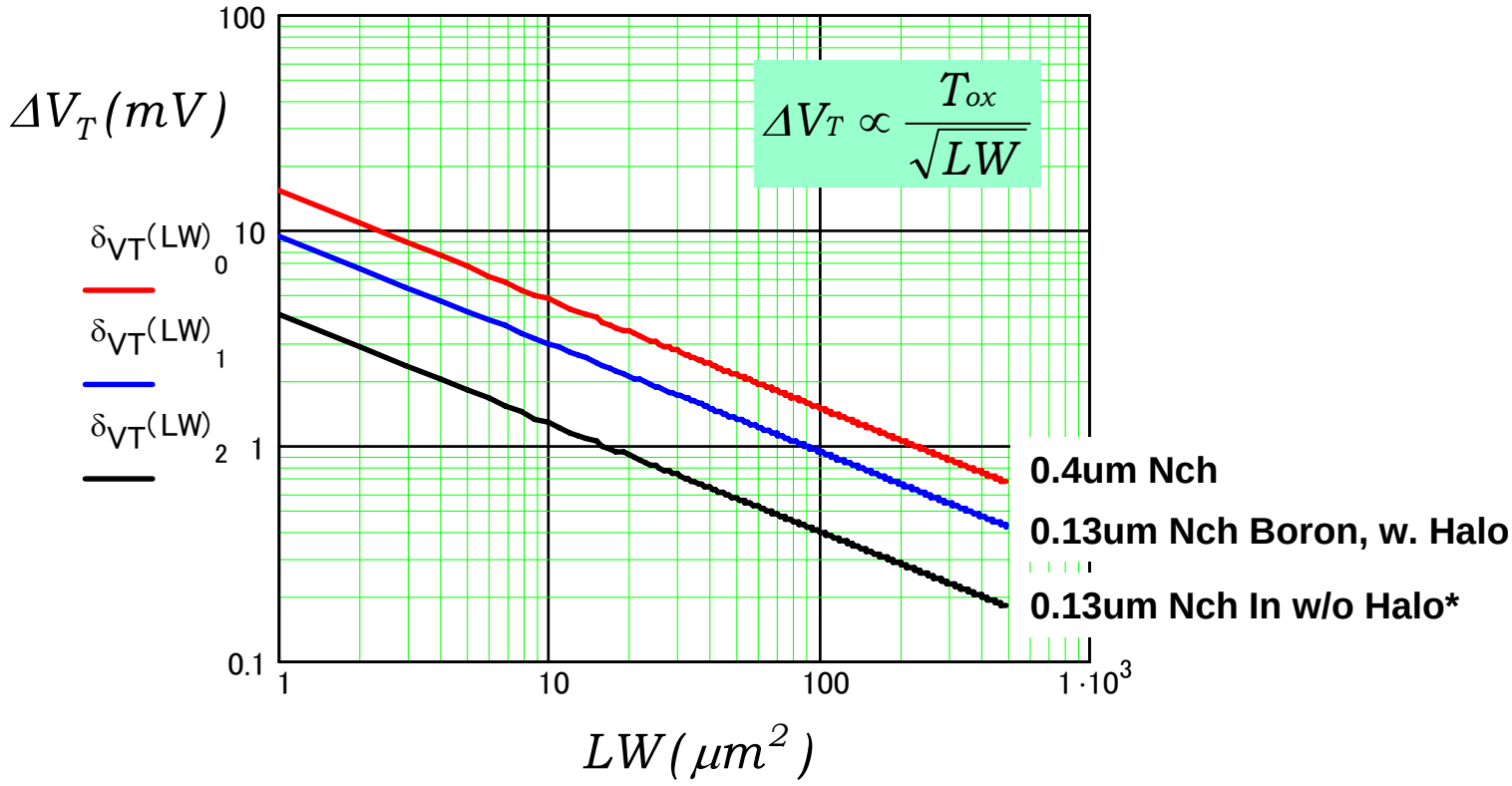
INL yield



Van den Bosch,.. Kluwer 2004

V_T mismatch

Larger gate area is needed for smaller V_T mismatch.
Technology scaling reduces V_T mismatch if the gate area is equal.



Mismatch current and transistor size

Smaller mismatch requires larger L and W.

$$I_{ds} = K' \frac{W}{L}\left(V_{gs} - V_T\right)^2$$

$$\Delta I_{ds} = \frac{\partial I_{ds}}{\partial V_T}\Delta V_T + \frac{\partial I_{ds}}{\partial K'}\Delta K' + \frac{\partial I_{ds}}{\partial\left(\frac{W}{L}\right)}\Delta\left(\frac{W}{L}\right)$$

$$\frac{\Delta I_{ds}}{I_{ds}} = \frac{-2\Delta V_T}{V_{gs} - V_T} + \frac{\Delta K'}{K'} + \frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)}$$

$$\left(\frac{\Delta I_{ds}}{I_{ds}}\right)^2 = \frac{4K' A_{VT}^2}{L^2 I_{ds}} + \frac{A_K^2}{WL} + A_{WL}^2\left(\frac{1}{W^2} + \frac{1}{L^2}\right)^2$$

Mismatch

$$\Delta V_T \approx \frac{A_{VT}}{\sqrt{LW}}$$

$$\frac{\Delta K'}{K'} \approx \frac{A_{K'}}{\sqrt{LW}}$$

$$\frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)} = A_{WL}\sqrt{\frac{1}{W^2} + \frac{1}{L^2}}$$

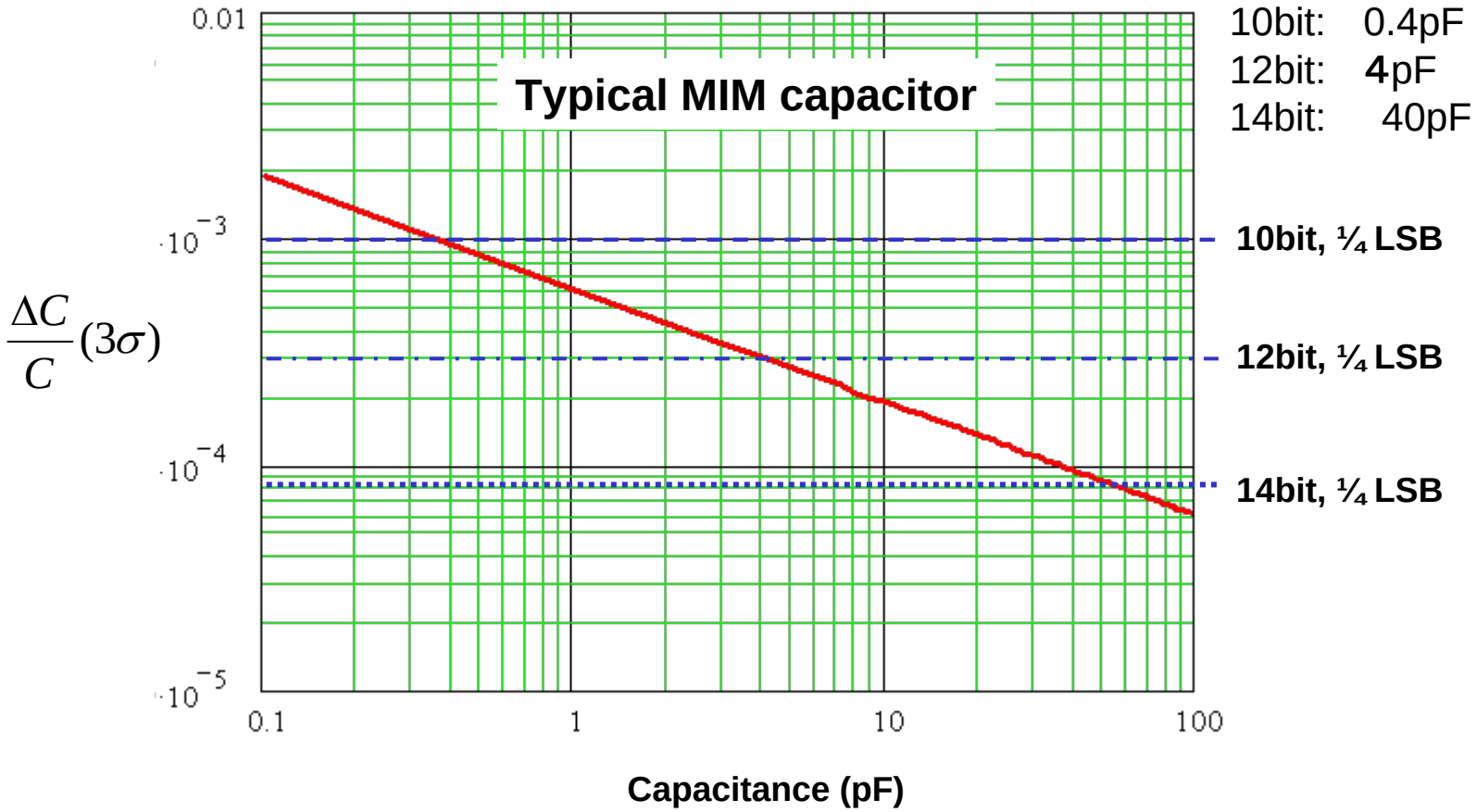
$$V_{gs} - V_T = \sqrt{\frac{I_{ds}}{K'\left(\frac{W}{L}\right)}}$$

Capacitor mismatch

Smaller capacitor mismatch requires larger capacitance

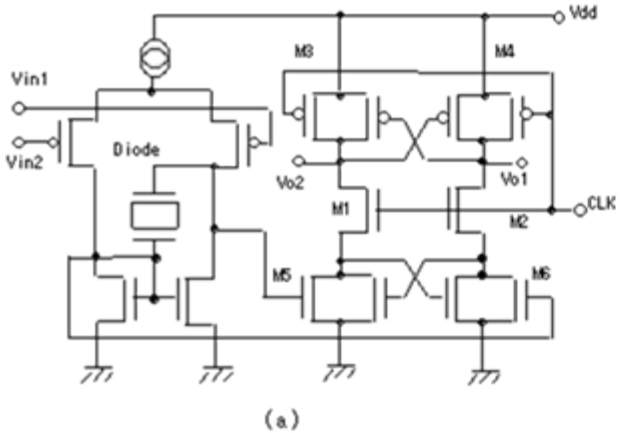
$$\frac{\Delta C}{C}(3\sigma) = \frac{6\times10^{-4}}{\sqrt{C_{(pF)}}}$$

Coefficient depends Fab.

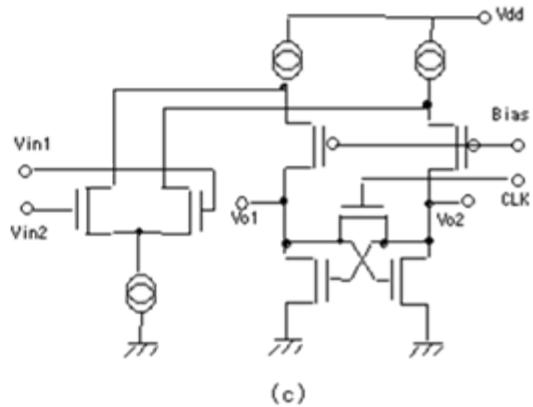


CMOS comparators

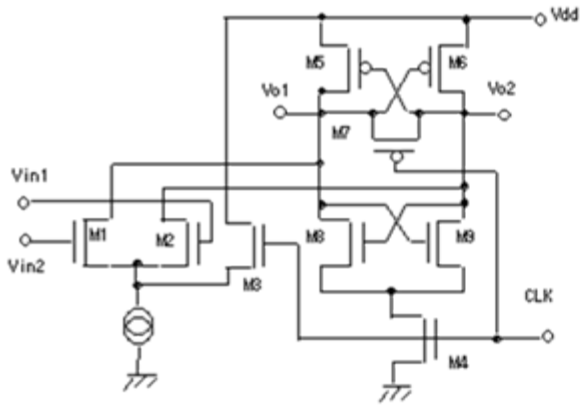
There are many types of comparator circuits



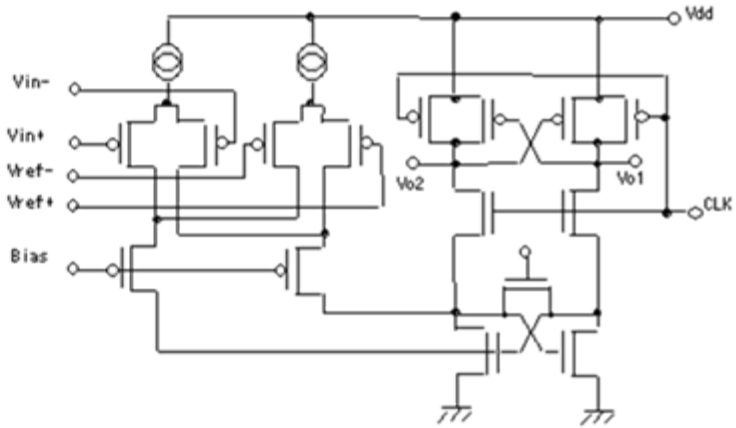
(a)



(c)



(b)



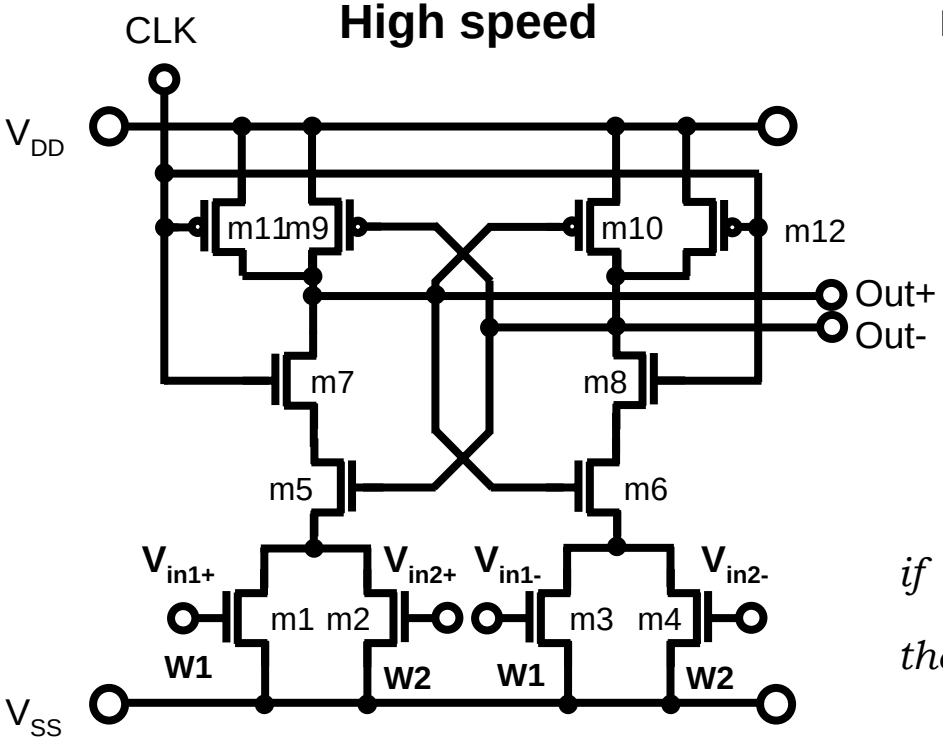
(d)

Low power CMOS comparators

CMOS comparator are low power because of the lack of static current.

No static current
Differential comparison
Interpolation action
High speed

T.B.Cho., et al., J.S.C., Vol.30, No.30, pp.166-172, Mar. 1995.



Interpolation action

$$G_1 = K_p\left[\frac{W_1}{L}\left(V_{in1+} - V_{th}\right) + \frac{W_2}{L}\left(V_{in2+} + -V_{th}\right)\right]$$

$$G_2 = K_p\left[\frac{W_1}{L}\left(V_{in1-} - V_{th}\right) + \frac{W_2}{L}\left(V_{in2-} + -V_{th}\right)\right]$$

$$if\ W_1 : W_2 = \frac{m-n}{m} : \frac{n}{m}$$

$$then,\ (m-n)V_{in1+} + nV_{in2+} = (m-n)V_{in1-} + nV_{in2-}$$

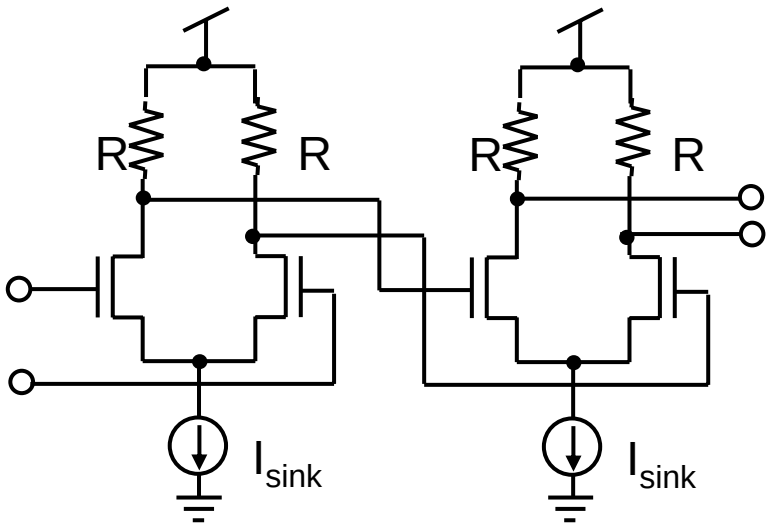
Design rule and Speed in Comparator

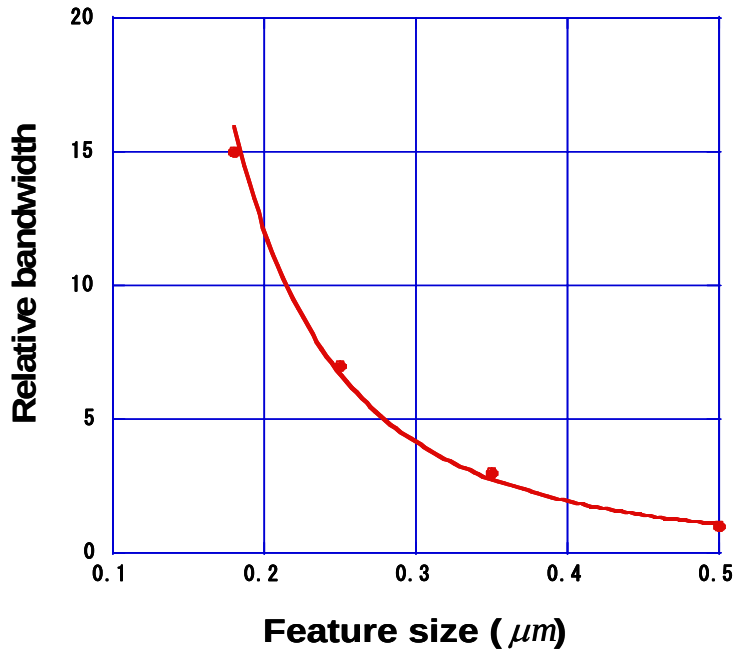
Gain bandwidth (=Speed) is inversely proportional to the L^2 (channel length).
Technology scaling is still effective in increasing the comparator speed,
if we are not concerned with the signal's dynamic range.

$$GBW = \frac{g_m}{2\pi\left(WC_j + \frac{2}{3}C_{ox}LW\right)} = \frac{I_{sink}}{2\pi\left(WC_j + \frac{2}{3}C_{ox}LW\right)V_{eff}}$$

$$GBW = \frac{\mu V_{eff}}{2\pi L^2\left(\frac{2}{3} + \frac{C_j}{k}\right)}$$

$$I_{sink} = \frac{\mu C_{ox}}{2}\frac{W}{L}V_{eff}^2 \qquad C_{ox} = \frac{\kappa}{L}$$

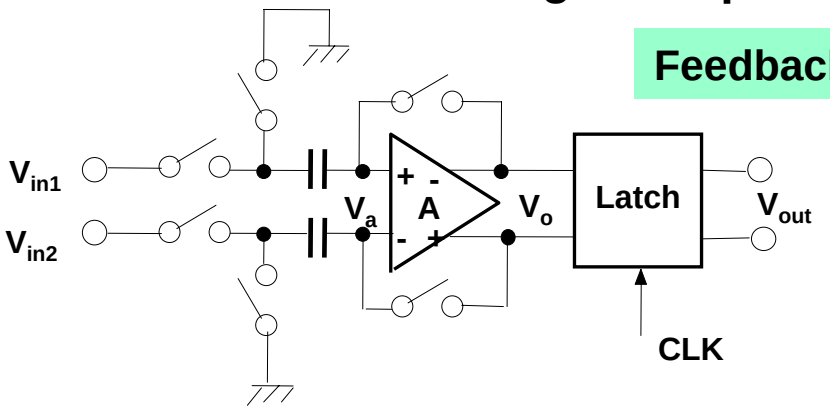




Offset compensation

Two ways for suppressing offset voltage.

Store the offset voltage in capacitors and subtract it from the signal.



a) Offset cancel at input nodes

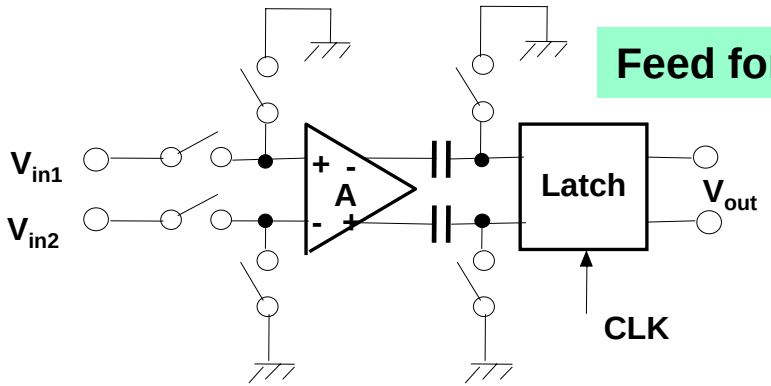
Feedback= High gain type

$$(V_a - V_{osA})(-A) = V_o = V_a$$

$$\therefore V_o = V_a = \frac{A}{1+A} V_{osA}$$

V_{osA}: Offset of the amplifier

V_{osL}: Offset of the latch



b) Offset cancel at output nodes

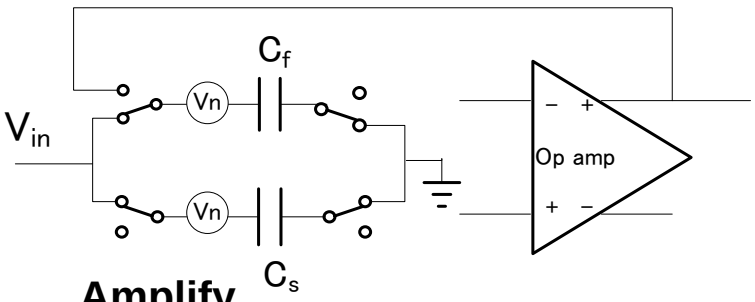
Feed forward =Low gain type

$$V_{os\_in} = \frac{V_{osl}}{A}$$

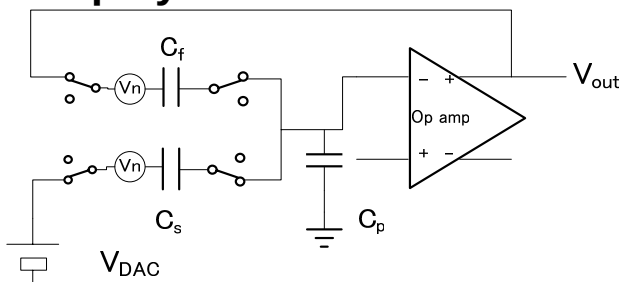
Operational amplifier

Higher resolution requires higher open loop gain.
Higher conversion frequency requires higher closed loop GBW.

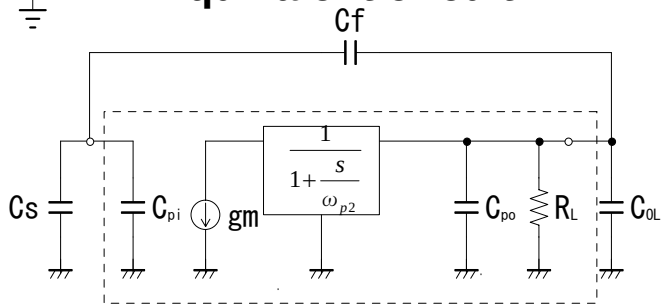
Sampling



Amplify



Equivalent circuit



DC gain

$$G_{error} \approx -\frac{1}{G}\left(2+\frac{C_p}{C_f}\right) \approx -\frac{1}{G\beta} \qquad \beta \equiv \frac{1}{\left(2+\frac{C_p}{C_f}\right)}$$

$$\frac{1}{G} \le \frac{\beta}{2^{N-M+1}}$$

N:ADC resolution
M:Stage resolution

$$G(dB) > 6N + 10$$

for 1.5b pipeline ADC

Closed loop gain-bandwidth

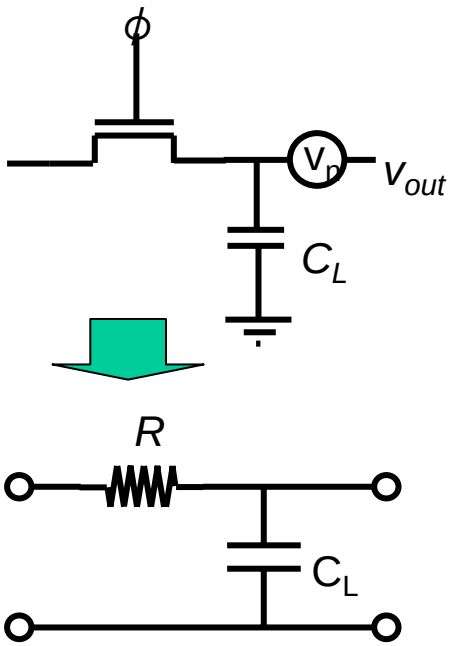
$$GBW_{\_close} = \frac{g_m \beta}{2\pi C_L} > \frac{N \cdot fc}{3}$$

$$\beta = \frac{C_f}{C_f + C_s + C_{pi}}$$

$$C_L = C_{po} + C_{oL} + \frac{C_f\left(C_s + C_{pi}\right)}{C_f + C_s + C_{pi}}$$

kT/C noise

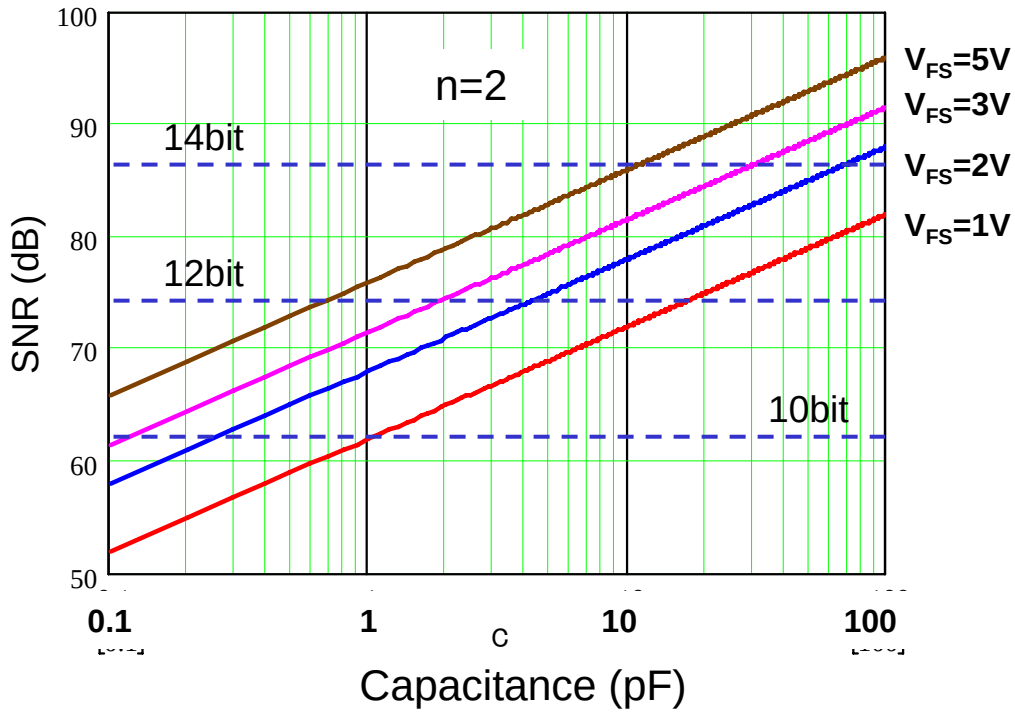
Larger SNR requires larger capacitance and larger signal swing.
Low signal swing increases required capacitance.



$$\overline{v_n^2} = \frac{nkT}{C}$$ n: configuration coefficient

$$SNR(dB) = 10\log\left(\frac{CV_{FS}^2}{8nkT}\right)$$

$$\left\langle v_n^2 \right\rangle = 4kTR\int \frac{1}{1+(\omega CR)^2}\frac{d\omega}{2\pi} = \frac{kT}{C}$$



Basic design consideration

Very tough tradeoffs, so let's keep up the design effort.

Small mismatch

$$\frac{\Delta C}{C} \text{ or } \frac{\Delta V_{off}}{V_{FS}} \propto \frac{1}{2^N}$$

Increase Capacitance

$$\frac{\Delta C}{C} \propto \frac{1}{\sqrt{C}} \text{ or } \Delta V_{off} \propto \frac{1}{\sqrt{LW}} \propto \frac{1}{\sqrt{C_g}}$$

$$C \propto 2^{2N}$$ *Results in*

Decrease speed and Increase Power

$$f_s \propto GBW \propto \frac{g_m}{C} \propto \frac{g_m}{2^{2N}} \quad GBW \propto \frac{I_d}{C} \propto \frac{I_d}{2^{2N}}$$

$$P_d \propto V_d I_d \propto f_s \cdot C \propto f_s \cdot 2^{2N}$$

$$f_s \propto \frac{I_d}{2^{2N}} \qquad P_d \propto f_s \cdot 2^{2N}$$

Solutions

1) Architecture
Pipeline, Parallel
2) Redundancy
3) Error compensation
4) Circuit design

However, kT/C issue remains

$$SNR \propto CV_{sig}^2 \propto 2^{2N}$$

$$C \propto \left(\frac{2^N}{V_{sig}}\right)^2$$

Solutions

1) Increase signal swing
2) Increase OSR

$$SNR \propto OSR$$

Acknowledgement

- **The author thanks Mr. T. Matsuura from Renesus for some slides provision.**

Study-aid books

- **B. Razavi, “Data conversion system design,” IEEE press.**
- **P. E. Allen and D. R. Holberg, “ CMOS Analog Circuit Design,” 2nd Edition, OXFORD University Press.**
- **D. A. Johns and K. Martin, “Analog integrated circuit design,” John Wiley & Sons.**
- **R. J. Baker, “ CMOS mixed-signal circuit design,” IEEE Press.**
- **R.van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters,” 2nd Edition, Kluwer Academic Publishers.**
- **M. Gustavsson, J. J. Wikner and N. N. Tan, “CMOS data converters for communications,” Kluwer Academic Publishers.**
- **C. Shi and M. Ismail, ”Data converters for wireless standards,” Kluwer Academic Publishers.**
- **A. Rodriguez-Vazquez, F. Mederio, and E. Janssens, “CMOS Telecom Data Converters,” Kluwer Academic Publishers.**