A Study on Full Digital Clock Data Recovery (CDR)

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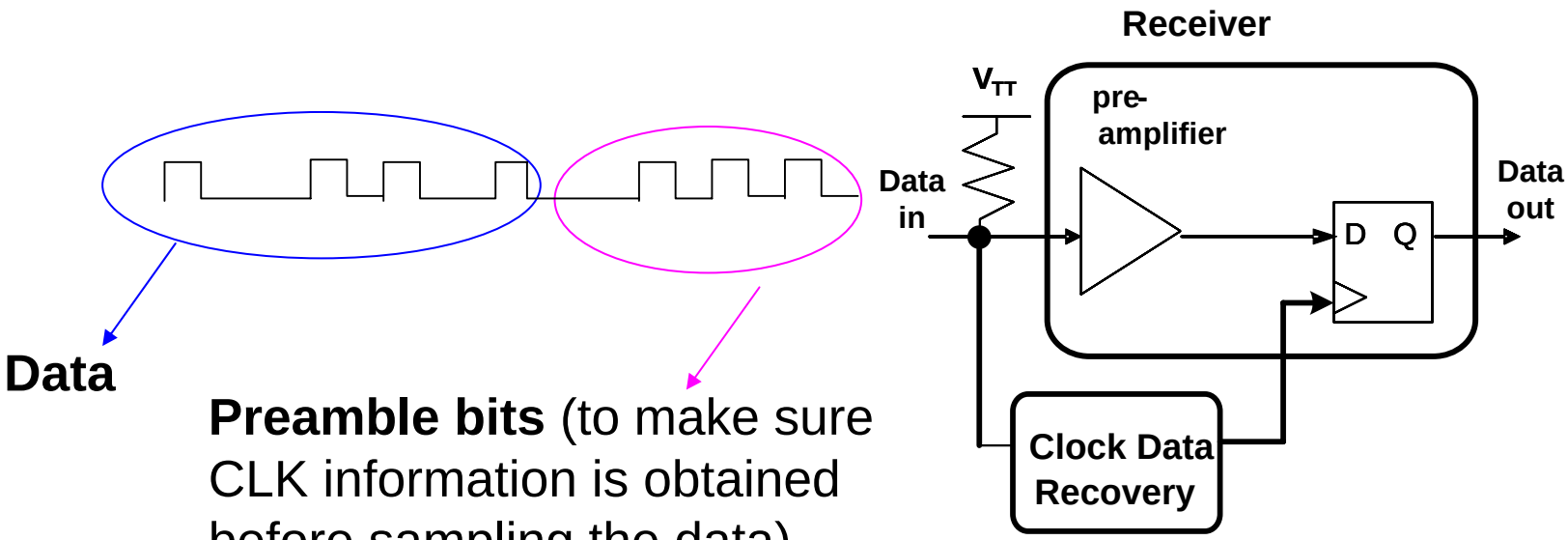
- CDR fundamentals
- PLL based CDR and Oversampling CDR
- Proposed CDR concept
- Concept verification by system level simulation
- Merit & Demerit
- Summary and Future work

CDR Fundamentals

A part of receiver that:

Preamble bits —**get**→ Timing —**sample**→ Incoming Data



Preamble bits (to make sure CLK information is obtained before sampling the data)

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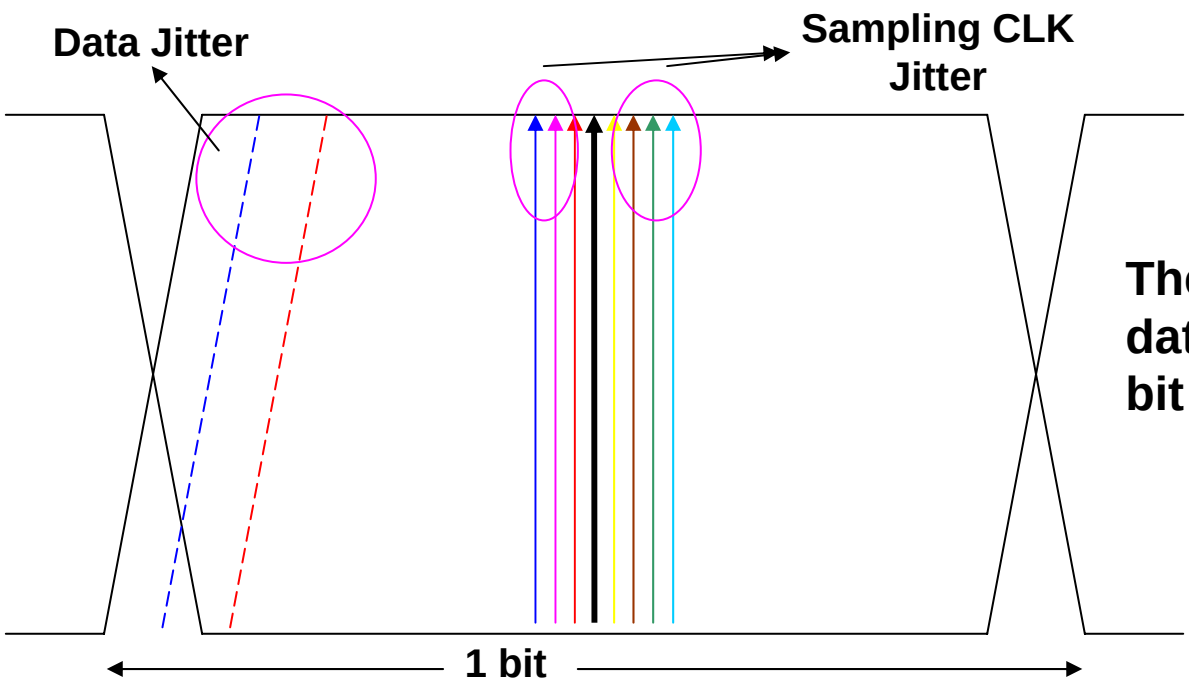
Applications

Any digital communication systems/network that use serial link:

- **Optical Receivers (SONET)**
- **Chip to chip**
- **Peripheral I/O**
- **Crossbar switches for Asynchronous Transfer Mode**

CDR Fundamentals



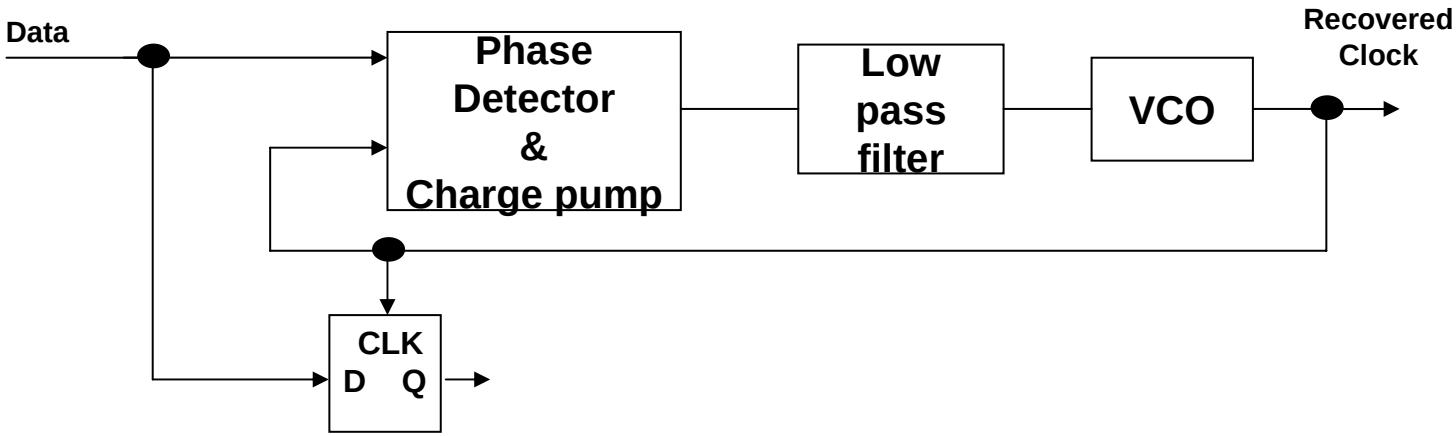
The optimum point to sample data is at the middle of the bit window (black arrow)

Bit error only occurs when the CLK jitter is greater than 0.5bit period

CDR classification

- **Phase Locked Loop**
- **Oversampling Clock Recovery**

Phase Locked Loop:



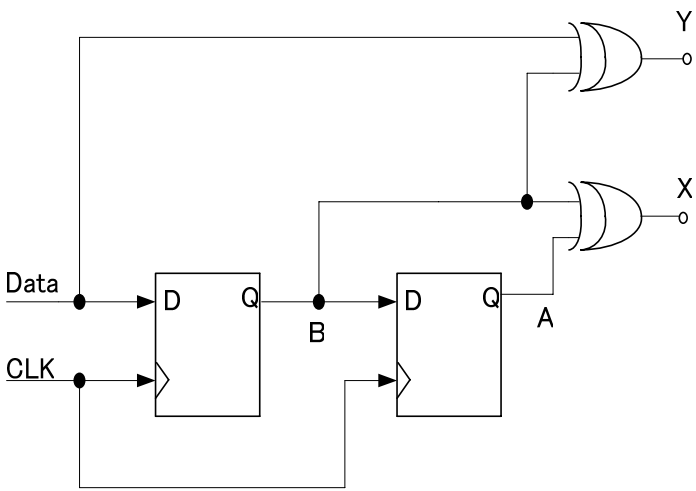
PLL based CDR

Phase detector in PLL for CDR must be able to detect edges and phase difference in random data.

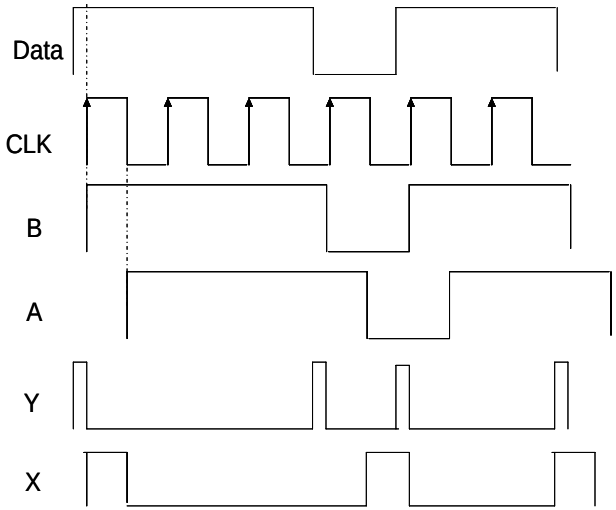
Classified into:

- **Hogge's Analog Phase Detector**
- **Alexander Binary Phase Detector**

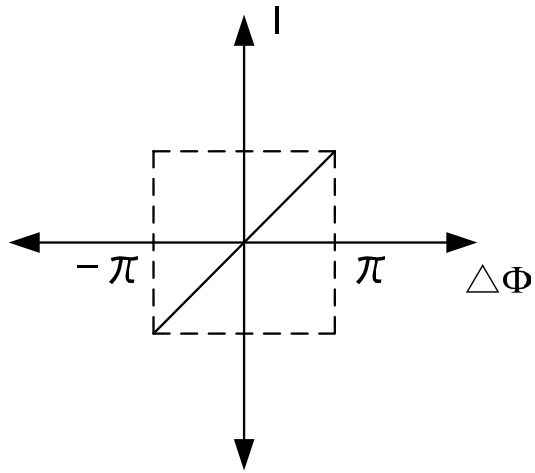
Hogge's Phase detector



Timing Waveform



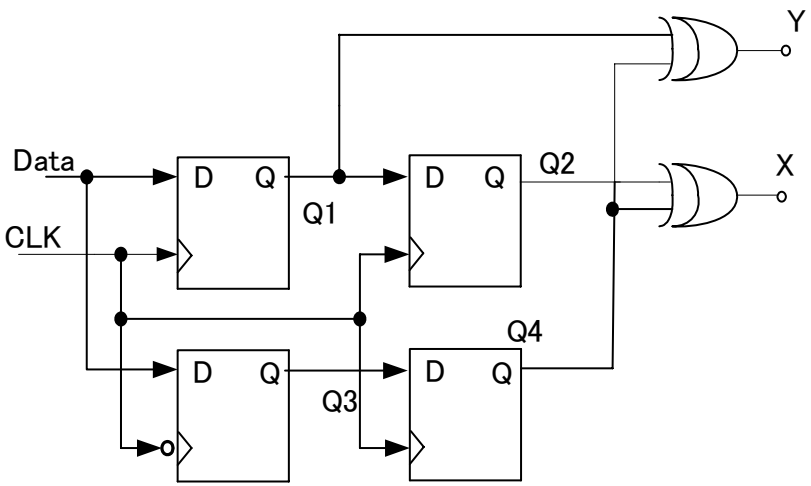
Transfer Function



The difference between X & Y will show the phase difference amount and polarity

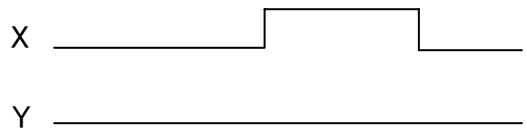
PLL based CDR

Alexander Binary PD

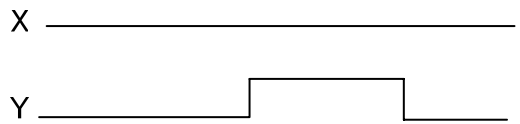


Timing Waveform

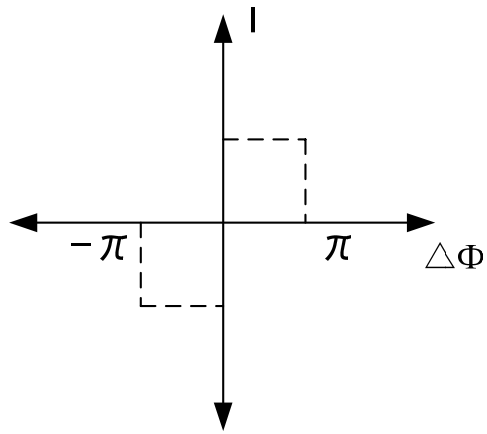
When data edge leads



When CLK edge leads



Transfer Function



The result of phase detection only tells the polarity, whether leading or lagging.

The amount of phase difference is not detected

Thus, jitter is constantly produced at every phase detection

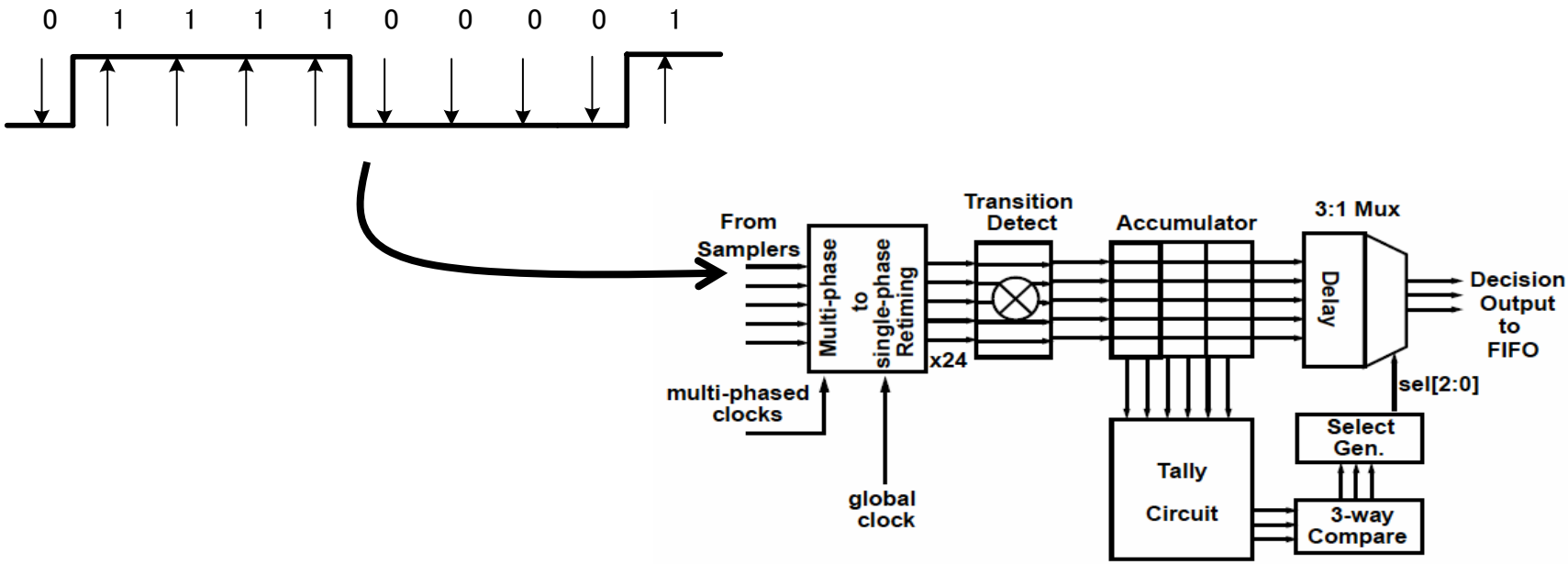
PLL Issue

- **Low frequency acquisition, within 25% of VCO center frequency**
- **Long lock time, about 100 preamble data** (depends on bandwidth, which also affect jitter performance, there's a trade off)
- **Possibility of harmonic lock**

Oversampling CDR

Data is obtained by sampling data by multiphase clock:

Data is processed to choose which values represent the data bit:



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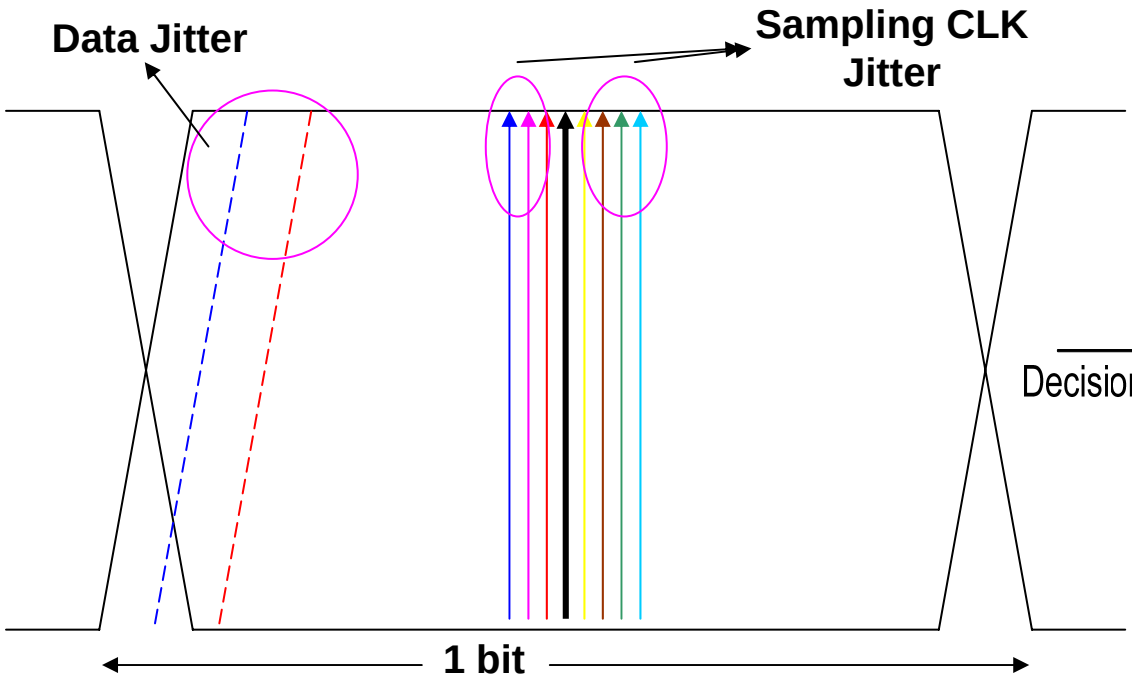
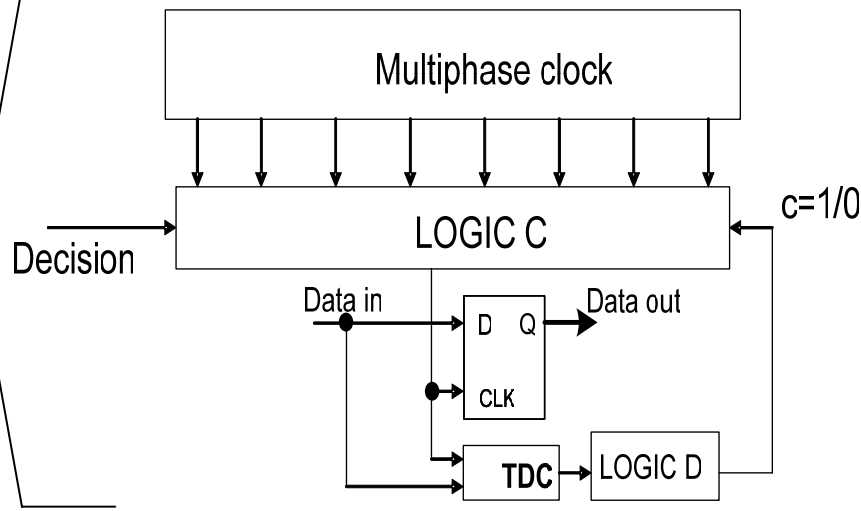
Oversampling CDR Issue

- **At least 3 sample is needed for each data bit and special clock is needed for sampling.**
  (When input frequency change,
  sampling clock must also be changed.)
- **Jitter due to phase quantization**

Proposed CDR Intro

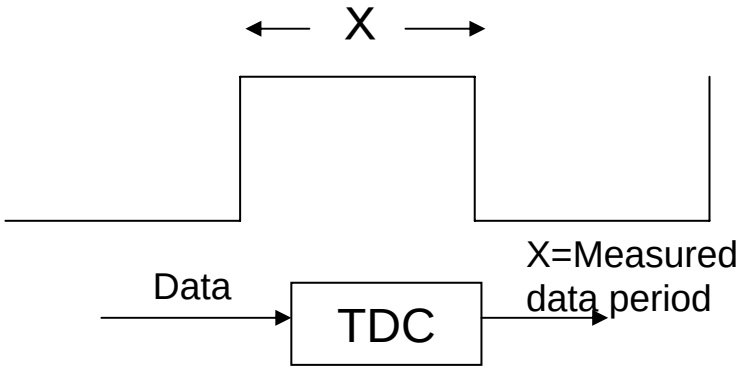




The proposed CDR is maintained to sample around the middle of the bit window (colourful arrows)

But NEVER at the middle of bit window!!

Proposed CDR

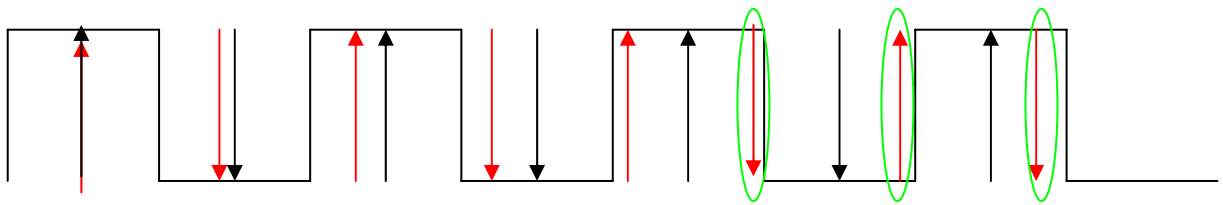


Example: TDC resolution ＝10 ps

Data period ＝1001.3 ps

⇨ X=1000 ps or 1010 ps

Due to the fact that $\Delta\Phi=\Delta\omega.T$, if we use X directly, large BER will occur:



= sampling using X as sampling period

=sampling using ideal data period

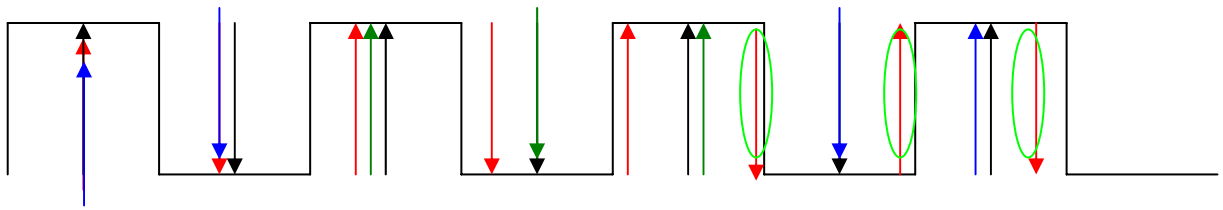
=sampling error

Alternate Sampling

Data period = 1001.3 ps
TDC resolution = 10 ps

Data period lies within 1000 ps and 1010 ps
(TDC step interval)

If we use this sampling period alternately :



= 1010 ps (Upper boundary)

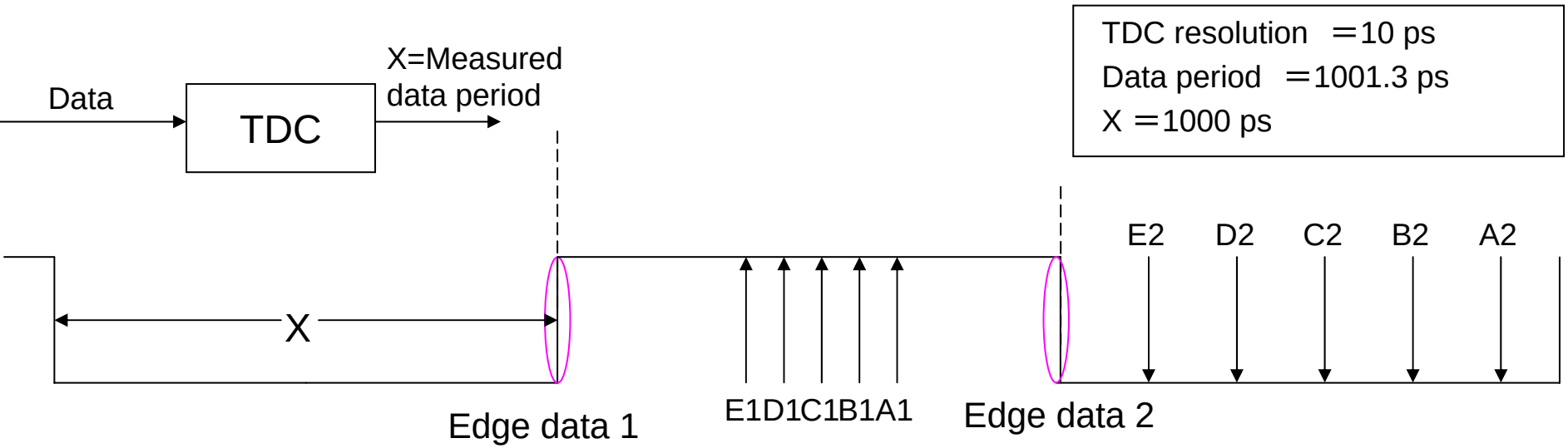
= 1000 ps (Lower boundary)

= ideal sampling point

= sampling point using result from TDC directly

Error will not occur !

Obtaining Upper and Lower boundary



A ＝ X + 2*TDC resolution= 1020 ps

B ＝ X + TDC resolution= 1010 ps

C ＝ X = 1000 ps

D ＝ X - TDC resolution= 990 ps

E ＝ X - 2*TDC resolution= 980 ps

Compare

A2>A1

B2>B1

C2<C1

D2<D1

E2<E1

Lower Boundary ＝1000 ps

Upper Boundary ＝1010 ps

Theoretically, only 3 preamble data is needed!!

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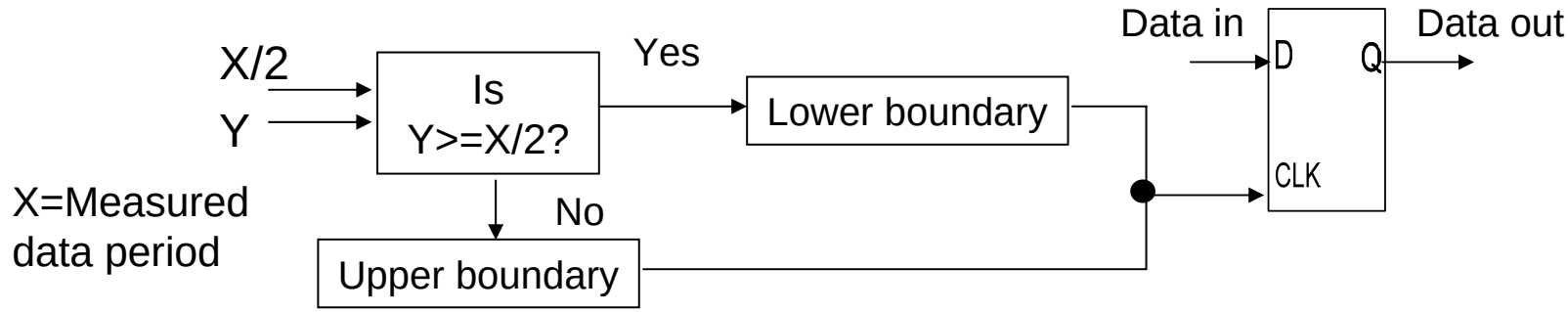
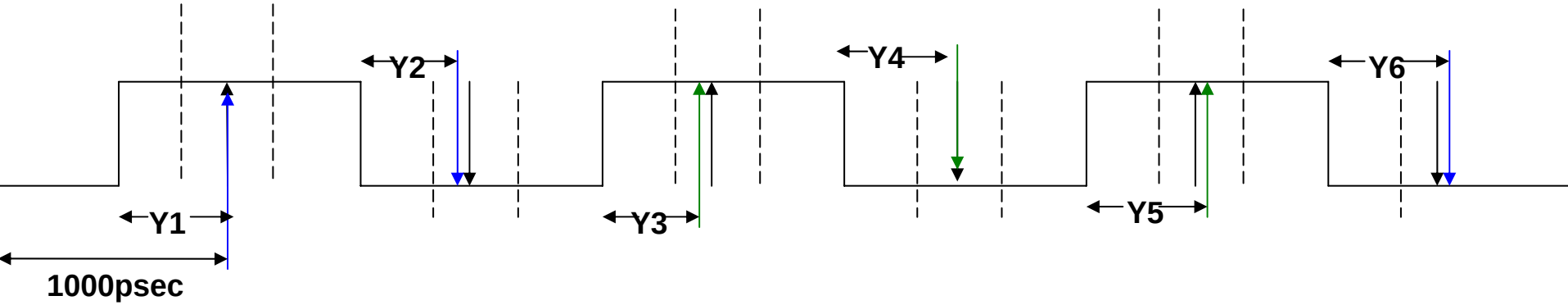
Sampling Based on Feedback system

Compare distance between data edge and sampling edge (Y's) with X/2





= 1010 ps (Upper boundary)

= 1000 ps (Lower boundary)

= ideal sampling point

Comparison is executed at every data edge

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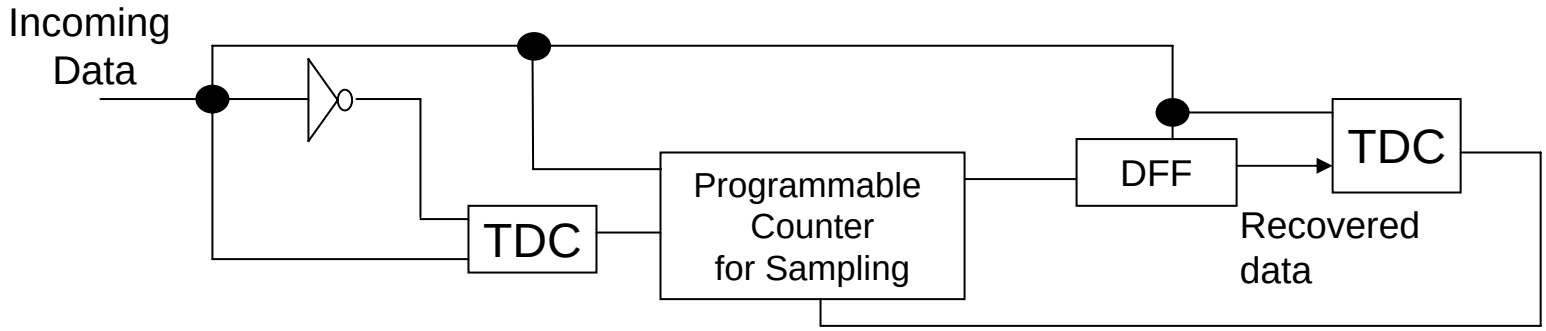
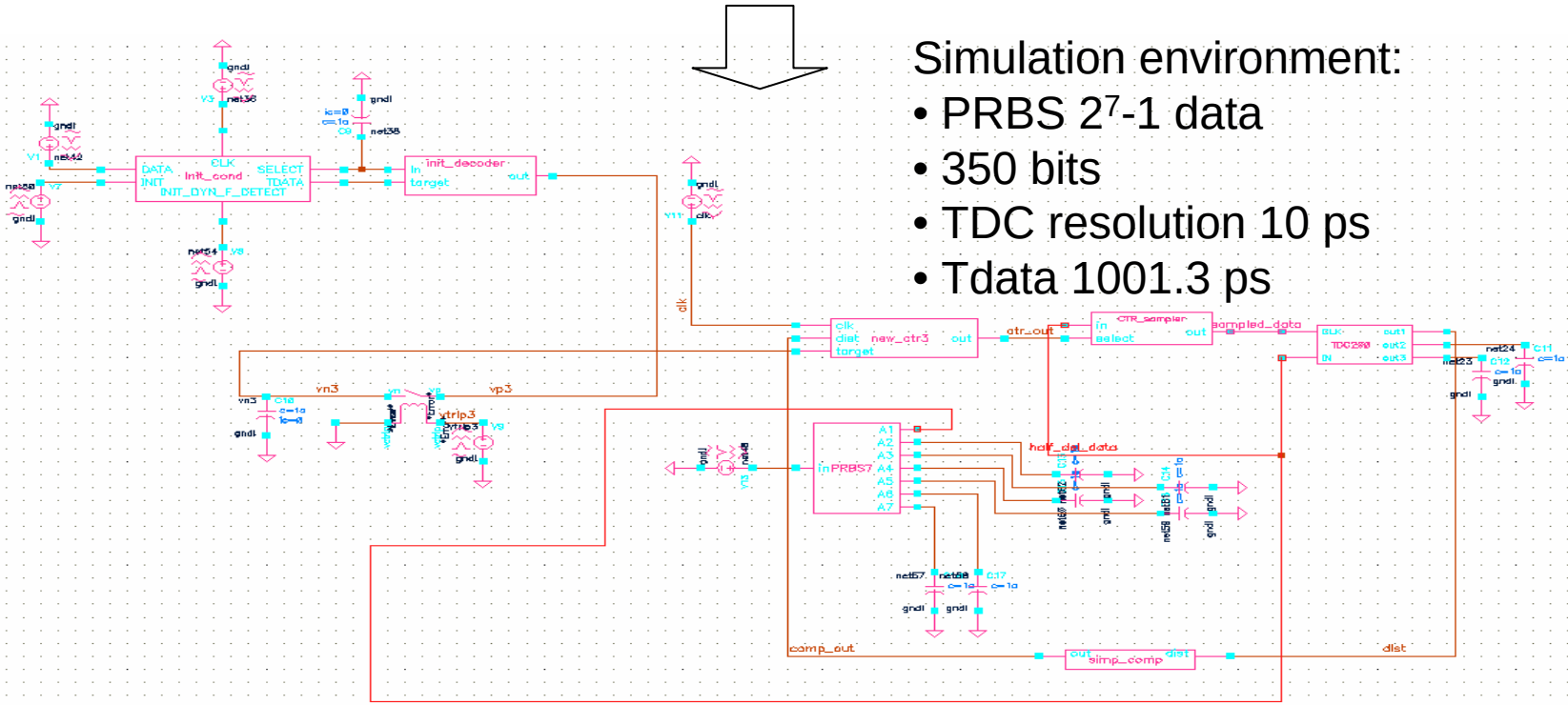
Simulation Result in Verilog-A

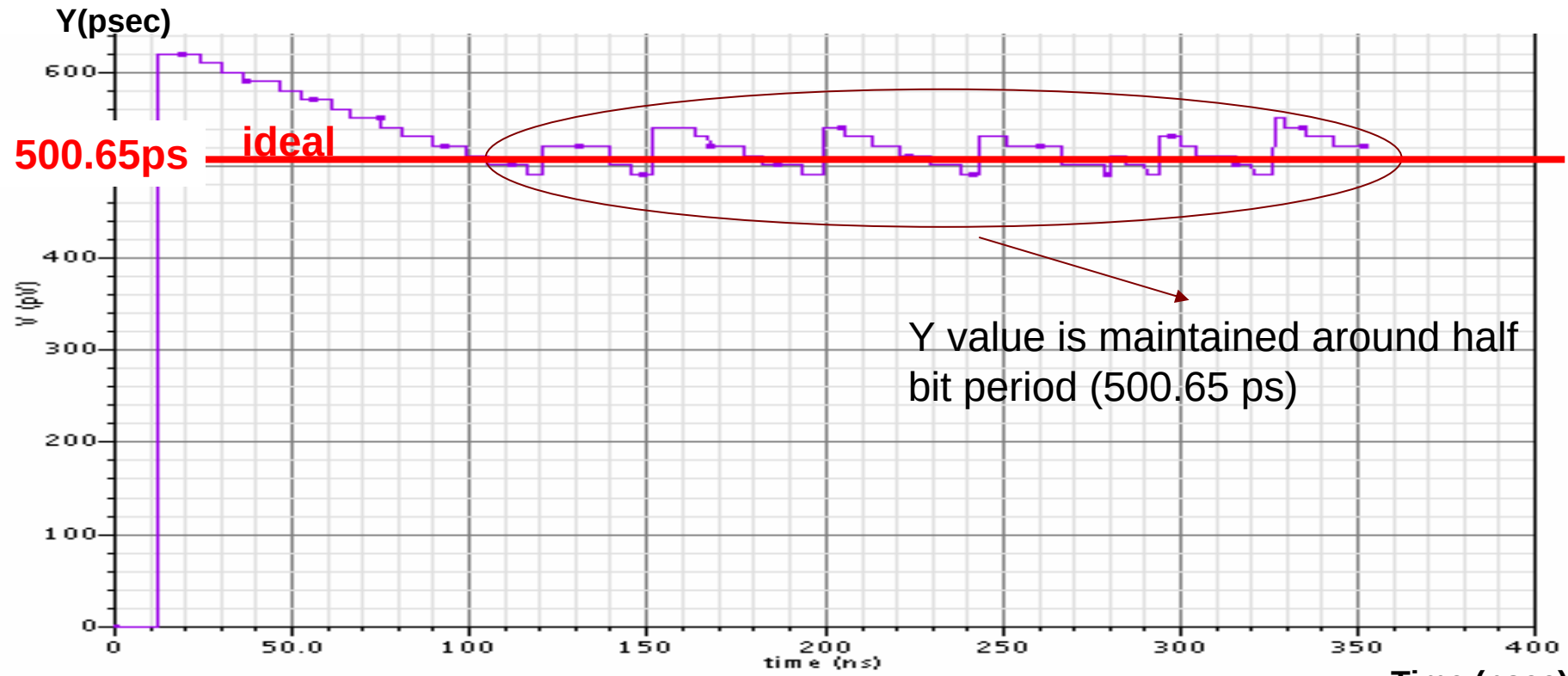


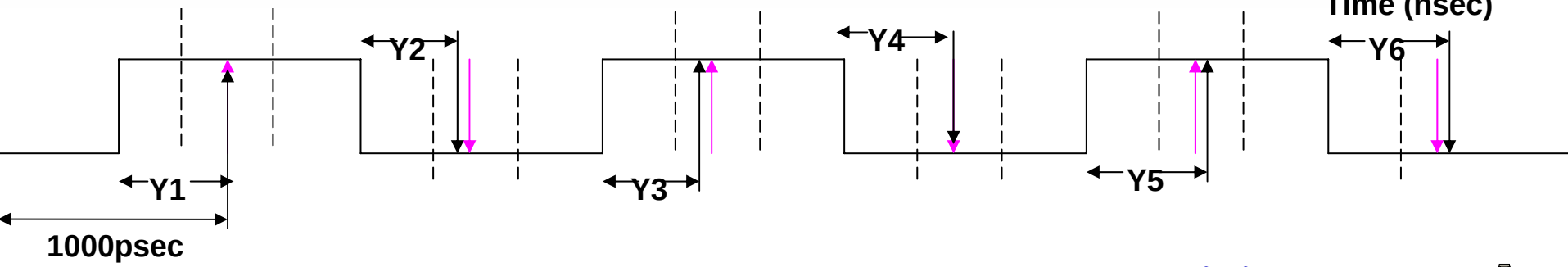


Simulation environment:

- PRBS 2^7-1 data
- 350 bits
- TDC resolution 10 ps
- Tdata 1001.3 ps

Simulation Result in Verilog-A



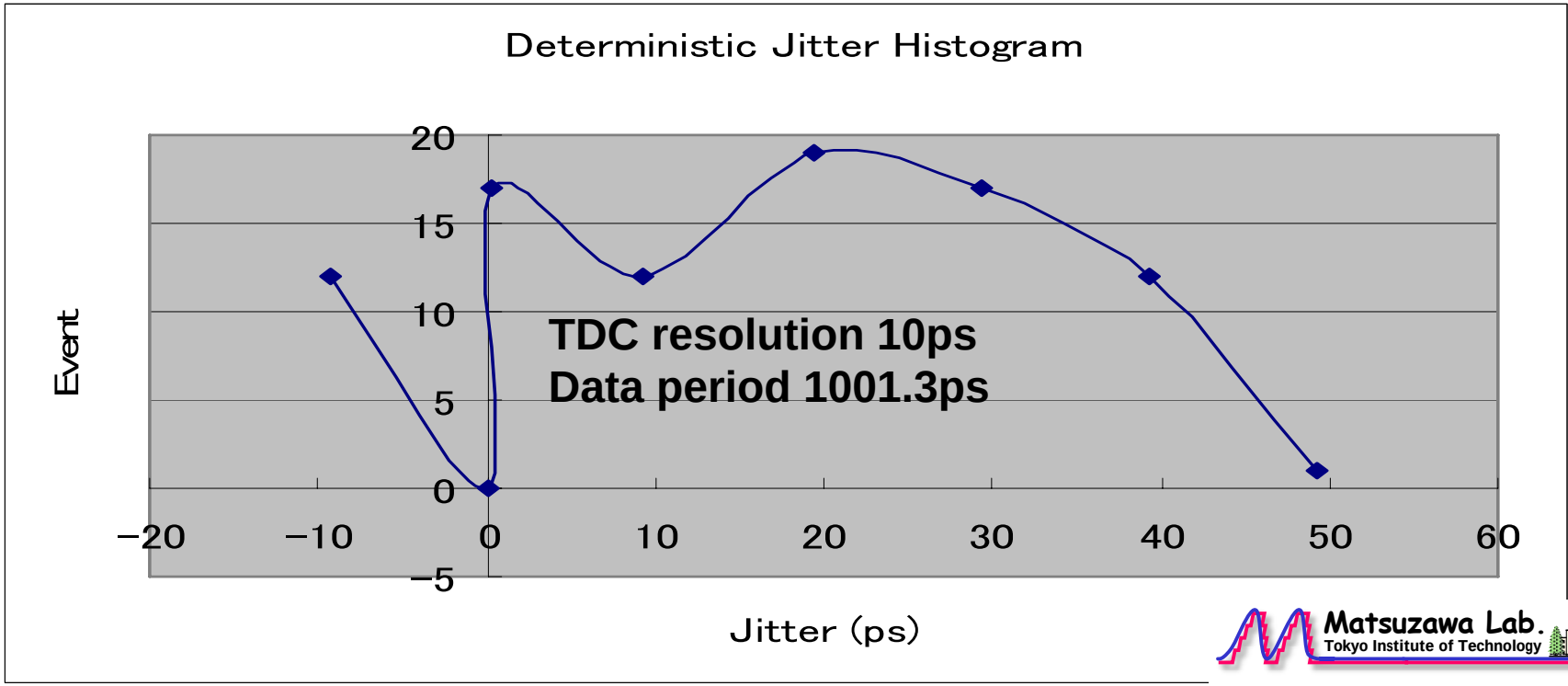


Deterministic Jitter estimation

The peak to peak jitter is dependent upon TDC resolution and data type:

2^N-1 ⟶ N*TDC resolution

The RMS jitter is dependent upon the time distance between data period and lower/upper boundary

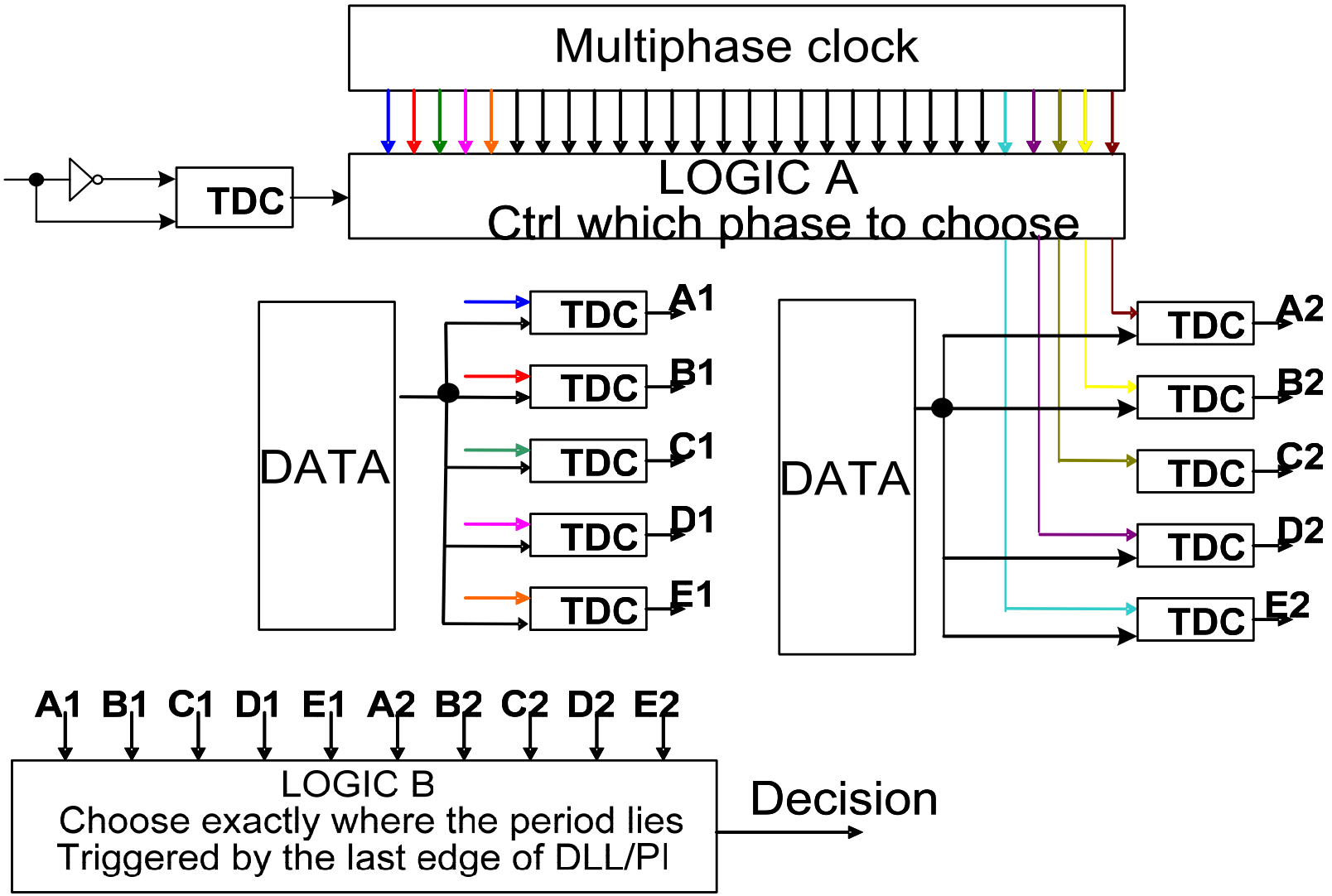


Realization issues

- **Counter with tens of ps speed is difficult**
- **Counter is replaced by multiphase clock generator and logic**
- **[5] has shown 10 ps multiphase clock is possible in TSMC 0.18 μm**

[5]“A Sub-10-ps Multiphase Sampling System Using Redundancy” Lee. Li, Weinlander. D, Yang. C-K K

Clock Recovery Stage



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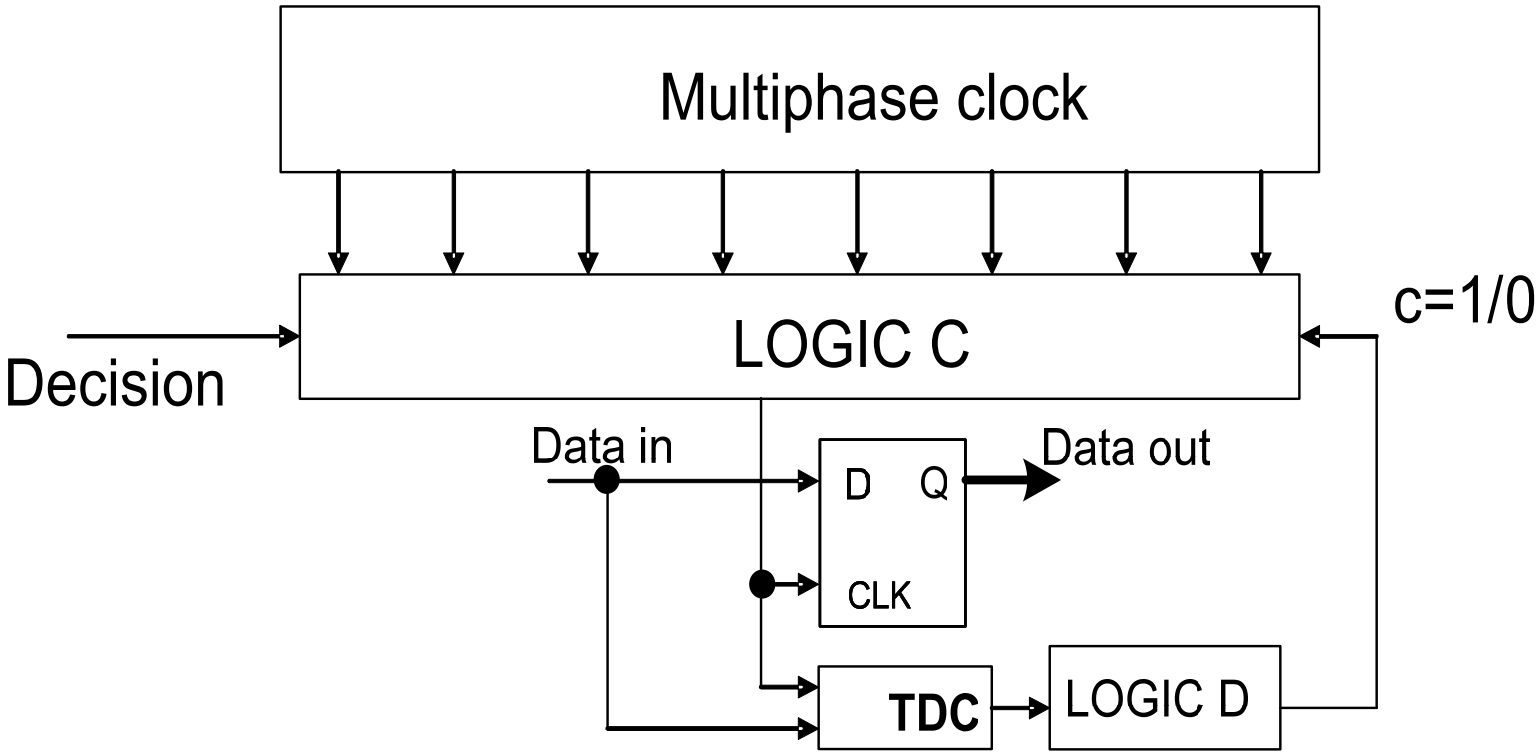
Data Recovery Stage



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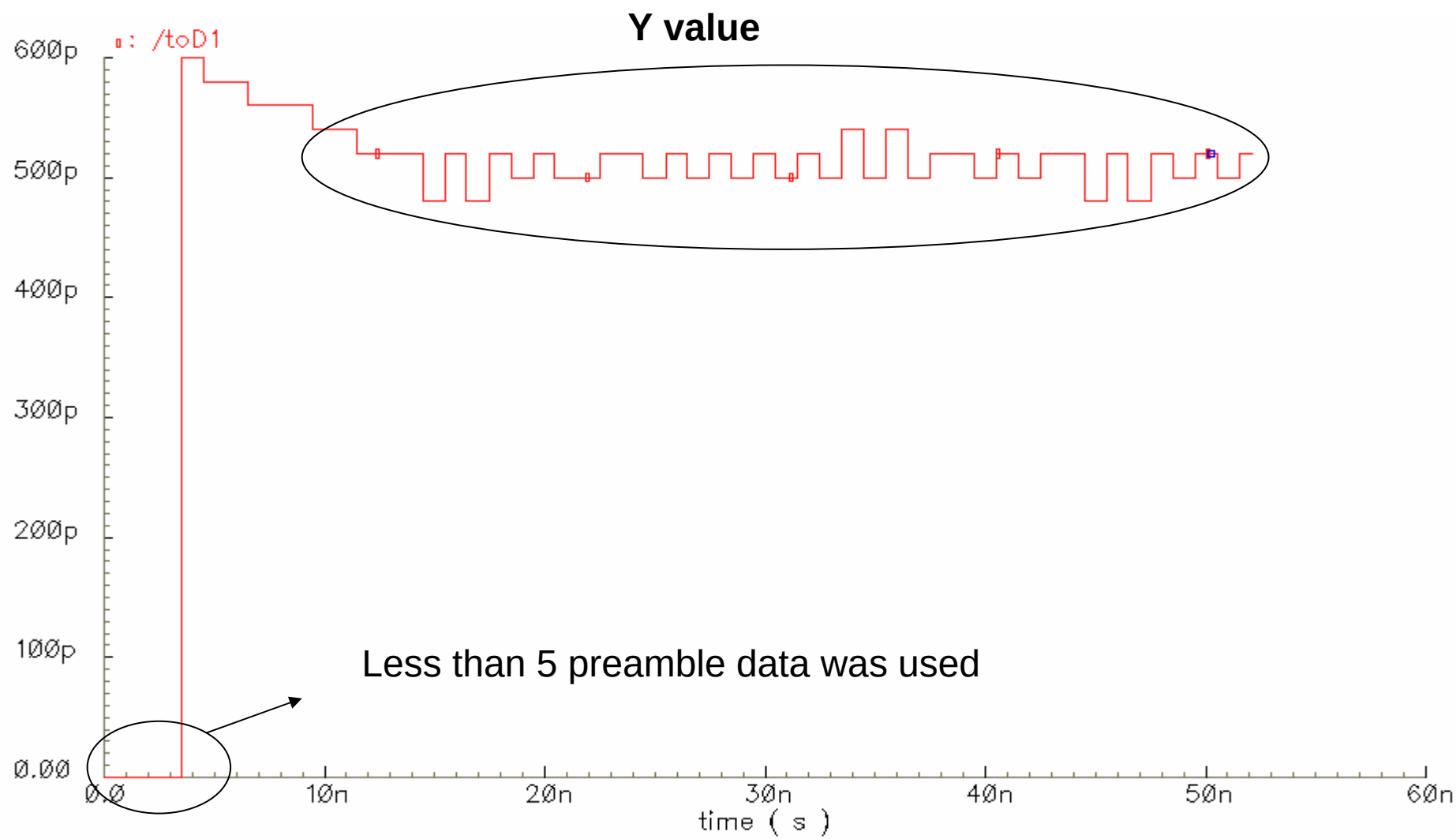
With logic and ideal Multiphase clock



Merit and demerit

MERIT

- Fast lock
- Infinite frequency acquisition range
- Robust
- Scalable

DEMERIT

- Jitter occurs in every data sampling

(deterministic jitter)

- Jitter depends on data type

Deterministic Jitter is dependent on digital resolution. As technology scales, jitter will reduce as well

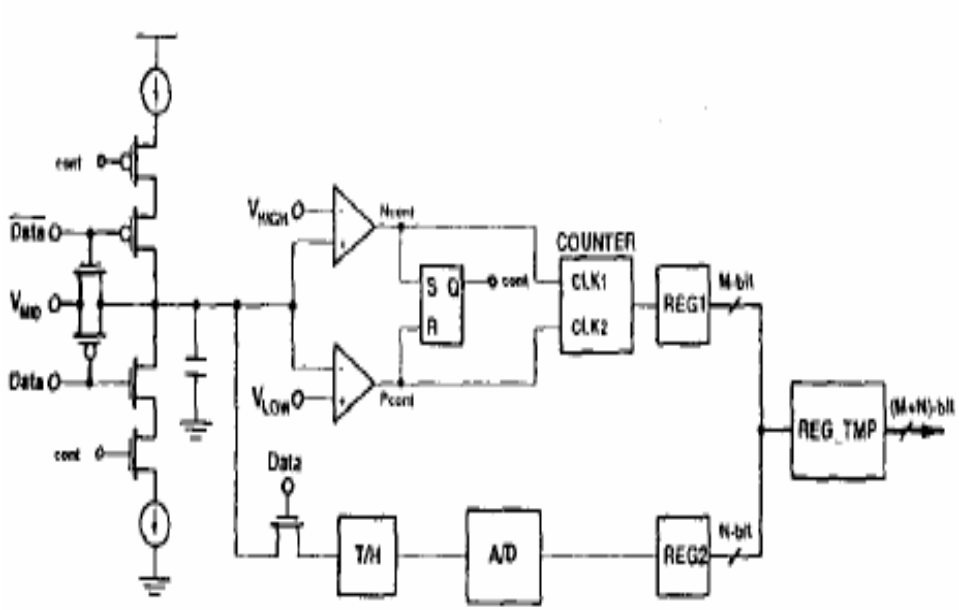
Comparison to PLL

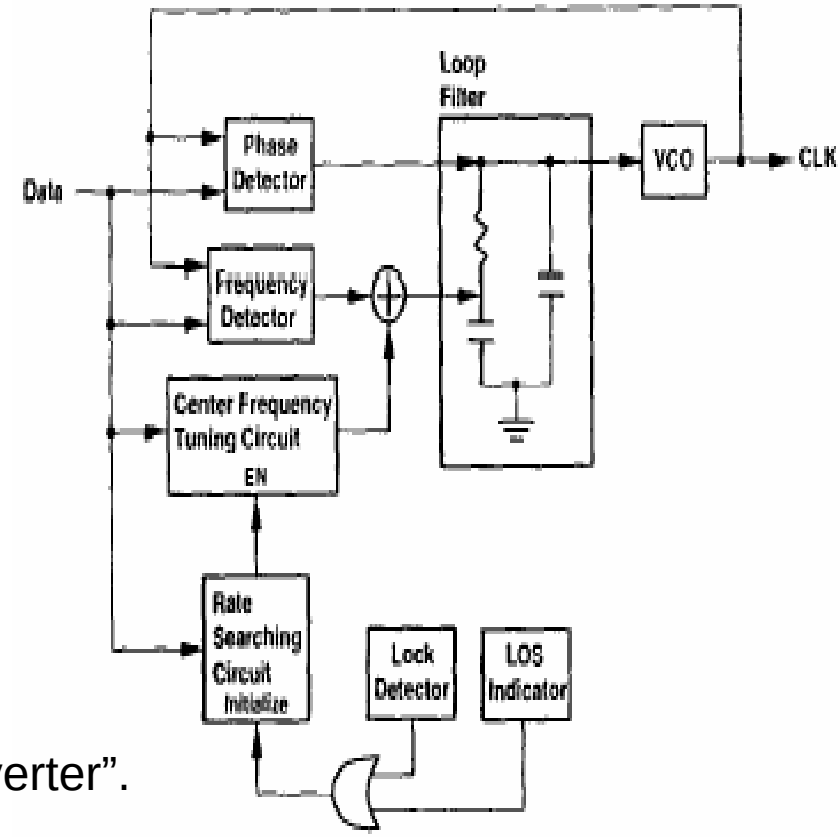
	PLL based CDR	Proposed CDR
Lock Time	> 100 preamble data. Depends on loop bandwidth	A few data bits
Jitter	Depends on analog block's noise, loop bandwidth, mismatch & variations	Depends on TDC resolution & multiphase clock jitter
Freq acquisition	Finite	Depends on TDC memory capacity, theoretically infinite
Scalability	NO	YES

Comparison to Oversampling

	Oversampling CDR	Proposed CDR
Lock Time	Within a few data bits	Within a few data bits
Jitter	Depends on multiphase clock jitter	Depends on TDC resolution & multiphase clock jitter
Response to Change of Input freq	Take time for the multiphase clock to relock	Fast, only a few data bits
Scalability	YES	YES

Comparison





[1] "An Auto-Ranging 50-210Mb/s Clock Recovery Circuit with Time-to-Digital Converter". ISSCC'99, Seoul National University

Use 3 analog loop, lock time takes several μ sec

PRBS 2^8-1 ⇒ **P-P Jitter 280 ps**

Summary and Features

- **A new concept for Full digital CDR has been verified in verilog-A**
- **The proposed CDR has infinite frequency acquisition.**
- **The highest operating frequency is only limited to speed of digital circuit.**
- **Scalable, and as device shrinks, jitter and speed are automatically improved**
- **To sum up, fast lock, mobility, robustness, and scalability is this circuit's main attraction**

Future Works

- **Phase detection and Phase compensation circuit**
- **Improvements against data jitter (Jitter tolerance)**

Reference

[1] “An Auto-Ranging 50-210Mb/s Clock Recovery Circuit with Time-to-Digital Converter”. Park, Joonbae; Kim, Wonchan
[2] “Phase Interpolator Using Delay Locked Loop”. Kim, Taesung, Kim, Beomsup
[3] “A 0.5um CMOS 4Gb/s serial link transceiver with data recovery using oversampling.” C.-K. K. Yang, R. Farjad-Rad, M. Horowitz.
[4] “A Multibitrate Burst-Mode CDR Circuit With Bit-Rate Discrimination Function From 52-1244Mb/s.” S. Kobayashi, M. Hashimoto
[5] “A Sub-10-ps Multiphase Sampling System Using Redundancy” Lee. Li, Weinlander. D, Yang. C-K K