Study on Full Digital Clock Data Recovery

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The purpose of this study is to develop a digital method to reduce lock time and preamble data in Clock Data Recovery circuits (CDR). Digital components ensure robustness against process variations and scalability compare to analog components. The under study CDR utilizes Time to Digital Converter (TDC) to have theoretically infinite frequency acquisition and digital circuit to increase lock time. The concept has been verified in system level simulation, and shown to be able to lock within less than 100 ns.