

Feed-Forward Compensation Technique for All Digital Phase Locked Loop Based Synthesizers

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Abstract— A method of direct input reference feed-forward compensation is proposed and discussed for all digital phase locked loop based synthesizers. The practical issues in implementing the system are addressed, and analysis of the feed-forward estimation error on the system is performed. A sample model was created and simulated. Simulation shows the effect of the feed-forward estimation error on the system's settling speed. The system was shown to be able to reduce the settling time to one eighth of the minimum achievable settling speed of a system without feed forward compensation.

I. INTRODUCTION

Traditionally digital phase-locked loops (DPLL) and more recently all digital phase-locked loops (ADPLL) based frequency synthesizers have been the preferred system for frequency synthesis due to its capability in generating relatively low phase noise reference signals, accurate settling characteristics, and ability to switch between non-integer frequencies. The limitations of PLL based systems are, however, evident. Being a feed-back system the trade-off between settling time upon a frequency switch, and the settling characteristics (output phase noise of the settled system) is inherent, and dependent upon the loop bandwidth.

Various techniques have been proposed to alleviate this problem. One of the most popular techniques that have been studied to alleviate this tradeoff is the control of the system's loop bandwidth. This technique has been studied and published in several papers, for example in [1]. The need for complex control algorithms, or analog circuit design,

however, is often necessary to implement this type of system. Other techniques that have been studied include, for example, the use of a non-linear element in the loop as in [2], and the use of binary search algorithms for ADPLL as in [3].

This paper proposes and analyzes the effects of direct feed-forwarding of the reference control signal for a class of phase-domain ADPLL structures described in [4-6] to speed up the settling time of the ADPLL. From this point forth, this system will be referred to as the feed-forward PLL, and should not be confused with PLL utilizing a feed-forward path in the loop filter as described in numerous references.

II. FEED-BACK PLL SYSTEMS UTILIZING INPUT REFERENCE FEED-FORWARDING

The linear continuous time model of the PLL is often represented as shown in Fig. 1 where $\omega_{ref}(s)$ represents the input reference frequency, θ_{ref} is the reference phase, $e(s)$ is the error signal, $F(s)$ represents the loop filter, $K_{vco}(s)$ is the voltage controlled oscillator (VCO) gain, ω_{fvc0} is the free running VCO frequency, $\omega_{out}(s)$ is the output frequency, and $\theta_{out}(s)$ is the output phase. A problem with the PLL system, as with all feed-back systems is that the system must incrementally adjust the output frequency and phase to be in line with the reference input. However, the part of the signal which contributes to this incremental change is the error signal $e(s)$ which is small and continues to decrease as it has been subtracted from the reference. It is then well known that the settling time of the system depends on system's loop bandwidth.

Mathematically, it is possible to conceive a system which feed forwards the input reference to the VCO's input bypassing the subtraction and loop filter as shown in Fig. 2. From the control system's perspective, this system treats the input reference signal as a disturbance to the system. When the input reference frequency changes, the system is

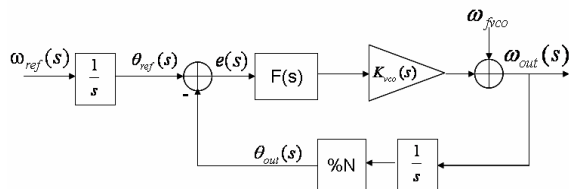


Figure 1. Linear continuous-time model of the PLL.

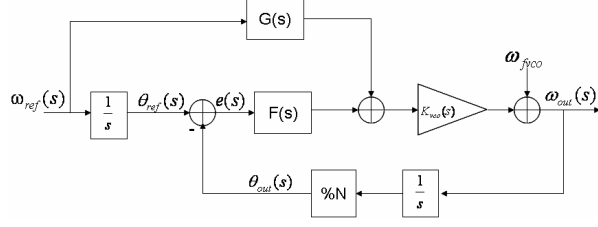


Figure 2. Conception of the feed-forward PLL.

disturbed and attempts to correct the error by feed-forwarding the reference change through the transfer function $G(s)$ which relies on know information about the system. This feed-forward signal sets the initial voltage to the VCO to predict the final value of the control voltage to the VCO. The remaining error due to the approximation is then corrected by the feed-back path.

From Fig. 2 it is seen immediately that the feed-forward compensation system is difficult to implement especially in an analog system as the function $G(s)$ requires the conversion of the input frequency to output voltage. The only reference known to the authors utilizing feed-forward compensation with the feedback loop in a phase-locked loop synthesizer is [7]. However, the system proposed in [7] does not directly use the input reference signal as shown in Fig.2 but instead utilizes the loop characteristics. In addition it is difficult to implement in practice as it requires pre-fabrication of the VCO to measure its characteristics, complex digital signal processor to control both the frequency divider and necessitates the use of a digital to analog converter to generate the feed-forward signal.

III. PROPOSED FEED-FORWARD SYSTEM

The proposed feed-forward all-digital PLL system is shown in Fig. 3. The input reference can be either a frequency control word (FCW) as in [5], or the output of a frequency to digital converter (FDC) or time to digital converter (TDC) similar to the one in the feed-back path as proposed in [5-6]. The phase-detector (PD) is just an adder, and the low pass filter (LPF) is a digital low-pass filter. The feed-forward function (FF function in Fig.3) is a mathematical operator as will be shown later. The digital controlled oscillator (DCO) can be either a digitally controlled inverter chain ring oscillator or LC oscillator.

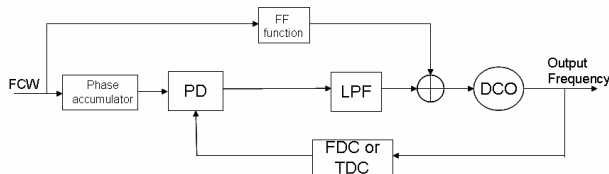


Figure 3. Conception of the feed-forward PLL.

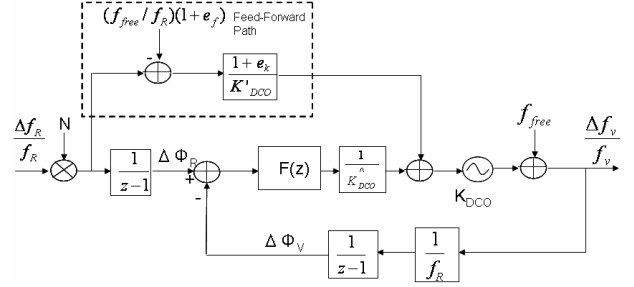


Figure 4. ADPLL feed-forward model.

A linear model of the feed-forward ADPLL is shown in Fig. 4 adapted to include the feed-forward path and scaling factors from [5]. The input reference $\Delta f/f_R$ is the time step unit value reference, N is the ratio between the wanted frequency at the output of the PLL and the reference frequency f_R . The function $F(z)$ is the digital low-pass transfer function while K_{DCO} is the DCO gain scaling constant. K_{DCO} is the DCO gain constant, K'_{DCO} is K_{DCO}/K_{DCO} , f_{free} is the free running VCO frequency, e_f represents the error in estimating the DCO's free running frequency while e_k represents the error in estimating the DCO's gain.

Neglecting the feed-forward path, the transfer function of the model in Fig. 4 can be found to be (1)

$$\frac{\Delta f_v}{f_v} = \frac{(N \cdot F(z) \cdot K'_{DCO})}{f_R \cdot (z-1) + F(z) \cdot K'_{DCO}} \cdot \frac{\Delta f_R}{f_R} + \frac{f_{free} \cdot (z-1) \cdot f_R}{f_R \cdot (z-1) + F(z) \cdot K'_{DCO}} \quad (1)$$

The first term of (1) represents the response of the system output to input change while the second term represents the offset due to the DCO's free running frequency which is unaffected by the change in reference input. The phase transfer function is similar and can be obtained by noting that $(\Delta f_R/f_R) \cdot (N/(z-1)) = \Delta\theta_R = N\phi_R/(2\pi)$, $\Delta\theta_V = \phi_V/(2\pi)$, and $f_{free}/(f_R(z-1)) = \phi_{free}/(2\pi)$.

From Fig. 4, it is seen that in this system, the feed forward path consists of two components. The first component f_{free}/f_R models the scaled version of the DCO's free running frequency. The second component $1/K'_{DCO}$ models a scaled version of the DCO's gain. Note that in this particular example scaling factors were present due to the account of certain practical aspects in the system's implementation. The general idea, however, applies to the general feed forward system. Taking into account the feed-forward path, but neglecting the errors e_f and e_k for the time

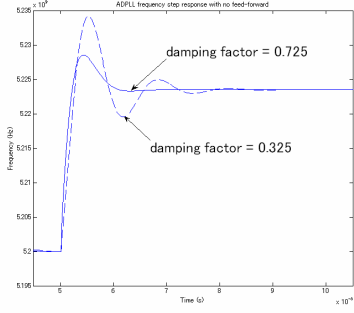


Figure 5. PLL response to a frequency step without feed forward compensation.

being (2) can be derived.

$$\frac{\Delta f_v}{f_v} \cdot \left(1 + \frac{F(z) \cdot K_{DCO}}{f_R \cdot (z-1) \cdot \hat{K}_{DCO}} \right) = \frac{\Delta f_R}{f_R} \cdot \frac{N \cdot F(z) \cdot K_{DCO}}{(z-1) \cdot \hat{K}_{DCO}} + \frac{\Delta f_R}{f_R} \cdot \frac{N \cdot K_{DCO}}{\hat{K}'_{DCO}} - \frac{f_{free} \cdot K_{DCO}}{f_R \cdot \hat{K}'_{DCO}} + f_{free} \quad (2)$$

from which if $\hat{K}_{DCO} = f_R$ (2) will become (3)

$$\frac{\Delta f_v}{f_v} = N \cdot f_R \cdot \frac{\Delta f_R}{f_R} \quad (3)$$

Since N is the ratio of the output frequency to the input reference f_R (3) basically states that the output will change to become the desired frequency instantaneously. However, in reality, it is impossible and impractical for such a system to exist, since the point of the feedback system is to control a unit (in this case DCO) which cannot be modeled 100% correctly. In other words, if it is possible to model the unit we want to control 100% correctly, a feedback system would not be necessary, and the system can be controlled directly.

Finally, taking into account the modeling error of the DCO, again taking $\hat{K}_{DCO} = f_R$ (4) can be derived.

$$\frac{\Delta f_v}{f_v} = \frac{\Delta f_R}{f_R} \cdot N \cdot f_R + \frac{\Delta f_R}{f_R} \cdot N \cdot f_R \cdot \frac{e_k \cdot (z-1) \cdot f_R}{(z-1) \cdot f_R + F(z) \cdot K'_{DCO}} - \frac{(e_k + e_f + e_f \cdot e_k) \cdot (z-1) \cdot f_R}{(z-1) \cdot f_R + F(z) \cdot K'_{DCO}} f_{free} \quad (4)$$

Equation (4) contains three components. The first is the same as (3) and represents the part of the feed forward function which has cancelled out with the ADPLL's loop parameters. The second term represents an error which is initially proportional to the step input and error in modeling

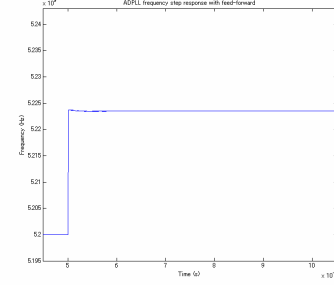


Figure 6. PLL response to a frequency step with 1% error feed forward compensation.

the DCO's gain, and decreases according the loop parameters. The third component is an error offset due to the error in estimating the DCO's free running frequency, and gain which is independent of the frequency switching and will be compensated by the feedback system just as the second term.

IV. IMPLEMENTATION CONCERNS AND SIMULATION

Since the feed-forward path is designed for an ADPLL system, implementation concerns are simplified. As the input reference is numerical, and the DCO's input is also numerical, the feed-forward function can be implemented mathematically using standard digital circuitry. The DCO's free running frequency can be found by breaking the loop at the feed back path, directing feeding a '0' input into the DCO, and storing the output of the TDC/FDC. This is achieved simply by adding a multiplexer before the DCO and tapping the feed back path. In general, this measurement can be expected to be almost exact with the effective resolution equaling the TDC/FDC error, which is the system's resolution. The DCO gain can be obtained by tapping the DCO control word (DCO) for two different frequencies shown in [5]. All this is performed in the calibration phase.

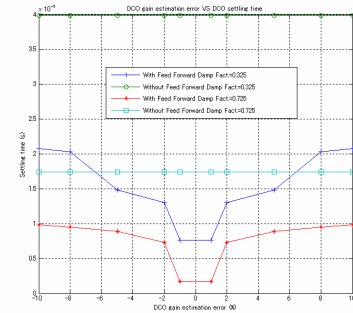


Figure 7. PLL settling time VS DCO gain estimation error

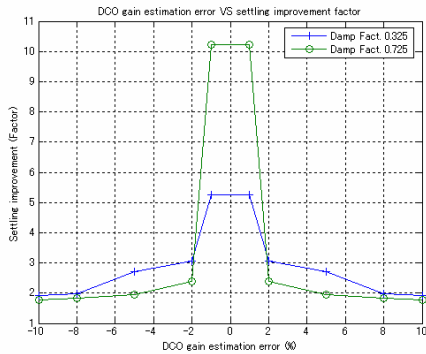


Figure 8. PLL settling improvement factor VS DCO gain estimation error

A linear discrete-time model of the ADPLL with and without a feed forward path was modeled in Matlab. The reference frequency was 10MHz, and a low pass filter with one pole and one zero was chosen. The free running DCO frequency was 5GHz. The input was switched such that the frequency output stepped between 5.2GHz and 5.2235GHz, a 23.5MHz step frequency. The PLL system response without feed-forward is shown in Fig. 5, while the system in Fig. 6 is the simulation of the system with 1% error in DCO gain estimation in the feed-forward path. A minimum error of 1% was chosen as it was mentioned in [5] as an achievable value for DCO gain estimation. Aside from the reduced settling time, it is observed that the feed-forward also limits the overshoot of the system, making it less dependent upon the damping factor.

Fig. 7 plots the settling time of the ADPLL system with feed-forward for various gain estimation errors compared with the system without feed forward where settling is defined as the time taken by the PLL system to settle within 10ppm (part per million) of the final value for two damping factor values 0.325 and 0.725. Fig. 8 shows the settling time improvement factor of the feed forward system when compared with the system without feed forwarding calculated by dividing the needed settling time of the non-feed-forward system by the feed-forward system. A maximum settling improvement of approximately 10 (at 1% DCO gain estimation error) can be observed from this example for the damping factor of 0.725.

In practice, the settling improvement factor depends on the loop parameters and settling criterion. Fig. 9 plots the PLL settling time and improvement factor against the system's damping factor. A settling improvement factor of 8 is observed at the PLL's minimum settling time without feed forward at the damping factor of 0.825. Note the sudden jumps in settling improvements for example when the damping factor changes from 0.7 to 0.725. This occurs as a result of the defined settling criterion which necessitates the

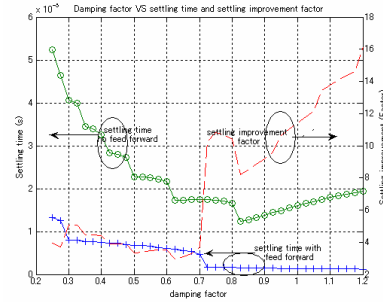


Figure 9. PLL damping factor versus settling time and settling improvement

overshoot and undershoots ripples become lower than a certain critical point before it is considered settled. For this reason if an over or undershoot does not meet the settling criterion it must take some time until the next or following over or undershoot ripple has met the settling criterion.

CONCLUSION

A powerful method for settling speed improvement of ADPLL was introduced. The feed forward compensation for ADPLL system was proposed and critical factors concerning the settling improvement (the DCO gain estimation) was analyzed. Analysis was performed on the discrete time model of an example system, and simulation has shown the ability of the feed-forward system to improve the setting speed of the system. In practice achievable settling speed improvement depends on the loop parameters and settling criterion. Dynamic gain correction by reusing the system's error signal output may enable greater improvements in the system's settling speed.

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