A Background Optimization Method for PLL by Measuring Phase Jitter Performance

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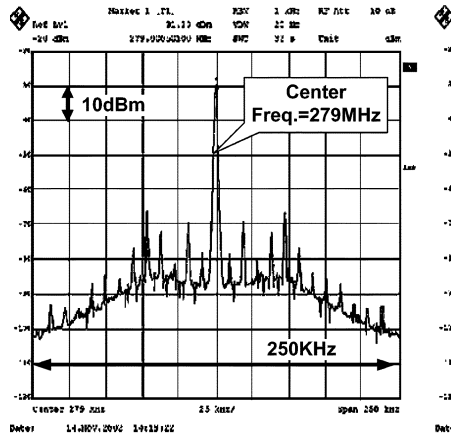
***Abstract*—This paper describes a background (BG) optimization method for a phase-locked loop (PLL) by changing the circuit parameters of the PLL circuits. Measuring the phase shift of the voltage-controlled oscillator (VCO) at each input reference clock, we can determine the phase jitter performance with accuracy equal to a time interval analyzer (TIA). Using the combination of the global optimization method at initial stage and the local optimization method for the background calibration always gives the PLL the smallest jitter performance under process variation, supply voltage modulation, and temperature variation. The test environment fabricated by the 0.15-μm CMOS controlled by an external FPGA demonstrates enough ability to suppress the impacts of the environmental variations.**

***Index Terms*—Background, CMOS, noise suppression, optimization, phase jitter, phase-locked loop (PLL).**

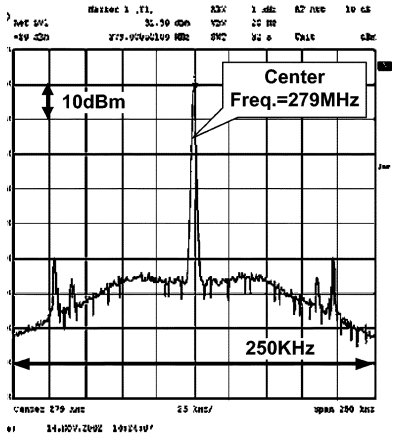
I. Introduction

THE phase-locked loop (PLL) is a very popular circuit component of system LSI. Every system LSI has at least one PLL circuit. PLLs for system LSI are improving for low-voltage and high-speed operation [1]–[3]. Increasing the speed of the digital circuit causes large digital noise, which degrades the performance of the PLL [4]. Moreover, lowering the supply voltage of the PLL also causes large jitter to the PLL by reducing the dynamic range of the voltage-controlled oscillator (VCO). Therefore, the noise problem is becoming the main issue in PLL design. The substrate noise or supply noise di/dt affect the PLL jitter performance. The EDA tools or the design method for analyzing such digital noise are improved day by day [5]–[7]. However, we must fix the PLL design before full chip design is completed. Thus, it is very difficult to predict the impact of the noise on the PLL, because we hardly predict the noise from the digital block without the layout information of the chip and the parasitic information of the board. Some papers show the qualitative way of decreasing the effect by digital noise [8] and the elaborate circuits for reducing the digital noise impact [9], [10]. In spite of such efforts, we have not been able to estimate the effect quantitatively yet.

Moreover, it will be very hard work to estimate the transfer characteristics of such digital noise to a PLL. The PLL is very sensitive to digital noise. Especially, in case of the PLL with high divider ratio, the inclination is remarkable. For example, Fig. 1(a) and (b) shows the output spectrum from the PLL applied 10-MHz and 10.1-MHz digital noise from substrate respectively. In spite of only 1% difference of the noise frequency, the output spectra are very different from each other. In order to maintain the best performance by avoiding the influences from digital noise, a PLL must have some new functions. In this paper, we show the first attempt to avoid the accidental effects in the PLL such as digital noise, power supply noise, process variation, and temperature variation. A background (BG) calibration method to keep the minimum jitter is described in this paper. This new method can also optimize the performance of the PLL against several variation factors such as process and temperature variations. The system configuration of the PLL with optimization system is shown in



(a)Noise Freq. is 10.0MHz



(b) Noise Freq. is 10.1MHz

Fig. 1. PLL output spectrum with substrate noise.

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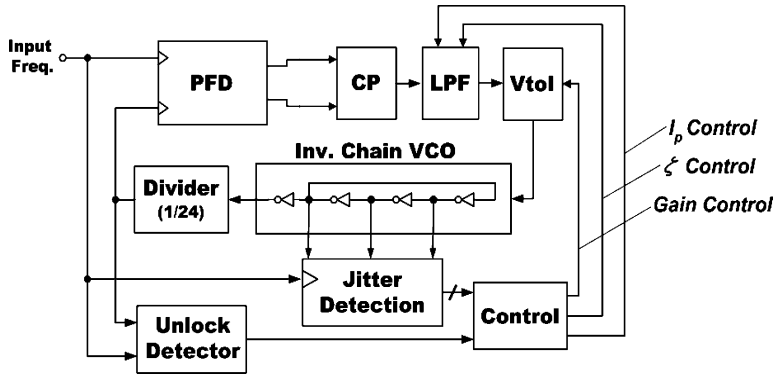

Fig. 2. Block diagram of the PLL with BG calibration.

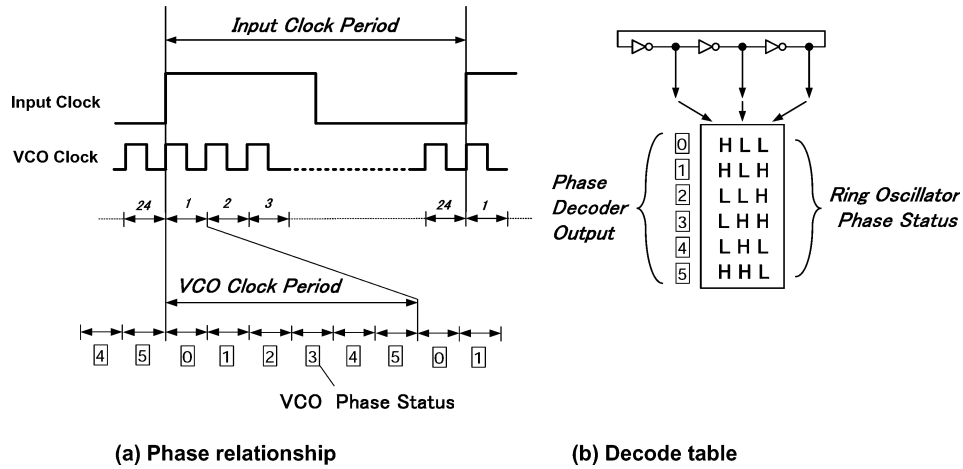

Fig. 3. Concept of jitter detection.

Section II. The concept of the jitter detection is explained in Section III. In Section IV, the circuit configuration of the PLL is described and the detail of the optimization method is shown in Section V. Finally, the chip layout and measurement results are illustrated in Section VI.

II. System Configuration

Fig. 2 shows a block diagram of the PLL and BG calibration. The PLL is conventional charge pump type which can output 1-GHz oscillation clock. The divider ratio is 24. The VCO has three inverters. The jitter detector (JDET) monitors the phase of the ring oscillator at every input clock and detects the phase change, which is accumulated for enough time. The concrete period is discussed in Section VI. The output of the JDET is digital code so that the controller can change the PLL response nonlinearly. The amount of phase changes of the ring oscillator indicates the jitter value directly. According to the jitter value from JDET, the controller optimizes the control codes of the charge pump current, damping factor and VCO gain so that the phase jitter is minimized.

The controller changes the parameter of the PLL very widely. Thus, there is possibility that the PLL goes into unlock status due to inappropriate parameters. When the PLL goes into unlock status during the optimization, the unlock detector detects the status and forces the controller to neglect the output of the JDET according to the unlock signal in order to omit the unnecessary measurement. This algorithm is for defining the unlock area of the control codes. Decision of the unlock area in the global optimization is helpful for preventing the unlock state in the local back ground optimization.

III. Concept of the Jitter Detection

Fig. 3(a) and (b) illustrates the concept of the jitter detection. Fig. 3(a) shows the relationship of the VCO phase to that of the input clock. Generally, n-stage inverter chain oscillators have $2n$ phases [11]. In our case, a three-stage inverter chain was used and the divider ratio is 24. Therefore, when the PLL is locked, the input clock is divided to $24{*}6 = 144$ phases. Assuming that the PLL has no jitter, the phase status of the VCO, which is monitored at the edge of the input clock, is always the same. However, the actual PLL has some jitter. The phase information of the VCO fluctuates around the center of the lock point. The fluctuation of the ring oscillator phase directly expresses the jitter value. Thus, we can estimate the jitter value by differentiating the phase information. In this case, we can estimate the phase jitter to the resolution of 0.7% (1/144). According to our internal jitter measurement results of several system LSIs, the average phase jitter of the PLL is about 1% of the input clock [12]. Thus, the resolution is enough to measure the jitter.

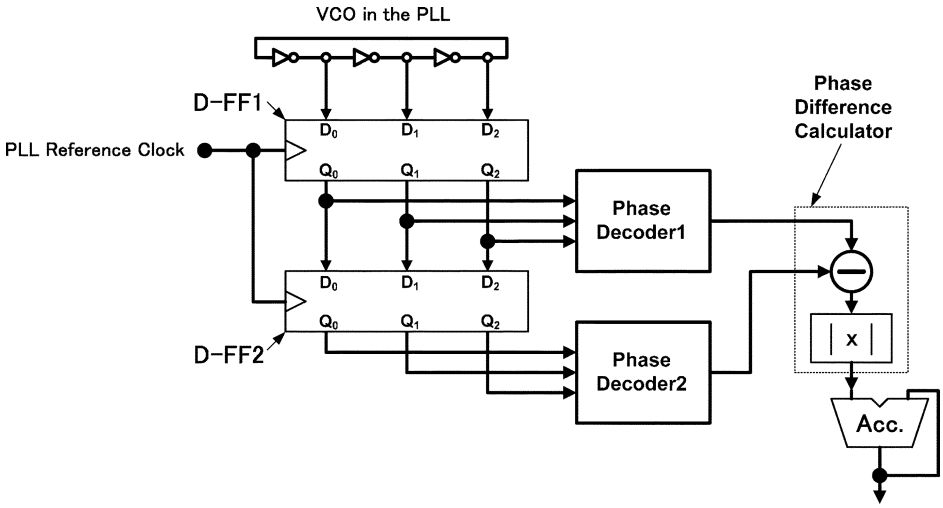

Fig. 4. Block diagram of the jitter detector.

Fig. 4 shows the block diagram of the JDET. The JDET is composed of two D-flip-flops (D-FF1 and D-FF2), phase decoders, phase difference calculator, and accumulator. The phase status of the ring oscillator is latched by D-FF1. The phase information at previous edge of the input clock is moved to DFF2. The 3-bit outputs of D-FF1 and D-FF2 is decoded by the phase decoder according to the rule shown in Fig. 3(b). The output of the phase decoder is digits numbered from 0–5. This is the quantized phase information of the VCO. The phase difference calculator calculates the phase difference of the outputs of the two decoders. For example, if the output of decoder 1 is 0 and that of decoder 2 is 2, the phase difference is 2. However, if the output of decoder 1 is 0 and that of decoder 2 is 4, the phase difference is not 4 but 2, because the calculator selects the smaller of the two candidates.

Finally, the output of the phase difference calculator is accumulated enough times to remove the influence of the background noise. The length of the accumulation is discussed in Section VI.

Fig. 5 displays the comparison of the phase jitters between the JDET and a time interval analyzer (TIA). In this case, the control code of the VCO gain was a constant value (120) and the oscillation frequency of the VCO was 1 GHz. The strong correlation of two broken lines in Fig. 5 shows that the JDET has good accuracy equal to the TIA. Taking into account the fact that the JDET has no influence from the BG noise such as phase noise caused by I/O, the JDET will be more accurate than the TIA.

IV. Circuit Configuration

The PLL can digitally change the charge pump current, damping factor and VCO gain digitally. The control bit width of I_p, ζ, and K_o is 8, 2, and 8, respectively.

Fig. 6 depicts the circuit schematic of the PLL and Fig. 7 shows the mechanism of the generation of the deterministic jitter, respectively. When impulse input train such as the error current between charge and discharge current of the charge pump enters the PLL, impulse responses of the PLL are convolved. The convolution of the impulse responses generates the

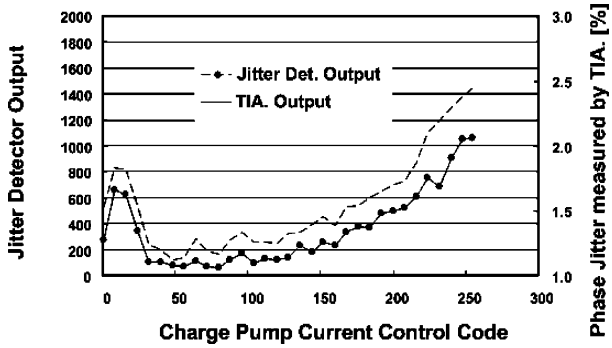

Fig. 5. Comparison of the jitter measurement results.

static phase error and the deterministic jitter which has the same period of the input signal. If impulse input train has the same period of the input clock, the period of the deterministic jitter is the same as that of the input clock. Thus, the deterministic jitter does not contribute to the phase jitter. This means that we cannot optimize the deterministic jitter by measuring the phase jitter.

Therefore, we have to minimize the deterministic jitter with another way. We adopt the active current mirror technique in order to minimize the difference between the charge and discharge currents of the charge pump circuit.

Fig. 8 displays the state-machine diagram of the phase frequency detector (PFD) and Fig. 9 shows the schematic of the unlock detector. Fig. 8 clearly shows that the unlock transitions occur when two succeeding rising edges enter REF_IN or VCO_IN.

Therefore, the unlock detector is composed of the PFD and DFFs, which is connected to the output of the PFD. When the unlock detector finds the two succeeded rising edge, the detector outputs the unlock signal. In such case, the output of the jitter detector is neglected.

Another characteristic of the circuit configuration is the offset bias control. During the BG optimization, we have to control the offset bias current of the VCO so that the phase error caused by the 1-bit change of the VCO gain can be suppressed within the tolerance level.

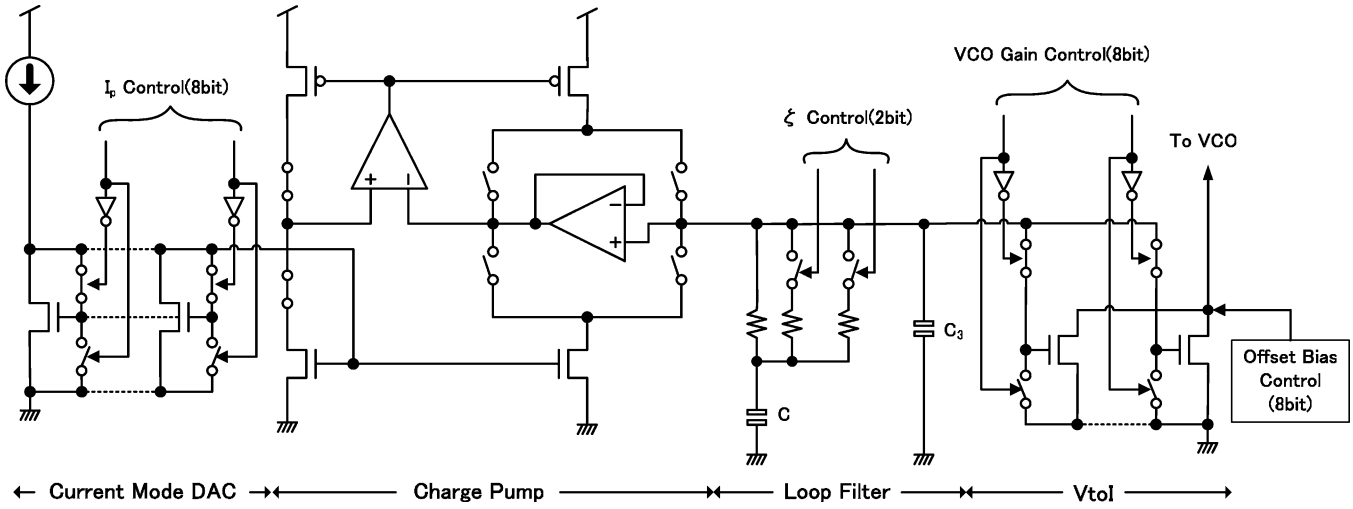

Fig. 6. Schematic of the control for the PLL parameter.

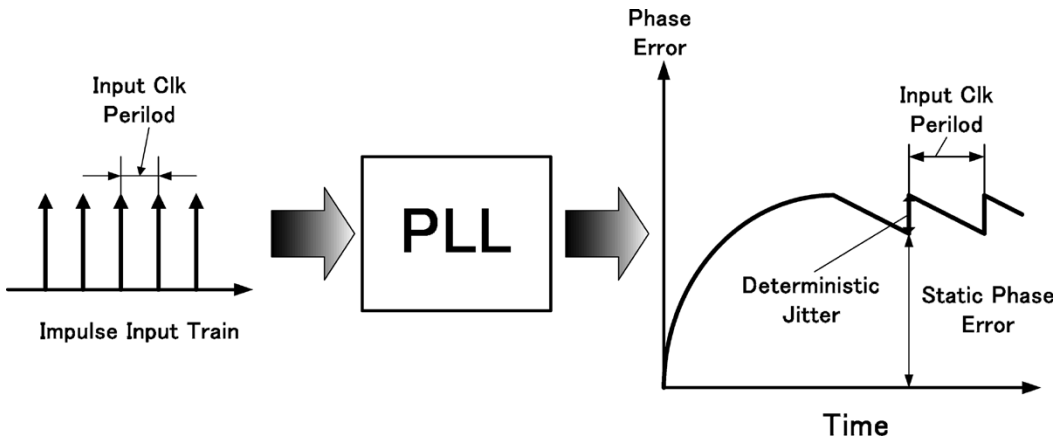

Fig. 7. Mechanism for the generation of the deterministic jitter.

The optimized open-loop transfer function of the PLL ($H_{\rm opt}$) is given by

$$H_{\rm opt} = \frac{\omega^2\sqrt{b}\left(s+\frac{\omega}{\sqrt{b}}\right)}{s^2(s+\omega\sqrt{b})} \tag{1}$$

where ω is the natural frequency and b is $1+{\rm C}/{\rm C}_3$ [13] as shown in Fig. 6. $\rm C_3$ is the main capacitor to suppress the pattern jitter and $\rm C$ is main capacitor of the loop filter. The transfer function from the input frequency change to phase error ($H_{\rm err}$) is given by

$$H_{\rm err} = \frac{1}{s(1+H_{\rm opt})}. \tag{2}$$

The phase error due to the step change of the input ($=\Delta\omega$) is calculated by the inverse laplace transform of $\Delta\omega \times H_{\rm err}/\,{\rm s}$. In this paper, b is set to 9. The transient response ($F_{\rm err}(t)$) is described by

$$F_{\rm err}(t = \Delta\omega t(\omega t+1)e^{(-\omega t)}. \tag{3}$$

Equation (3) has the maximum value at ${\rm t} = 2(1+\sqrt{5})/\omega$ and the maximum value($\theta_{\rm emax}$) is about $0.84\Delta\omega/\omega$. We have to suppress the phase error within 1% of the input clock period. Thus, the tolerable frequency change is calculated by the following equation. Here, the oscillation frequency of the VCO is 1 GHz and the divider ratio is 24. Hence, the input frequency is about 41.7 MHz. Consequently, we determined ω to be 4 MHz.

$$0.84\frac{\Delta\omega}{\omega} < 2\pi \times 1\%. \tag{4}$$

Solving the relation (4), we obtained that $\Delta\omega < 300$ kHz. As the VCO gain is 62.5 MHz/V, the minimum resolution of the offset bias control must be larger than 62.5 MHz/300 kHz. The ratio becomes about 209. Therefore, the resolution of the digital-to-analog converter (DAC) to generate the offset bias for the VCO was set to 256. When the controller changes the VCO gain, the DAC compensates the change of the bias current of the VCO so that the frequency change of the VCO is lower than 300 kHz.

V. Calibration Method

In the calibration method, we adopt a tandem approach. At first, the global optimization is applied in order to find the best parameter set to minimize the phase jitter. Next, the local BG calibration follows the global optimization to keep the

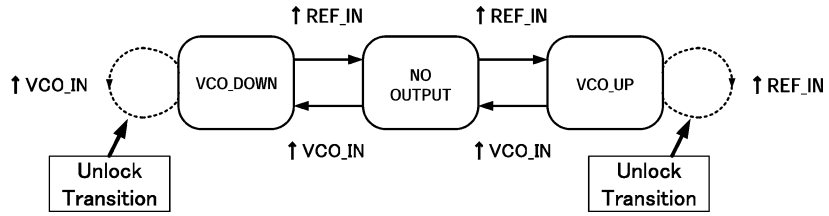

Fig. 8. State-machine diagram of the phase frequency detector.

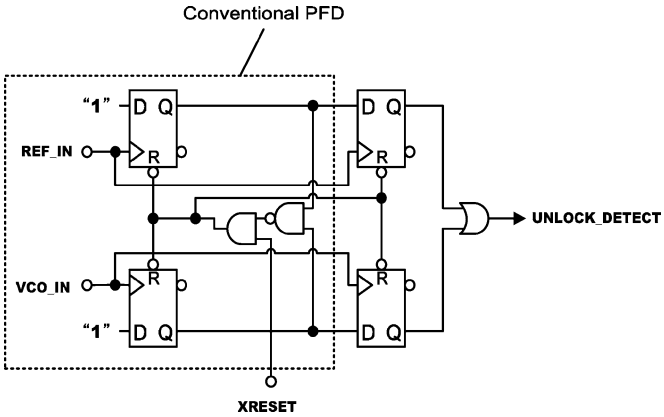

Fig. 9. Schematic of the unlock detector.

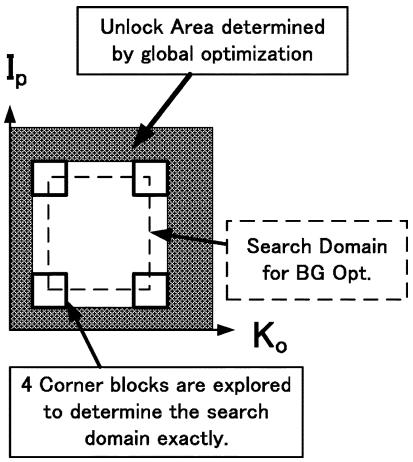

Fig. 10. Search domain of the optimization.

best phase jitter performance against the power supply noise, temperature variation, and so on.

Fig. 10 shows the search domain of the calibration and Fig. 11 represents the global calibration flow chart. In the global calibration, every combination of the control codes is tested, however, the number of the combinations is very large (2^{18}). In order to reduce the test time of the control codes, a coarse–fine combination search was adopted. The control codes of the PLL (K_o, I_p, ζ) are expressed as follows:

$$K_o = 8 + 16 \times I + U \tag{5}$$

$$I_p = 8 + 16 \times J + V \tag{6}$$

$$\zeta = 1, 2, 3, 4. \tag{7}$$

In the coarse global optimization, parameters I and J are changed from 0 to 15 and parameter ζ is changed from 1 to 4. Thus, we divided the code area which includes 256 control codes to 16 blocks. The representative of a block is its center value. The number of the tests in the first global optimization is $16 \times 16 \times 4 = 1024$. Once the parameters are changed, jitter measurement, which includes 32768 times sampling of the VCO phase status, is done after waiting time for PLL acquisition. The waiting time is 4096 input clock.

Next, the codes in the block are explored. Therefore, parameters U and V are changed from -8 to 7 and parameter ζ is changed from 1 to 4. As each block has 16 codes, the number of the tests is equal to the first one. The measurement times is reduced to 1/128 of the whole code exploration. In the global optimization, we are able to find not only the digital codes which minimize the phase jitter, but also the code area in which the PLL is unlocked. In order to search the unlocking area exactly, four additional blocks on the corner in the locking area are explored as shown in Fig. 10.

After the global optimization, the local BG calibration is on standby. Fig. 12 shows the flow chart of the BG calibration. When the jitter detector shows worse value than the threshold, the BG calibration starts. Once the BG calibration is started, the calibration is automatically stopped according to the set schedule. In this case, the calibration is stopped after 32 searches are finished. These algorithms are introduced for preventing the degradation of the jitter performance in steady state of the PLL, because changing the parameter frequently causes the jitter.

The adjustment of the damping factor was not adopted in the BG calibration, because we sometimes found abnormal operation when we included the damping factor adjustment in the BG calibration.

Avoiding the code area where the PLL is unlocked, the controller tests the current code and all adjacent codes, as shown in Fig. 13. After the measurements of the jitter for all adjacent codes, the control code is changed to the code which has the minimum jitter value. The influence of the 1-bit change of the control code must be set so that the transient response of the 1-bit change is small enough not to affect the jitter performance. The time needed for the one step of the BG calibration is about 7 ms. If we reduce the number of the measurement for the ring oscillator phase, we can increase the bandwidth of the calibration.

However, the smaller the number of phase jitter measurement is, the larger the variation of the phase jitter measurement becomes. Thus, there is an upper bound of the bandwidth of the calibration. Actually, our BG calibration system is suitable for

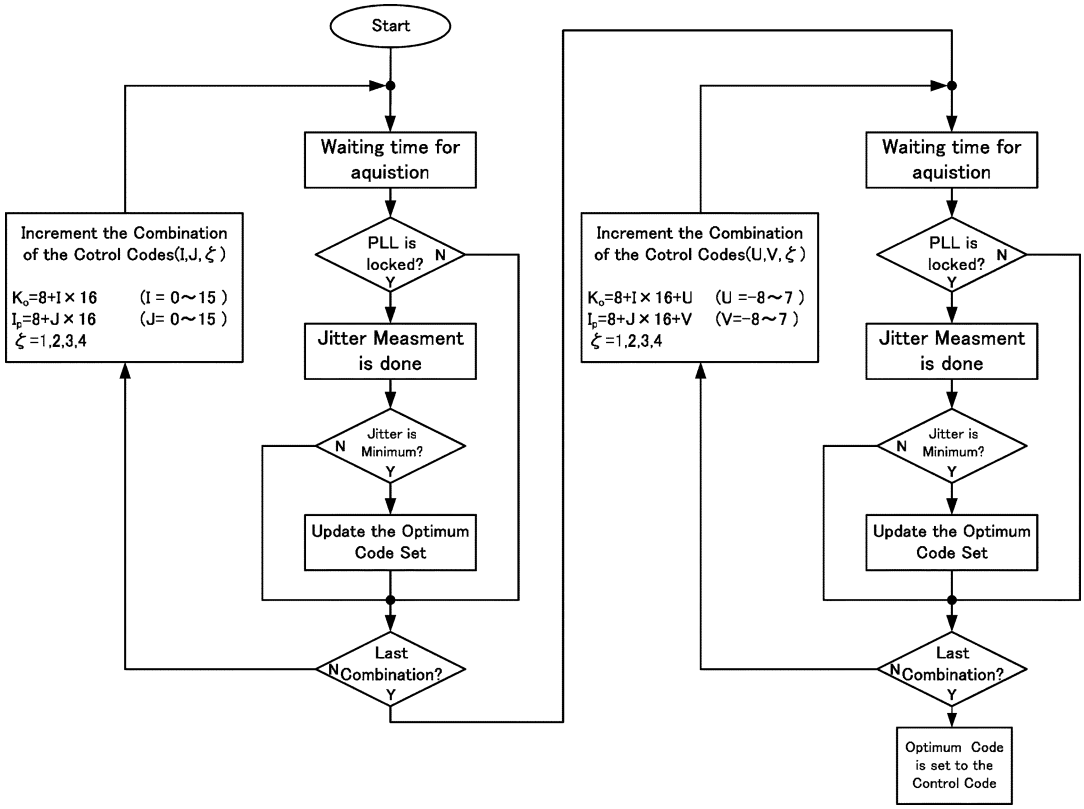

Fig. 11. Global calibration flow chart.

TABLE I
SPECIFICATIONS OF THE PLL

Supply Voltage	1.5V
Output Frequency	2GHz～250MHz
Power Consumption	7.6mW@2GHz-output
Divider Ratio	24

TABLE II
COMPARISON OF THE PERIOD JITTER

	Period Jitter(3σ) measured by Time Interval Analyzer	Output Value from Jitter Detector
without Optimization	1.36%～1.84%	912～1408
with Optimization	1.15%～1.24%	240～786

the compensation of low-frequency drift, such as a temperature variation or an average of the digital noise

Considering the actual use of the PLL, the high-frequency components of the supply voltage noise are removed by the capacitance inserted between the power lines. Substrate noise is significantly reduced by using a triple-well structure. The BG calibration can prove its merits by using such techniques for high-frequency noise reduction.

VI. CHIP LAYOUT AND MEASUREMENT RESULTS

The test chip was fabricated in 0.15-μm CMOS process with a MIM capacitor. Fig. 12 shows the layout pattern of the PLL. Fig. 14 includes the PLL circuit and the DACs for controlling the VCO gain, charge pump current, and offset bias current for the VCO.

The control logic for the calibration is set up in the FPGA outside of the chip in order to change the algorithm easily. Typical number of the gates of the control logic fabricated in the FPGA was about 4000. The FPGA is XC2S200E manufactured by Xilinx. The clock source of the FPGA is the reference clock of the PLL.

Table I summarizes the specifications of the PLL. Setting the output frequency to 1 GHz, the measurements described later were done.

Before the evaluation, we have to decide the measurement length of the jitter long enough to reduce the effect of the measurement error. Shorter measurement length gives less accurate jitter because each sample of the JDET has considerable variation due to the BG noise.

Fig. 15 shows the standard deviation and the peak-to-peak value of the outputs from the jitter detector against the measurement length. The X axis is the number of measurements. One measurement includes 4096 times accumulation of the output from the jitter detector. For example, measurement length of 8 means $8 \times 4096 = 32\,768 \times$ accumulation of the output.

We executed 1000 times trials for each measurement length. Taking into account of the tradeoff between measurement time and the variation of the measurement result, measurement length of 8 (32 768 accumulation of the phase jitter) was selected. If we reduce the measurement length less than 8, the accuracy of the optimization might be degraded. In particular, the reduction sometimes makes the local BG calibration unstable.

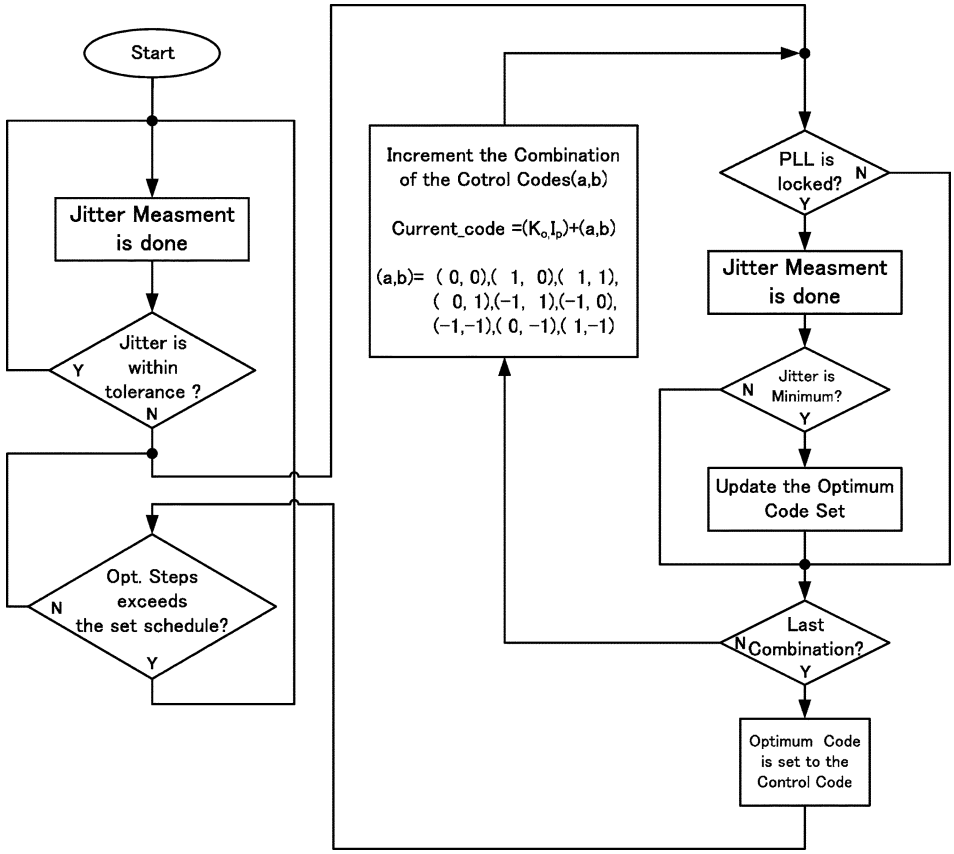

Fig. 12. Local background calibration flow chart.

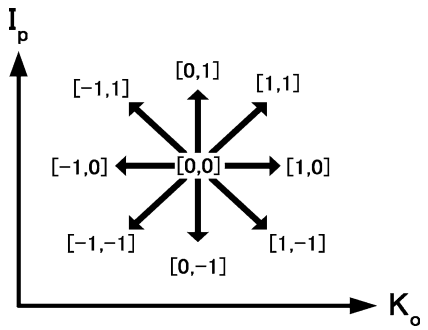

Fig. 13. Control codes for BG calibration.

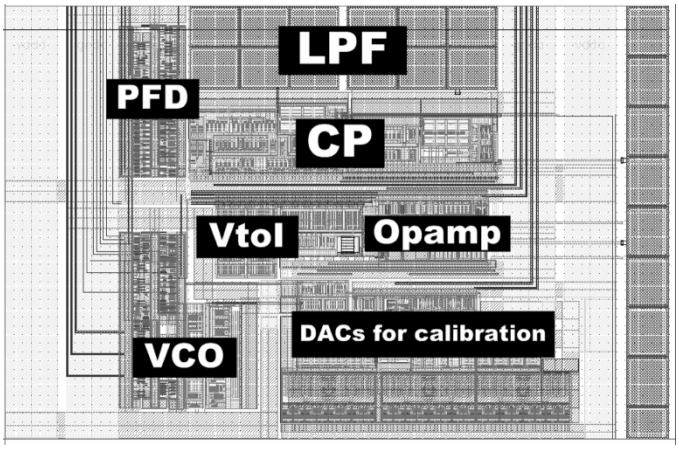

Fig. 14. Layout pattern of the PLL.

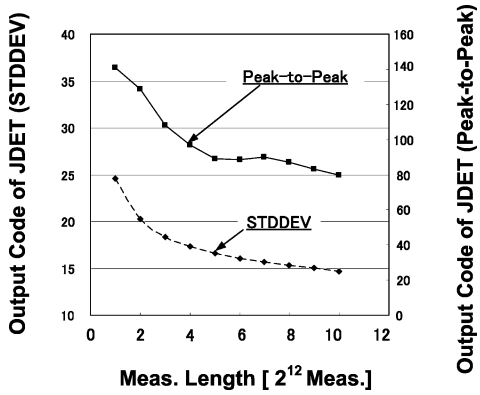

Fig. 15. Statistic values of the jitter detector against the measurement length.

As mentioned above, we need 2048 times measurements for the global optimization. The input clock is 41.7 MHz. Hence, the setting time is about $1/41.7\ \text{MHz} \times 32\,768 \times 2048 = 1.61$ s.

First, we confirmed the effect of the global optimization. Table II shows the comparison of the jitter performances. The number of the test chip for the measurement was 10. Table II clearly shows that the global optimization can suppress the period jitter of the PLL as compared with the nonoptimized case. When we use the TIA for the measurement, jitter reduction of 62%–91% is obtained, while we measured better jitter reduction result of 26%–56% from the internal JDET. The values resulted from JDET are more reliable, because the result of the JDET has no influence from the I/O or board noise.

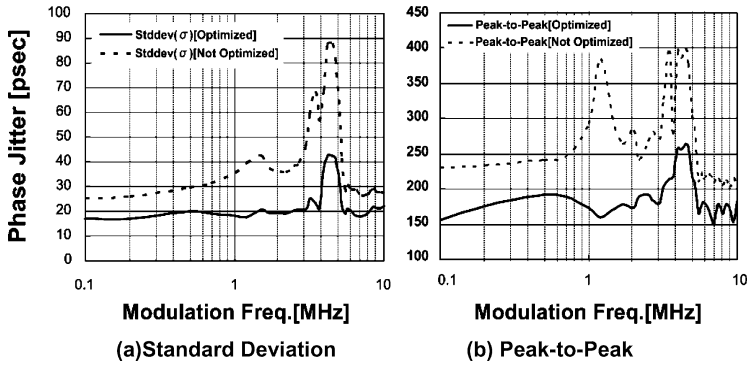

Fig. 16. Jitter performance against the frequency of 10% supply voltage modulation.

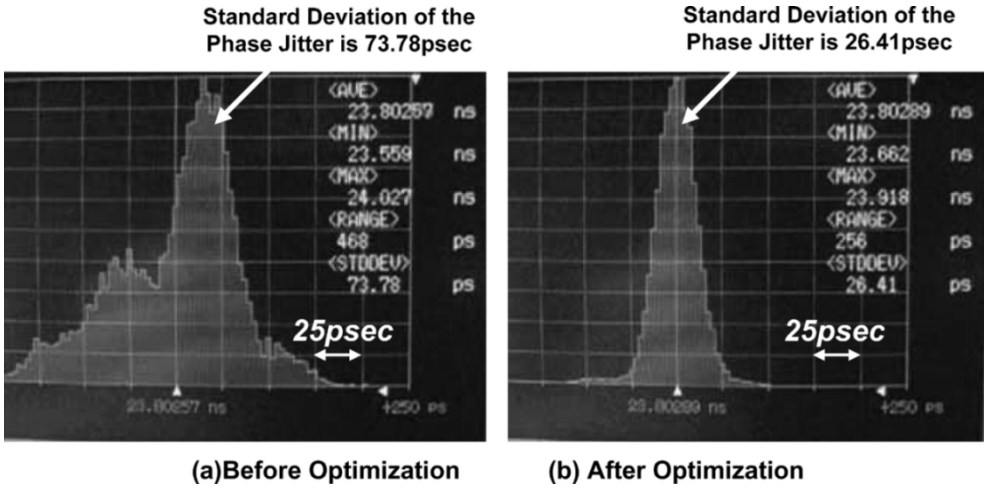

Fig. 17. Comparison of the output jitter spectrum of the TIA (voltage supply noise frequency $=$ 4 MHz).

Fig. 16 shows the jitter performance against the frequency of 10% supply voltage modulation. Fig. 16(a) shows the standard deviation of the phase jitter and Fig. 16(b) shows that of the peak-to-peak, respectively.

As is well known, the sensitivity of the jitter to the frequency modulation shows the bandpass filter (BPF) characteristics. The highest sensitivity point is around a loop bandwidth. In this case, the loop bandwidth is set around 4 MHz. Both of the figures clearly show that the optimization method can control the loop bandwidth so that the jitter performance becomes the best. Even if the optimized jitter performance goes worse around 4 MHz, the performance is much improved as compared with the nonoptimized one.

Fig. 17 shows the comparison of the output jitter spectra of the TIA. In the measurement, the supply voltage noise with modulation frequency of 4 MHz is applied to the PLL. In the spectrum before optimization, we can see the peak division due to the noise. However, the global optimization dissolves the peak division by changing the response parameters.

Next, we evaluate the effect of the local BG optimization. Fig. 18 shows the contour map of the jitter value against the control codes of the I_p and K_o. The circles and arrows in Fig. 18 show the start and end points of the local optimization, respectively. Every vector converged to the area where the jitter is the local minimum.

Fig. 19 shows the transient response of the JDET during the BG optimization. The worst value of the phase change was 0.79% of the input clock. The degradation of the phase jitter due to the change of the control codes is suppressed within a tolerable level.

Fig. 20 shows the performance of the phase jitter against the temperature variation. The figure shows that the local BG optimization keeps the better jitter performance at whole temperature compared with that without the BG optimization.

Fig. 21 also shows the transient response of the control codes during the BG optimization. The start point of the calibration is at 27 °C. At first, the optimum code is shifted to the right as the temperature goes high in order to compensate the decrease of the VCO gain. Next, we cooled the test chip to -40 °C. The optimum code of the VCO gain became small on the contrary at the high temperature. The control code moved around the minimum valley of the search domain. It means that the search domain has the small influence from the temperature variation. However, the sensitivity of the VCO gain to the phase jitter was higher than that of the charge pump current. The result clearly demonstrated the effectiveness of the BG calibration.

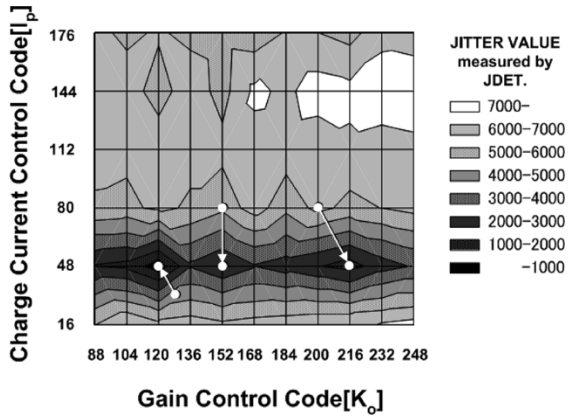

Fig. 18. Search domain of the local optimization.

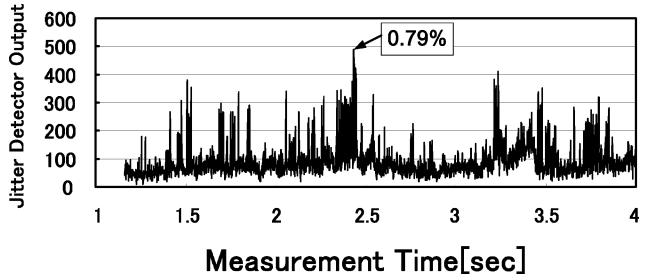

Fig. 19. Output of the jitter detector during BG optimization.

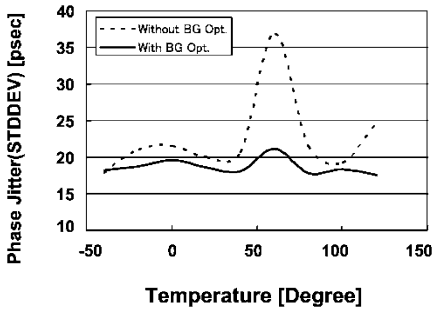

Fig. 20. Comparison of the phase jitter performance against the temperature variation.

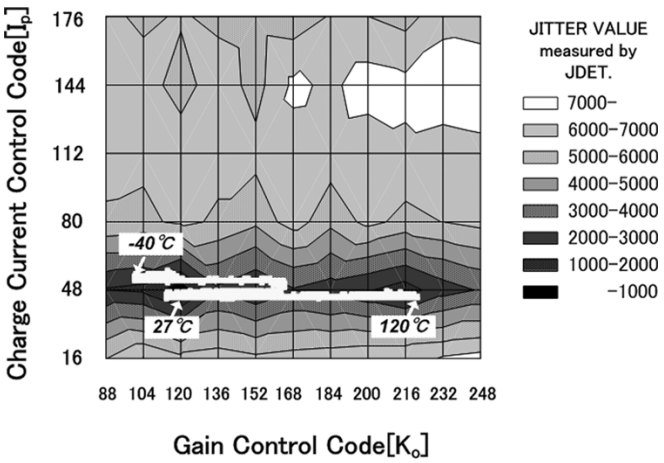

Fig. 21. Transient response of the control codes during the BG optimization.

VII. Conclusion

A new calibration method for the PLL by measuring the phase jitter is described. The test environment fabricated by the 0.15-μm CMOS PLL controlled by an external FPGA demonstrates sufficient ability to suppress the impacts of the environmental variations. This method can achieve the best jitter performance of the PLL under any condition while avoiding the risk caused by accidental noise. The new method is easily applied to any PLL which has a ring oscillator.

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