TOKYO TECH
Pursuing Excellence

Current and future of analog and RF circuits technology

Akira Matsuzawa

Tokyo Institute of Technology

2014/6/25

Matsuzawa & Okada Lab.

Contents

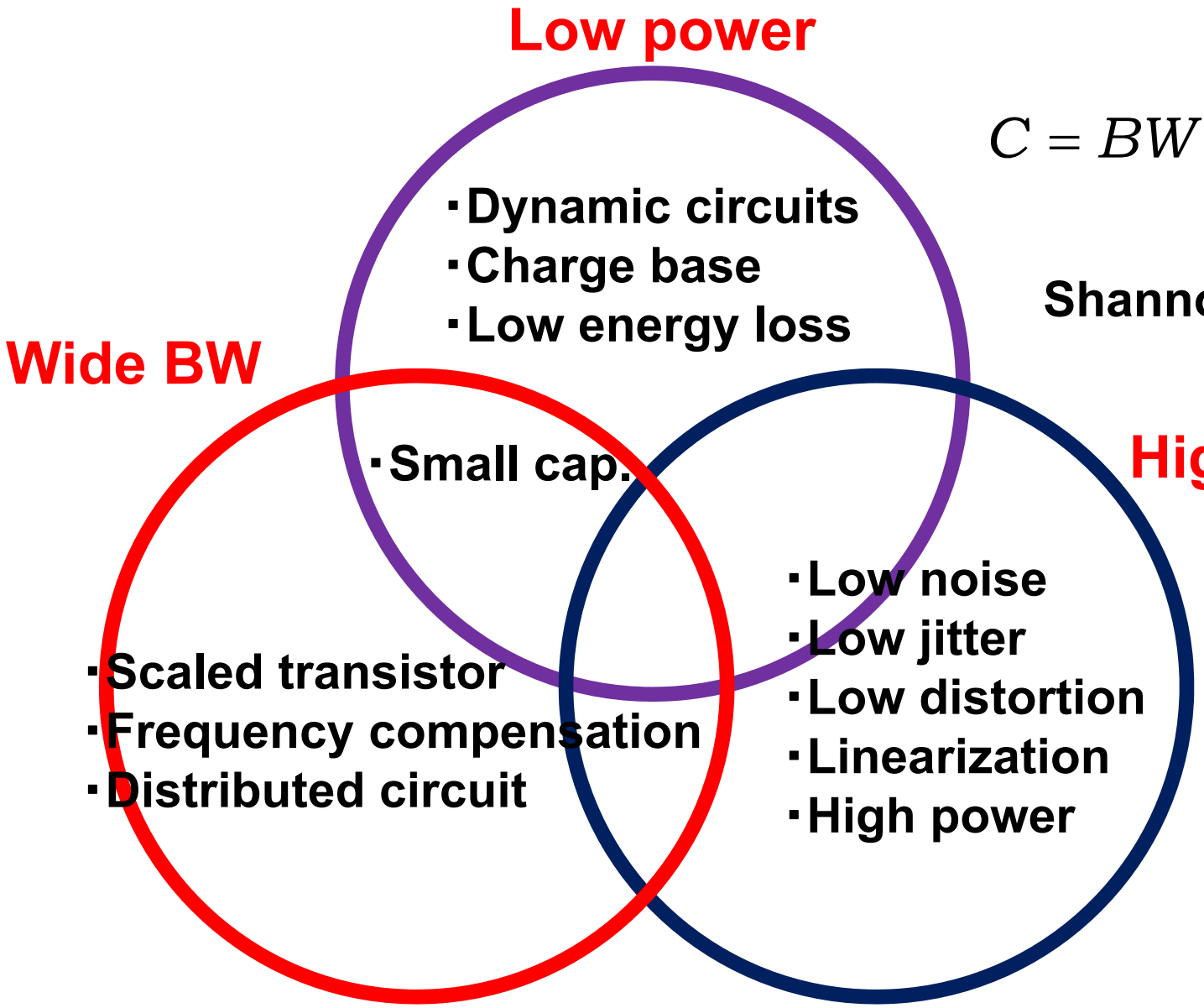
TOKYO TECH Pursuing Excellence

- RF circuits
  - Challenge for ultra-high speed data transfer using millimeter wave technology
    - 60GHz CMOS transceiver attained 28Gbps
    - Toward 300Gbps
- ADC
  - Performance trend
  - Scalable12bit SAR ADC
  - 7bit 2.2GHz ADC using time-domain signal processing
- PLL
- Layout-driven circuit design and programmable analog circuit technique
- Summary

Analog & RF circuits

TOKYO TECH Pursuing Excellence

Data rate∝BW×SNR(dB)



$$C = BW \log_2\left(1 + \frac{P_S}{P_N}\right)$$

Shannon's theorem

ADC and multi-value in data transfer

TOKYO TECH Pursuing Excellence

Wide BW and high SNDR are essentially important for the progress of analog circuits

Communication

$$D_{rate} \approx N \cdot BW$$

N: # of bits
BW: Signal bandwidth

ADC performance

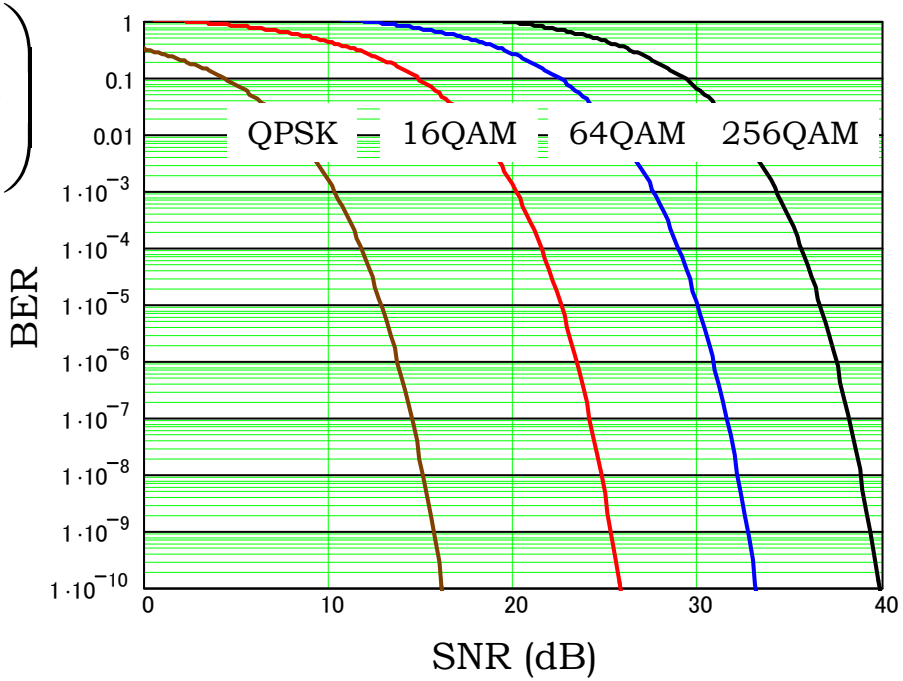
$$D_{rate} \approx N \cdot f_s$$

N: Resolution
f_s: Conversion frequency

Shannon's theorem

$$C = BW \log_2\left(1 + \frac{P_S}{P_N}\right)$$

Higher SNR is required for higher data rate



BW and SNR in ADC

$$BW < \frac{f_s}{2} \qquad \left.\frac{P_S}{P_N}\right|_{ADC} = 1.5 \cdot 2^{2N}$$

$$C \approx N f_s$$

TOKYO TECH
Pursuing Excellence

RF circuits

Challenge for ultra-high speed data transfer using millimeter wave technology

Ultra-high speed data transfer in 60GHz band

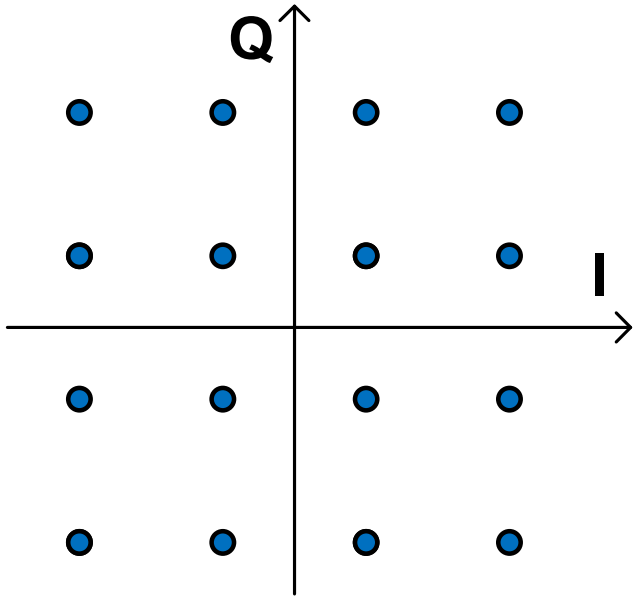
TOKYO TECH Pursuing Excellence

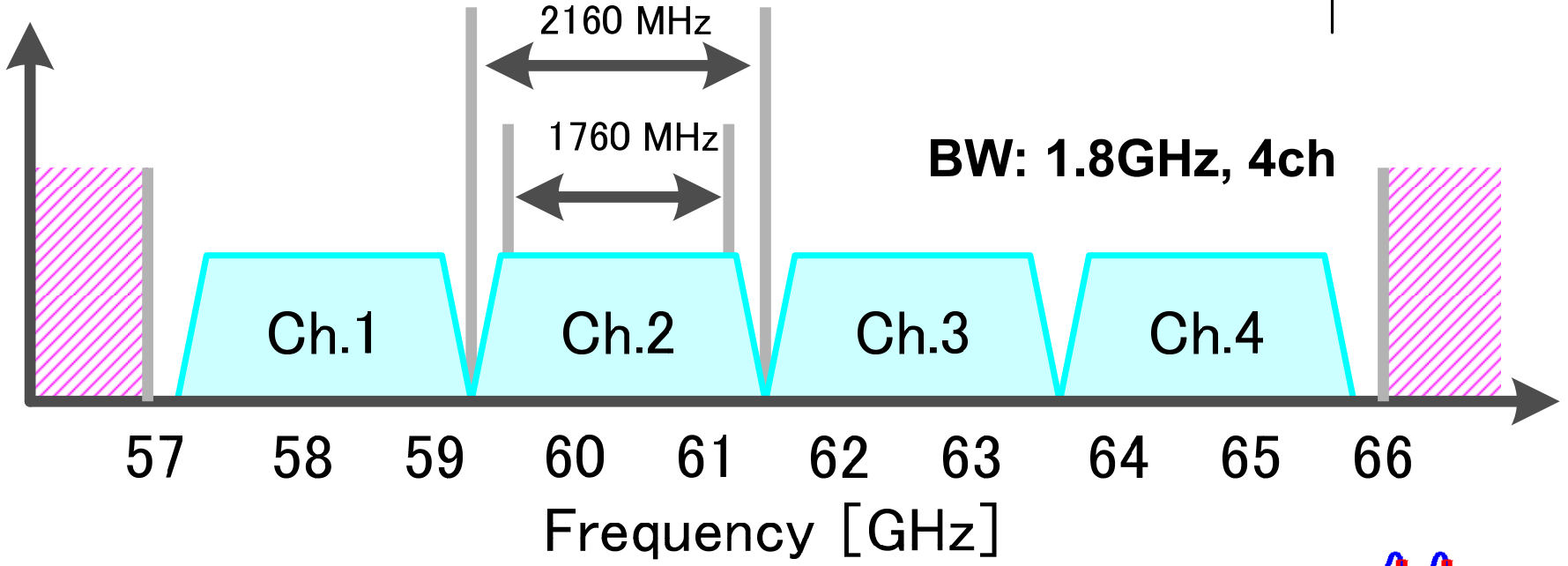
Wider BW and high # of bits are required

BPSK: 1.7 Gbps
QPSK: 3.5 Gbps
16QAM: 7 Gbps
64QAM:10.5Gbps

$$D_{rate} \approx N \cdot BW$$

16QAM





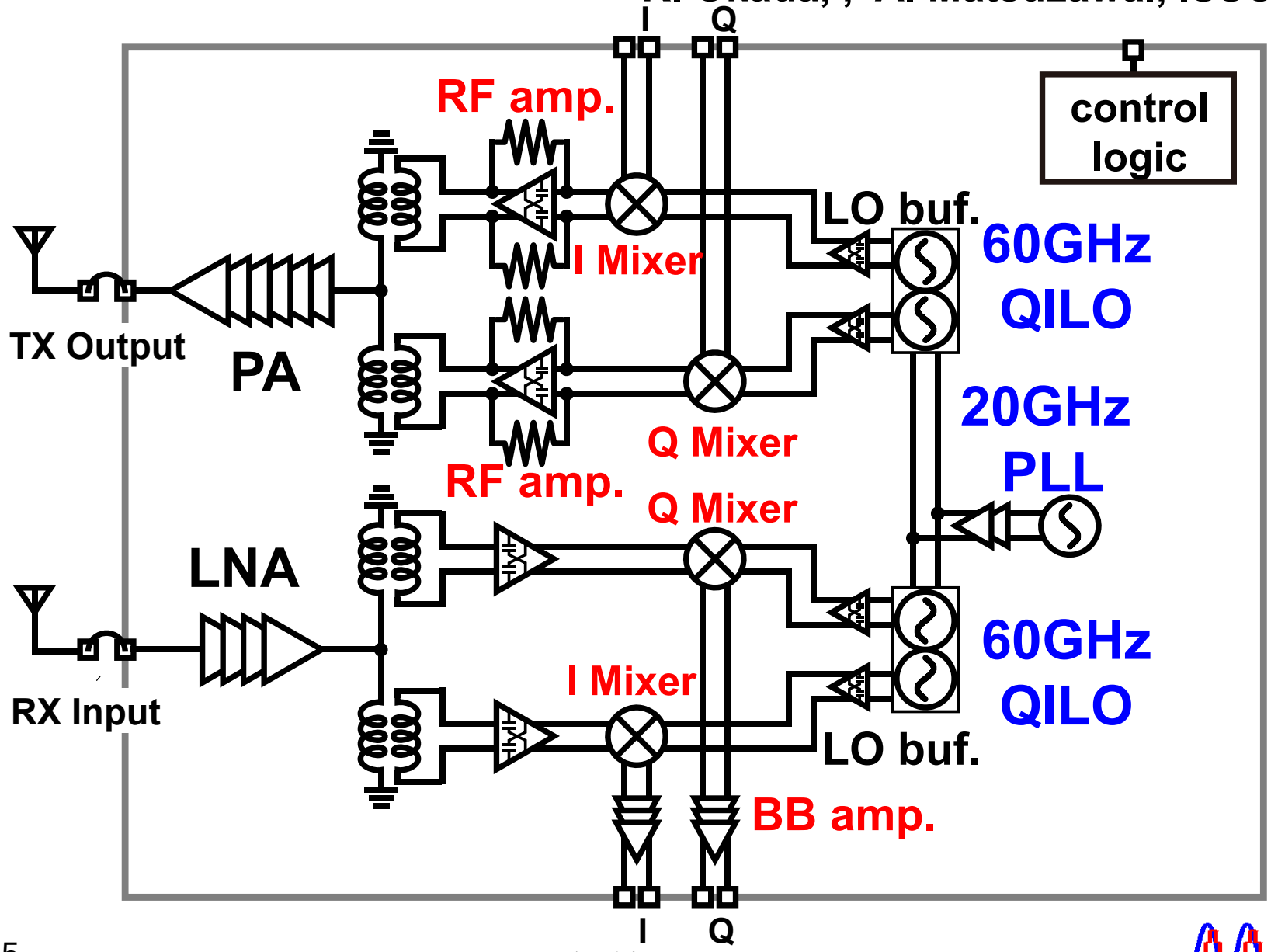
BW: 1.8GHz, 4ch

60GHz CMOS transceiver attained 28Gbps

TOKYO TECH Pursuing Excellence

Direct conversion 60GHz CMOS transceiver

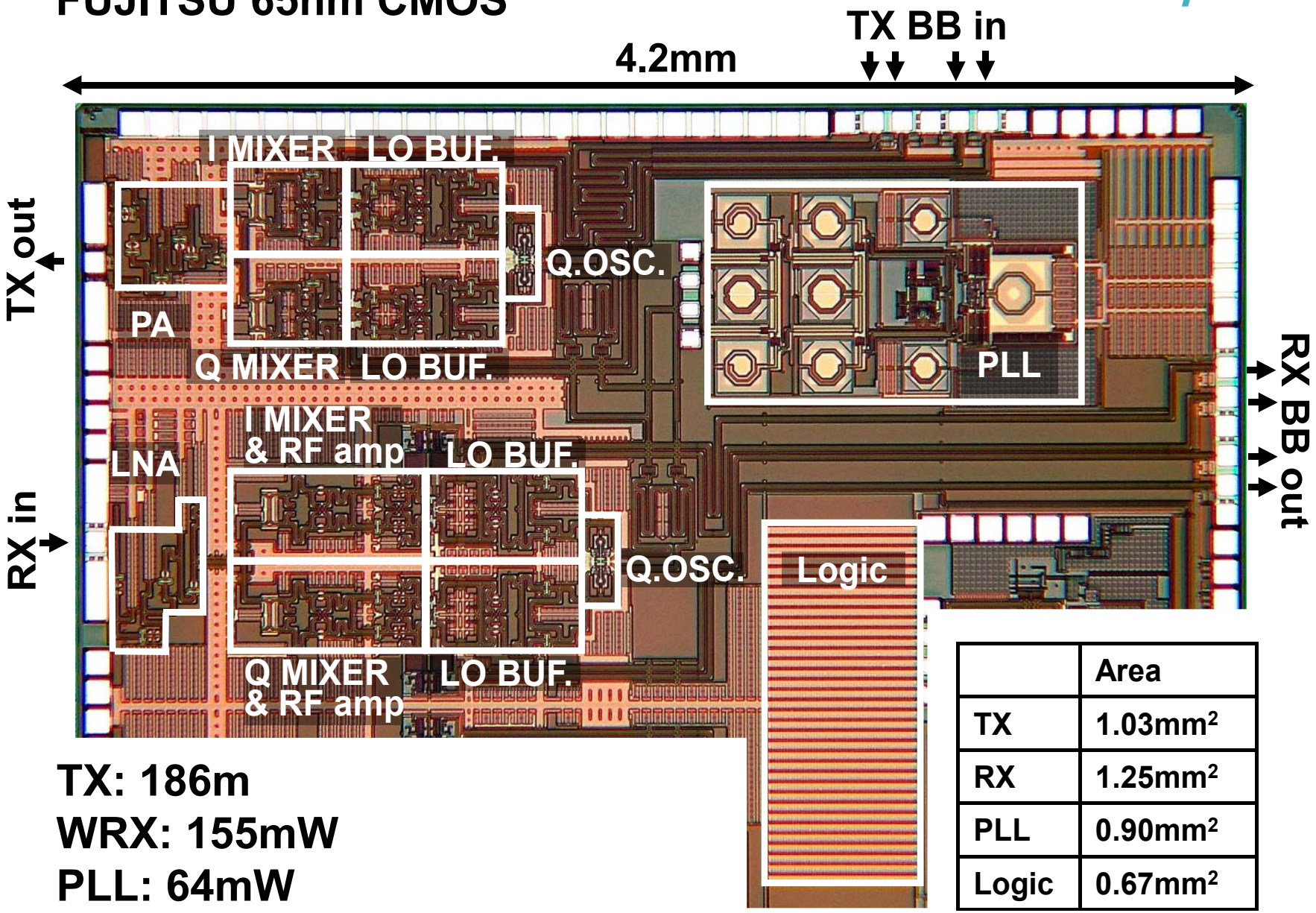
*K. Okada, , A. Matsuzawa., ISSCC 2014



Chip photo

TOKYO TECH Pursuing Excellence

FUJITSU 65nm CMOS



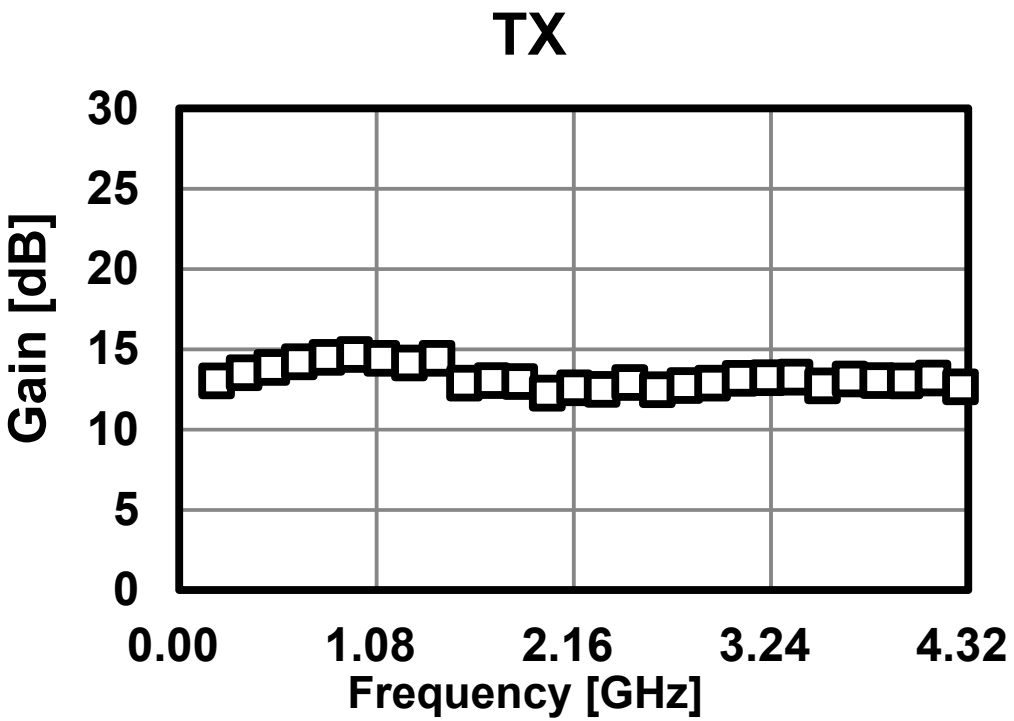
TX: 186m
WRX: 155mW
PLL: 64mW

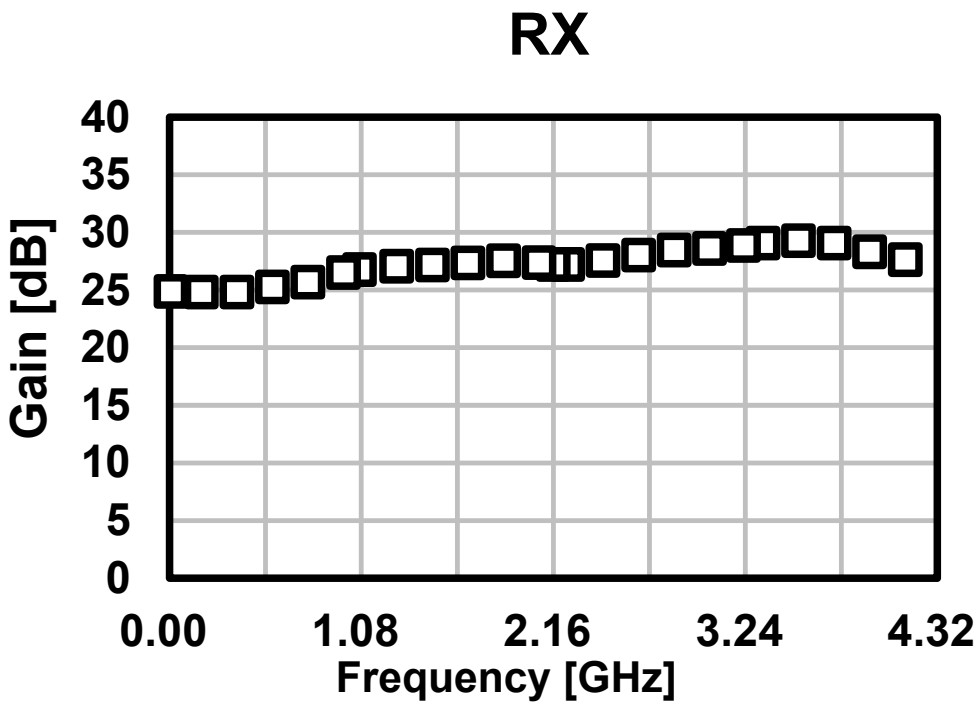
	Area
TX	1.03mm^2
RX	1.25mm^2
PLL	0.90mm^2
Logic	0.67mm^2

Frequency characteristics

TOKYO TECH Pursuing Excellence

Flat frequency characteristics in wide bandwidth (DC～4.32GHz) for the channel bonding

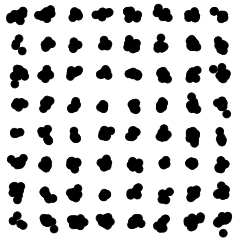
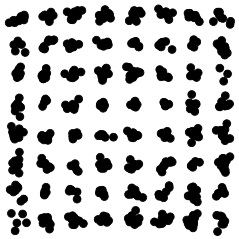
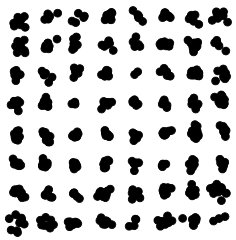
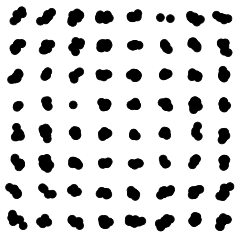
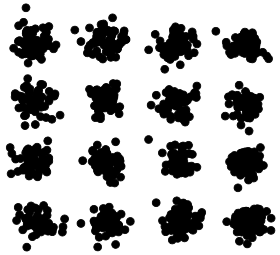
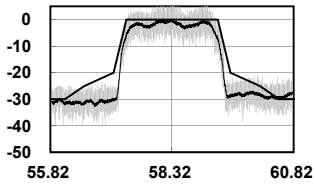
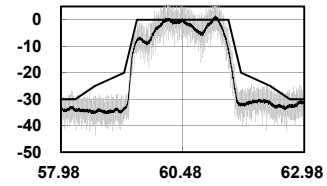
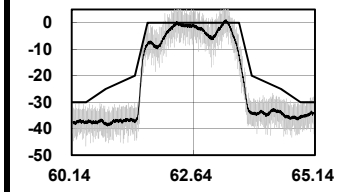
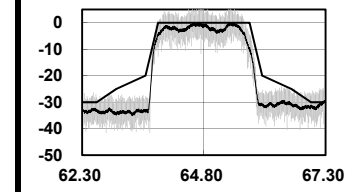
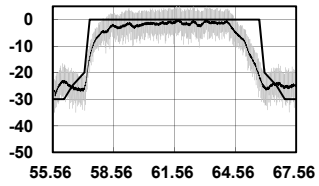




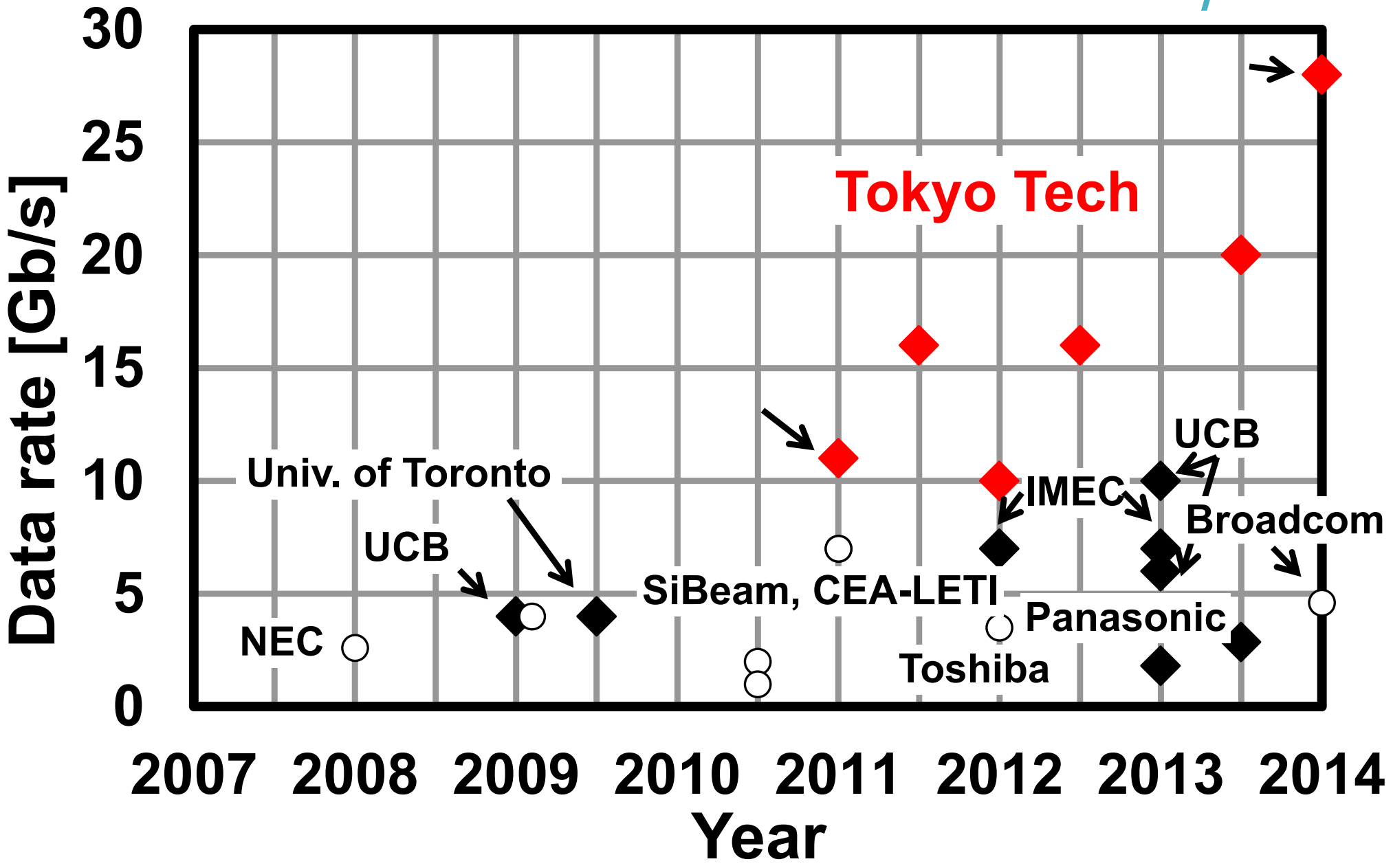
Measured characteristics

TOKYO TECH Pursuing Excellence

World's first 64QAM **World's fastest 28Gbps**

Channel/ Carrier freq.	ch.1 58.32GHz	ch.2 60.48GHz	ch.3 62.64GHz	ch.4 64.80GHz	ch.1-ch.4 Channel bond
Modula-tion	64QAM				16QAM
Data rate*	10.56Gb/s	10.56Gb/s	10.56Gb/s	10.56Gb/s	28.16Gb/s
Constella-tion**					
Spec-trum**					
TX EVM**	-27.1dB	-27.5dB	-28.0dB	-28.8dB	-20.0dB
TX-to-RX EVM***	-24.6dB	-23.9dB	-24.4dB	-26.3dB	-17.2dB

Progress of data rate in 60 GHz band



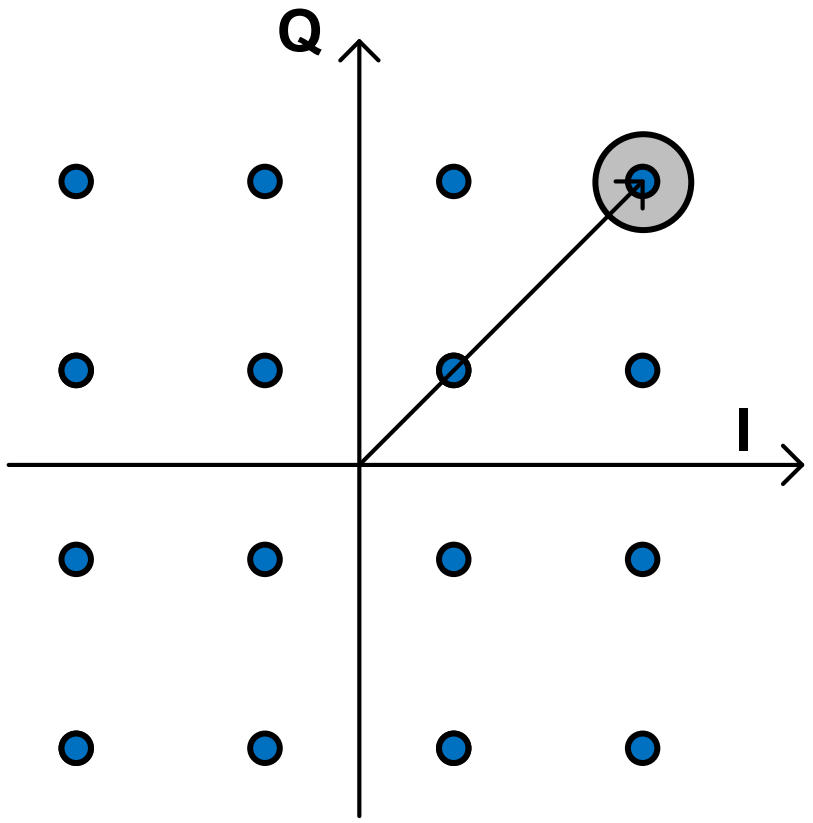
Technology for higher data-rate

TOKYO TECH Pursuing Excellence

$$D = BW \log_2\left(1 + \frac{P_S}{P_N + P_D}\right)$$

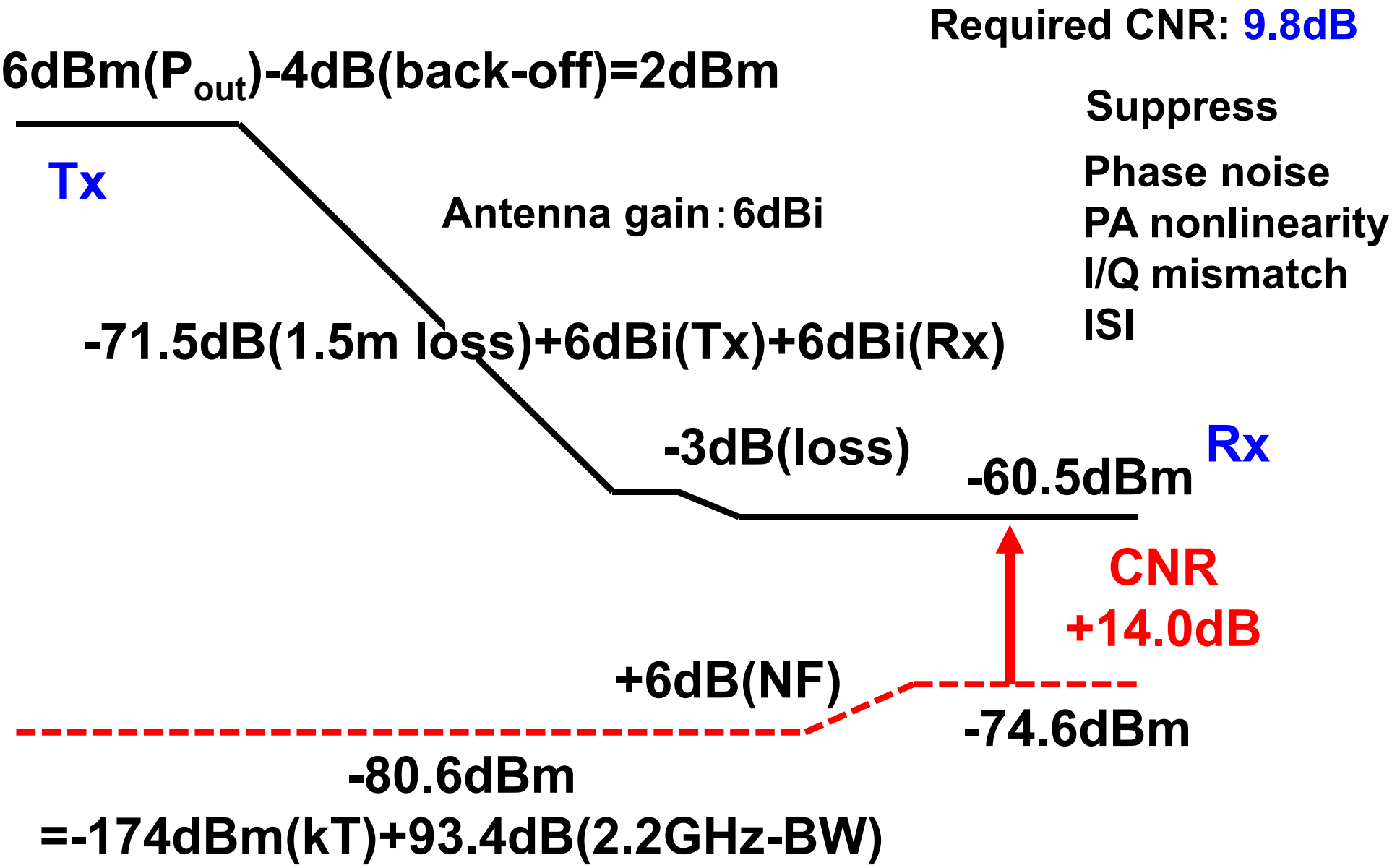
- **Wider BW**
  - **Reduction of parasitic comp.**
  - **Neutralization of parasitic comp.**
  - **Wide-band impedance matching**
- **Higher SNR**
  - **Increase of signal power**
  - **Reduction of power loss**
  - **Decrease of thermal noise**
  - **Decrease of phase noise**
  - **Reduction of distortion**

$$\left(P_s + P_{NT}\right)e^{j(\omega t + \phi_N)}$$



60GHz Link budget (QPSK)

TOKYO TECH Pursuing Excellence



Friis's equation

TOKYO TECH Pursuing Excellence

Higher frequency does not mean higher data rate

Received signal is inversely proportional to square of frequency

RX power　TX power　Antenna gains

$$P_{\mathrm{r}} = \left(\frac{\lambda}{4\pi d}\right)^2 P_{\mathrm{t}} G_{\mathrm{t}} G_{\mathrm{r}} = \left(\frac{c}{4\pi d f_c}\right)^2 P_{\mathrm{t}} G_{\mathrm{t}} G_{\mathrm{r}}$$

Distance　Carrier frequency

（Fixed carrier frequency）

Received power　Noise figure　Distance

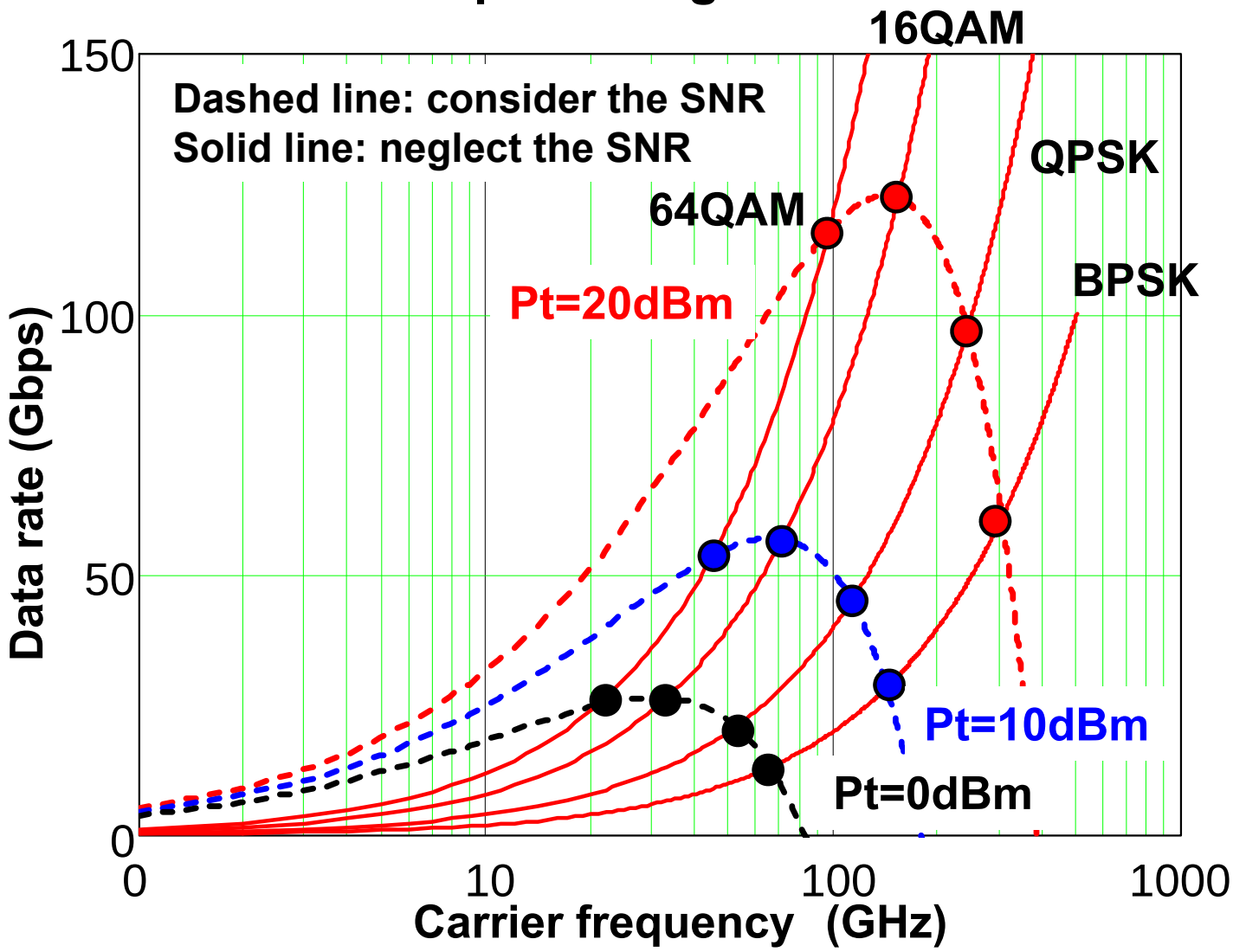
$$P_{\mathrm{eff}} = P_t + G_t + G_r - NF - IL - 20\log_{10}\frac{d}{1\mathrm{m}}\ [\mathrm{dBm}]$$

TX power　Antenna gains　Implementation loss

Estimated data rate

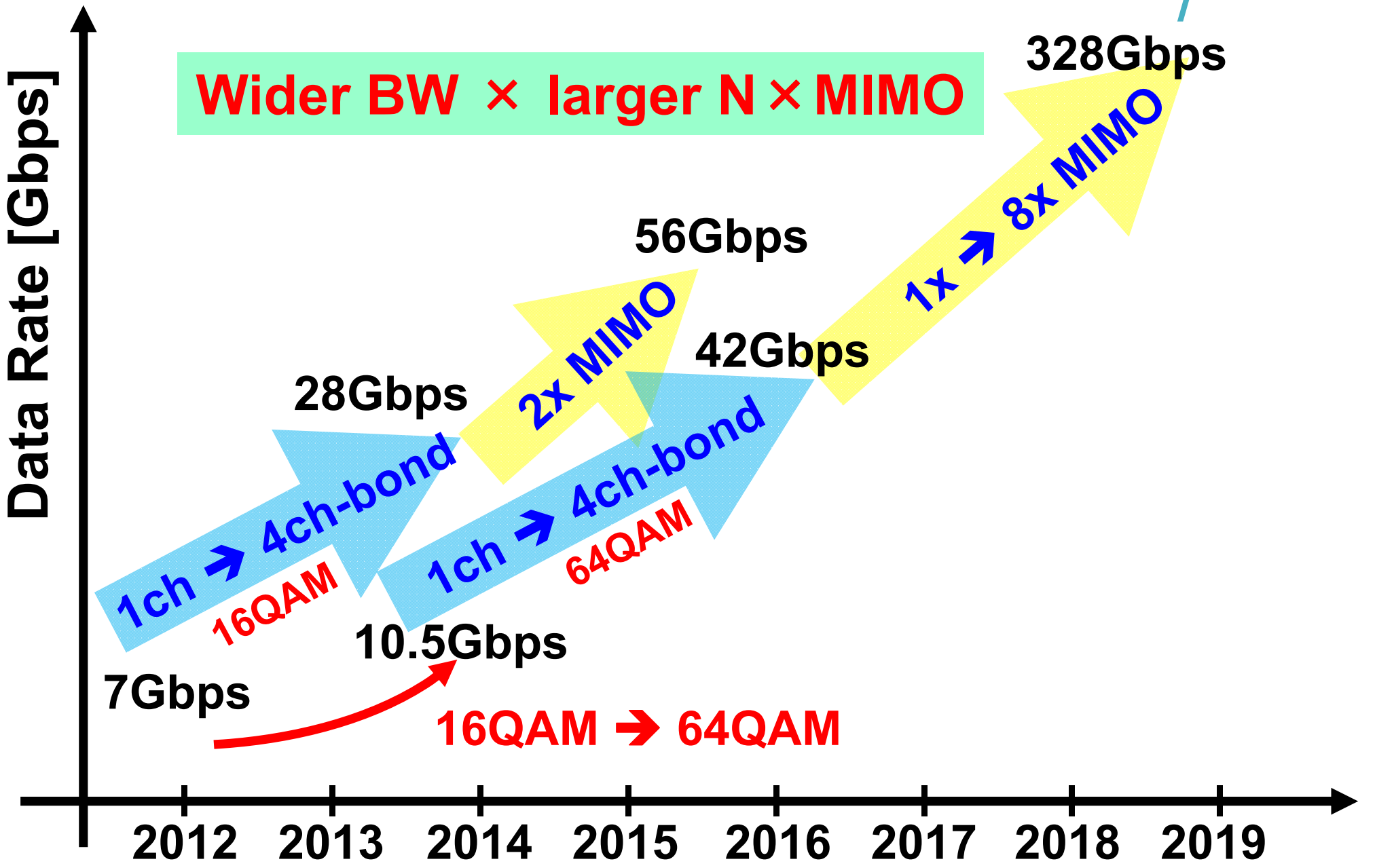
TOKYO TECH Pursuing Excellence

Higher data rate can be expected up to the certain frequency, however it is reduced after that frequency.
Higher power is required for increasing the data rate.
16QAM is the most promising method



Distance：1m
Antenna gain：6dBi
NF: 6dB
Back off： 4dB
Power loss： 3dB

Roadmap for 300Gbps data transfer



TOKYO TECH
Pursuing Excellence

ADC

Requirement for ADC development is still high.
Begin with ADC development and end with it ?

Begin with ADC development and end with it?

TOKYO TECH Pursuing Excellence

I developed the world's first video-rate 10b ADC in 1981.
I have been developing many ADCs during 35 years.
The development of ADC will not end.

Bipolar (3um)
10b, 20MS/s, 2W
$ 800

HDTV broad casting for Seoul Olympic game

T. Takemoto and A. Matsuzawa, JSC, pp.1133-1138, 1982.

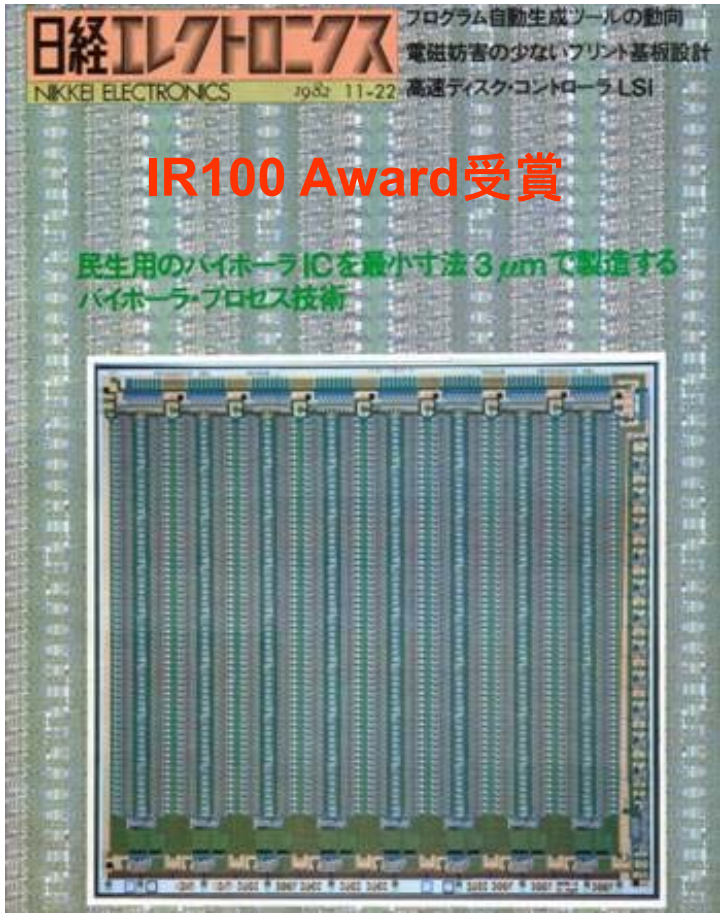
画像処理機器用A／D変換器

松下電器が高性能機

低消費電力で高速

価格 十万円 米TRW社の半値

当初月産五十万個 三月から販売開始



日経エレクトロニクス NIKKEI ELECTRONICS 1982 11-22

プログラム自動生成ツールの動向
電磁妨害の少ないプリント基板設計
高速ディスク・コントローラLSI

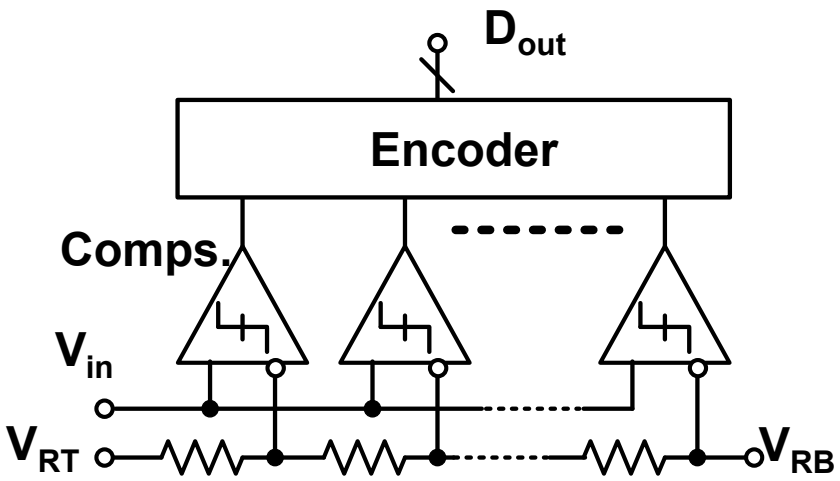
IR100 Award受賞

民生用のバイポーラICを最小寸法3μmで製造する
バイポーラ・プロセス技術

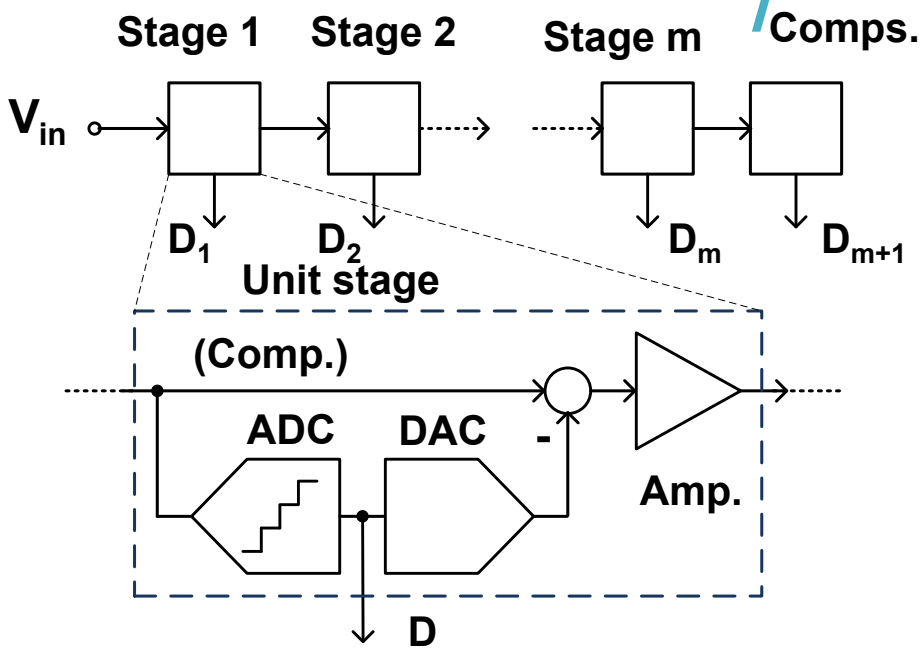
TOKYO TECH
Pursuing Excellence

Progress of ADCs

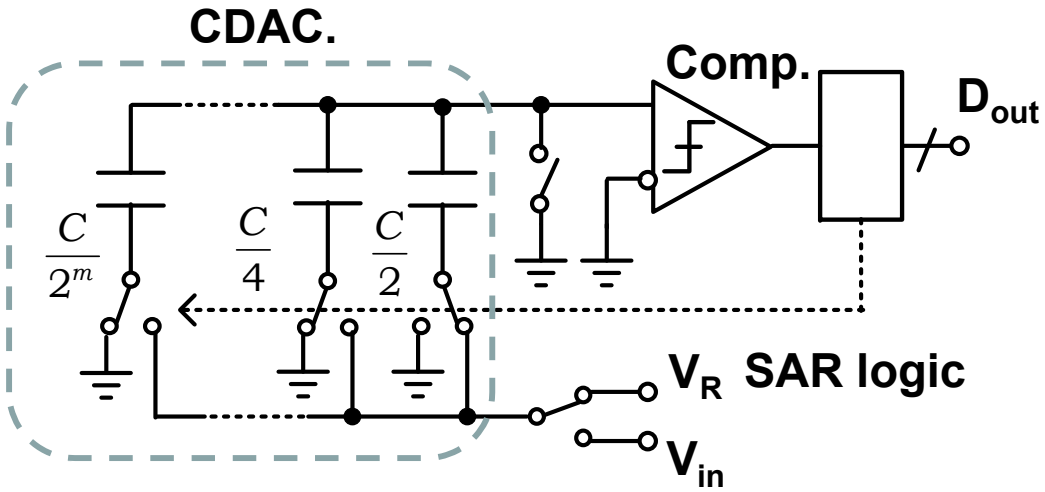
ADC architecture



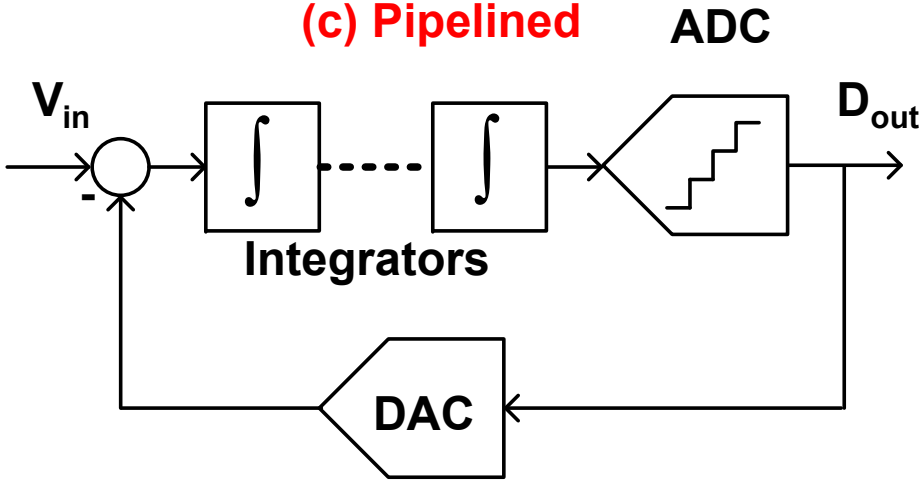
(a) Flash



(c) Pipelined



(b) SAR

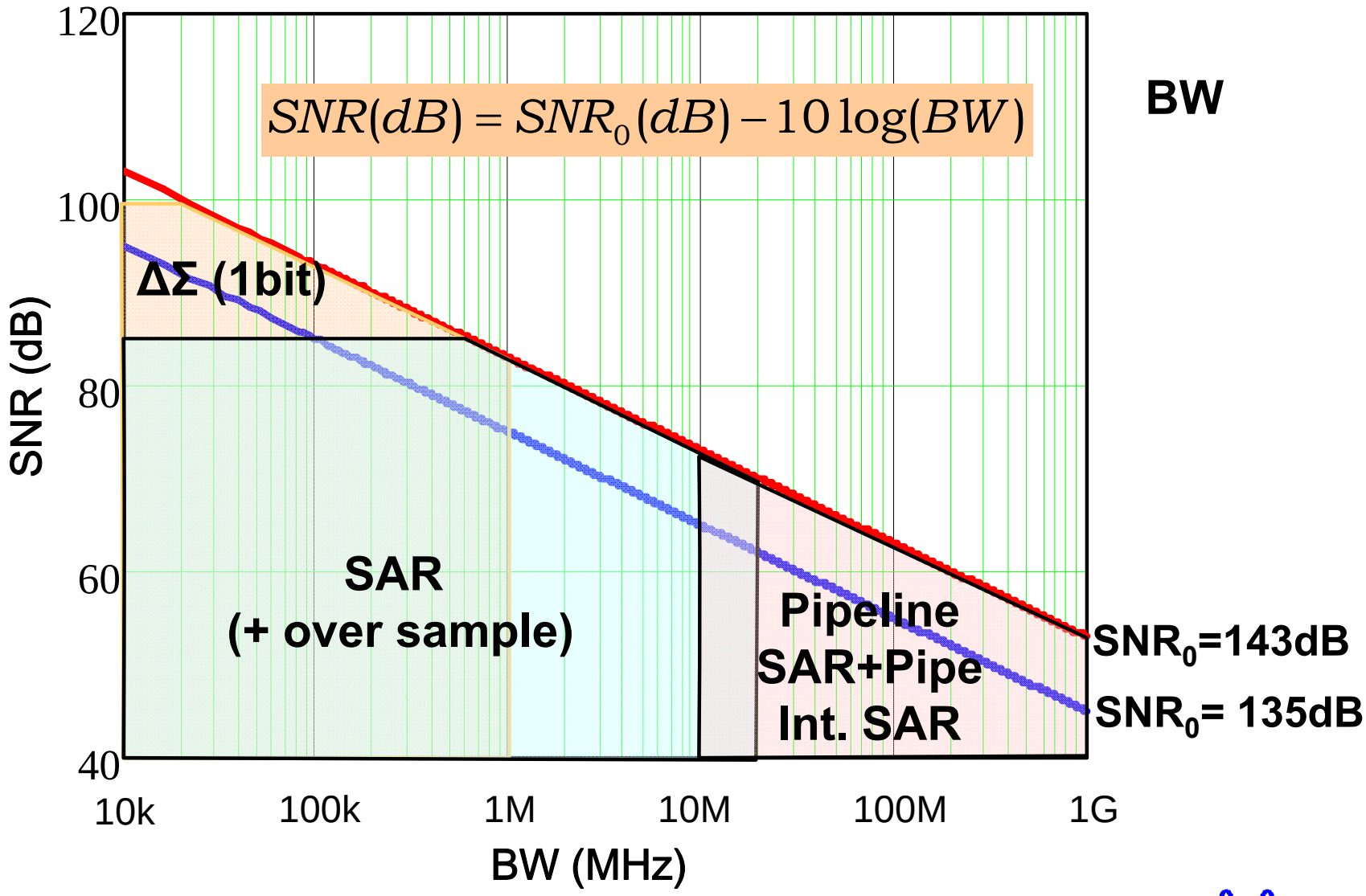


(d) Sigma-Delta

BW, SNR and ADC architectures

TOKYO TECH Pursuing Excellence

SAR ADC is major. DS ADC is for higher SNR than 80 dB.
Pipelined ADC is for wider BW than 40MHz.

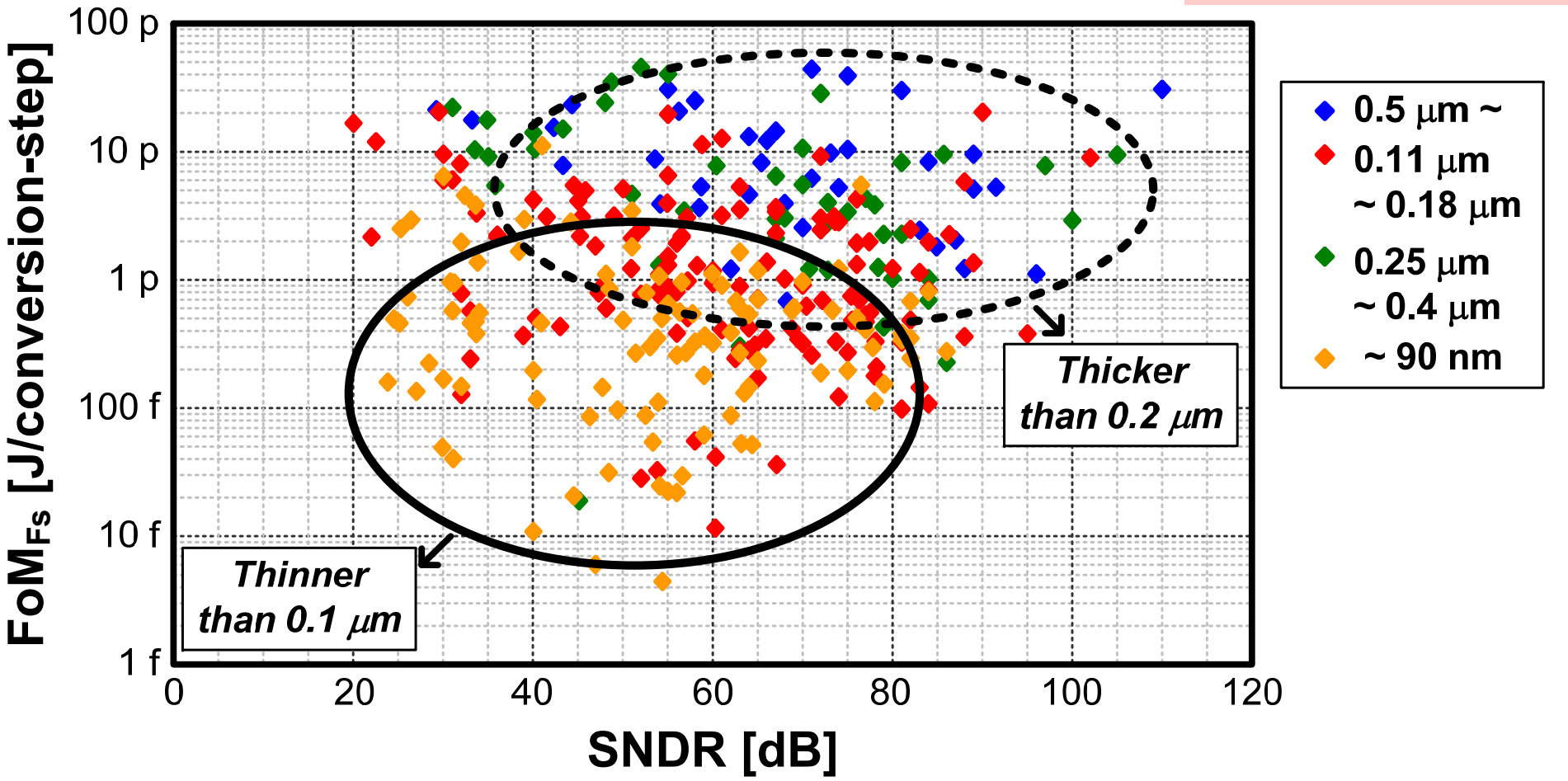


Technology scaling and ADC performance

TOKYO TECH Pursuing Excellence

Technology scaling is effective to lower the FOM for low SNR ADC, however not effective to higher SNR ADC.

$$FoM = \frac{P_d}{f_s \times 2^{ENOB}}$$



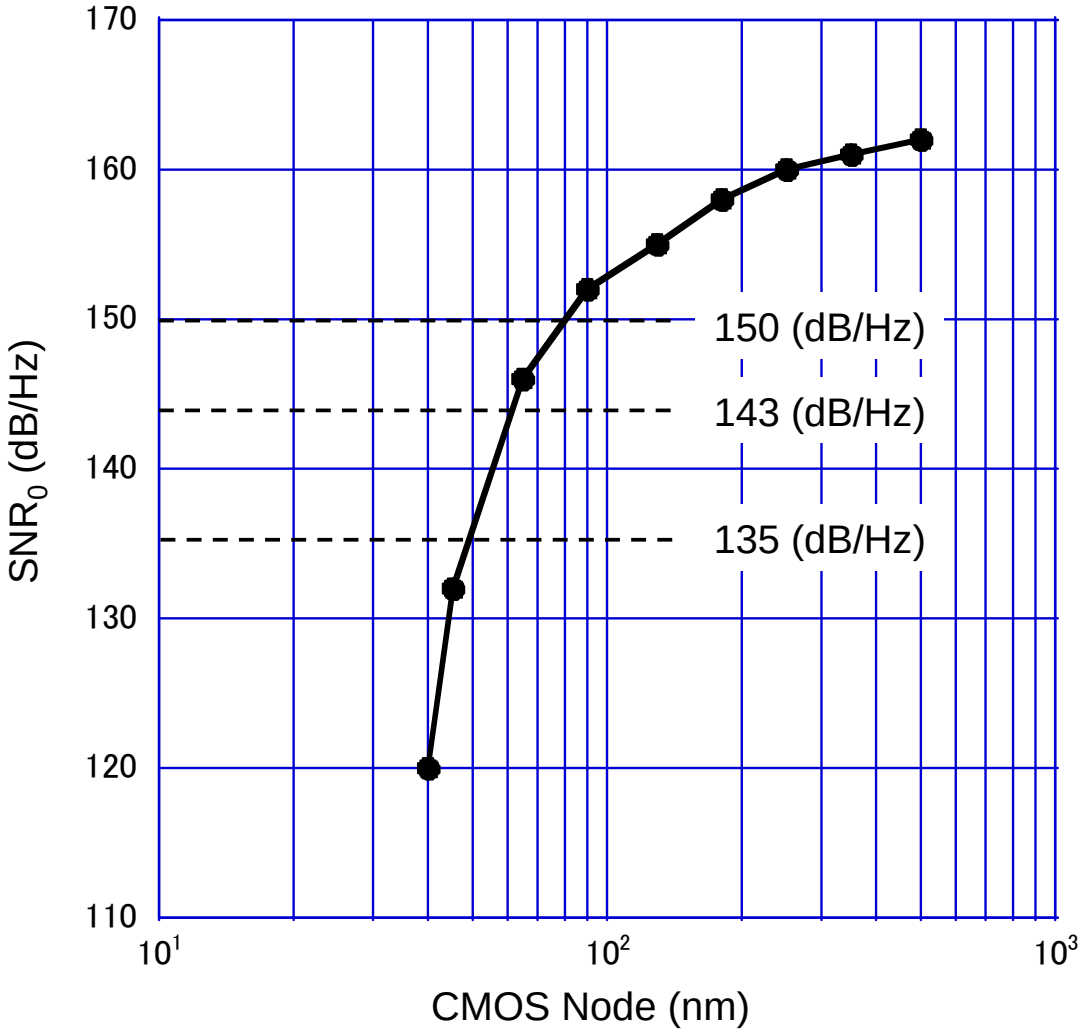
B. Murmann, "ADC Performance Survey 1997-2011," [Online].

Technology scaling and SNR in ADC

TOKYO TECH Pursuing Excellence

Longer technology node is needed for higher SNR

$$SNR(dB) = SNR_0(dB) - 10\log(BW)$$



Jonsson, B., ICECS 2010.

Fundamental Energy of sampling circuit

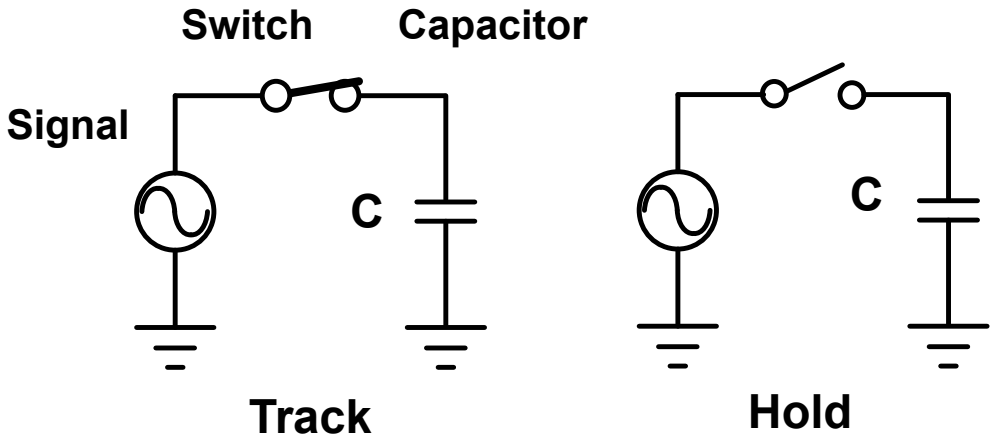
TOKYO TECH Pursuing Excellence

Fundamental energy of sampling is often used.

However this neglects the power for comparison.

$$E_{ADC} \approx N \times E_s = 24\mathrm{k}T \cdot N \cdot 2^{2N}$$

Sampling circuit



Quantization voltage

$$V_q = \frac{V_{FS}}{2^N}$$

Quantization noise power

$$\overline{V_q^2} = \frac{V_q^2}{12} = \frac{V_{FS}^2}{12 \cdot 2^{2N}}$$

Noise balance $\overline{V_n^2} = \overline{V_q^2}$

Electrical energy=Thermal energy

$$\frac{1}{2}CV_n^2 = \frac{1}{2}\mathrm{k}T \quad \therefore \quad V_n^2 = \frac{\mathrm{k}T}{C}$$

Capacitance $C = 12\mathrm{k}T\dfrac{2^{2N}}{V_{FS}^2}$

P_d of sampling circuit

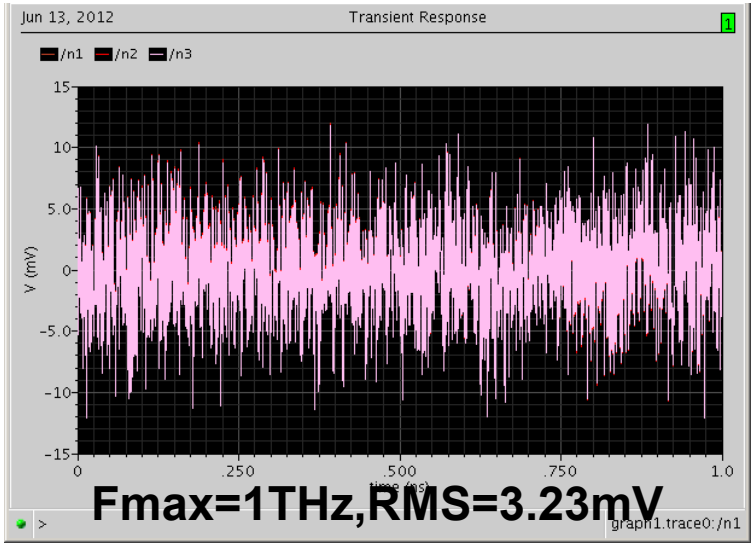
$$E_S = 2CV_{FS}^2 = 24\mathrm{k}T2^{2N}$$

Transient noise simulation

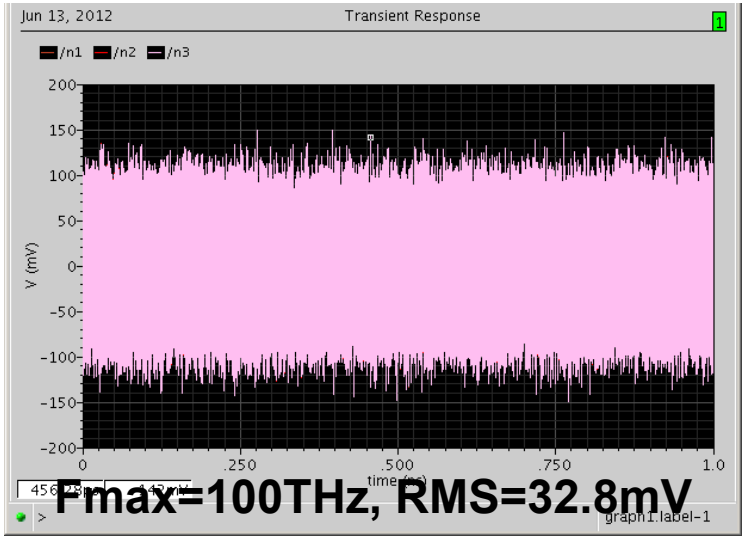
TOKYO TECH Pursuing Excellence

Input noise is increased with frequency bandwidth, if C_p is very small.
If C_p exists, it determines noise voltage.

C_p=0

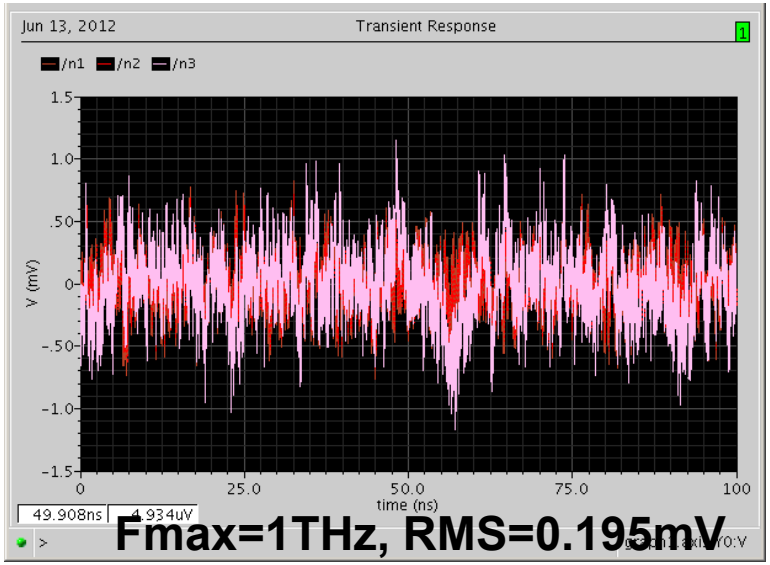


Fmax=1THz,RMS=3.23mV

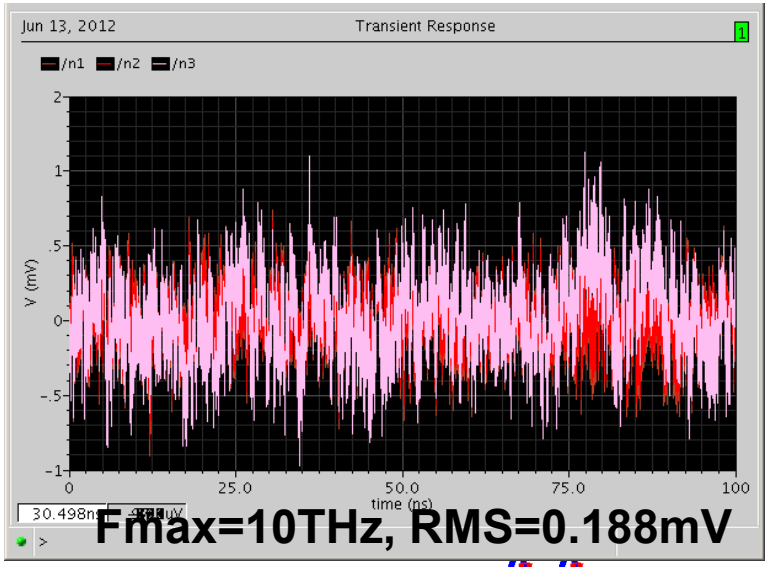


Fmax=100THz, RMS=32.8mV

C_p=100fF



Fmax=1THz, RMS=0.195mV

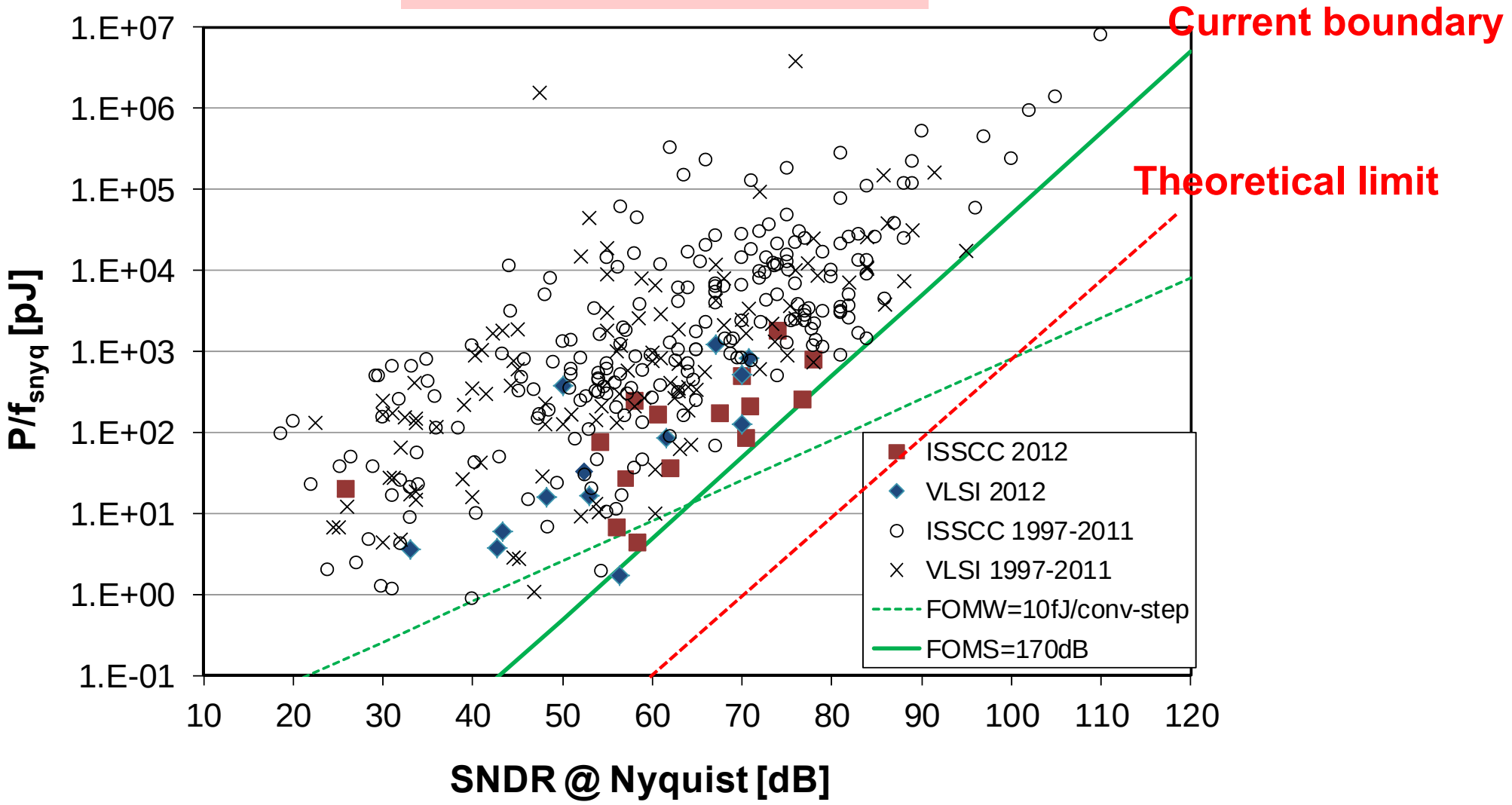


Fmax=10THz, RMS=0.188mV

P_d/f_s and SNDR

P/f_s is proportional to SNDR theoretically

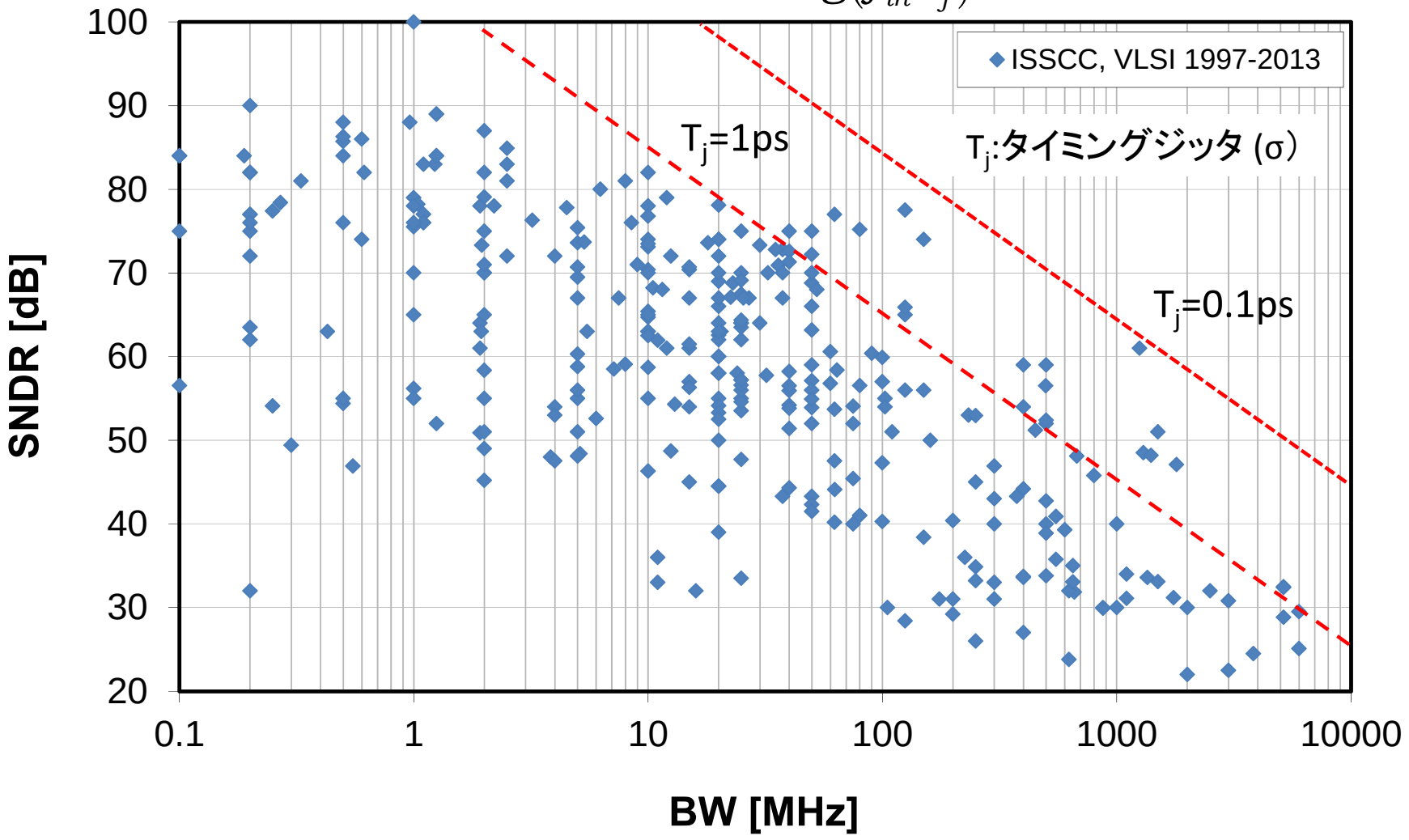
Theoretical limit $E_{ADC} = N \times 2^{2N} \times 10^{-19}$



BW and SNDR

SNDR is reduced with increasing BW.
Required timing jitter is less than 0.1 ps order.

$$SNDR \propto -20\log\left(f_{in}T_j\right)$$



TOKYO TECH
Pursuing Excellence

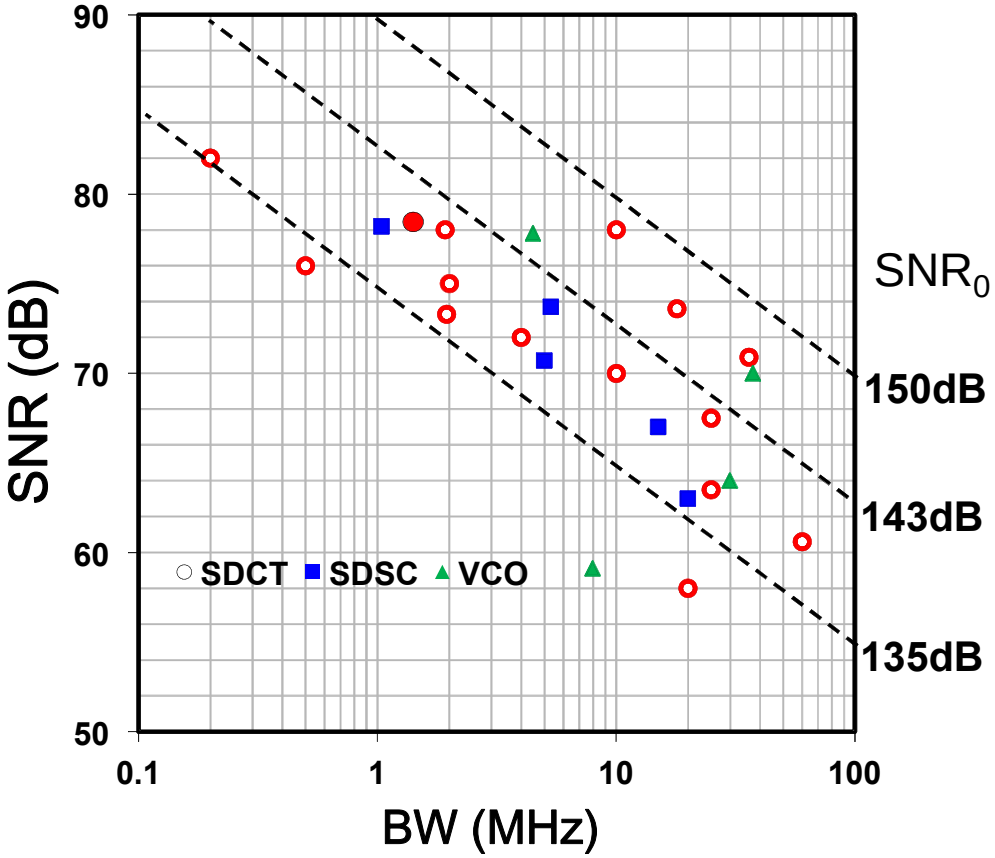
Scalable 12bit SAR ADC

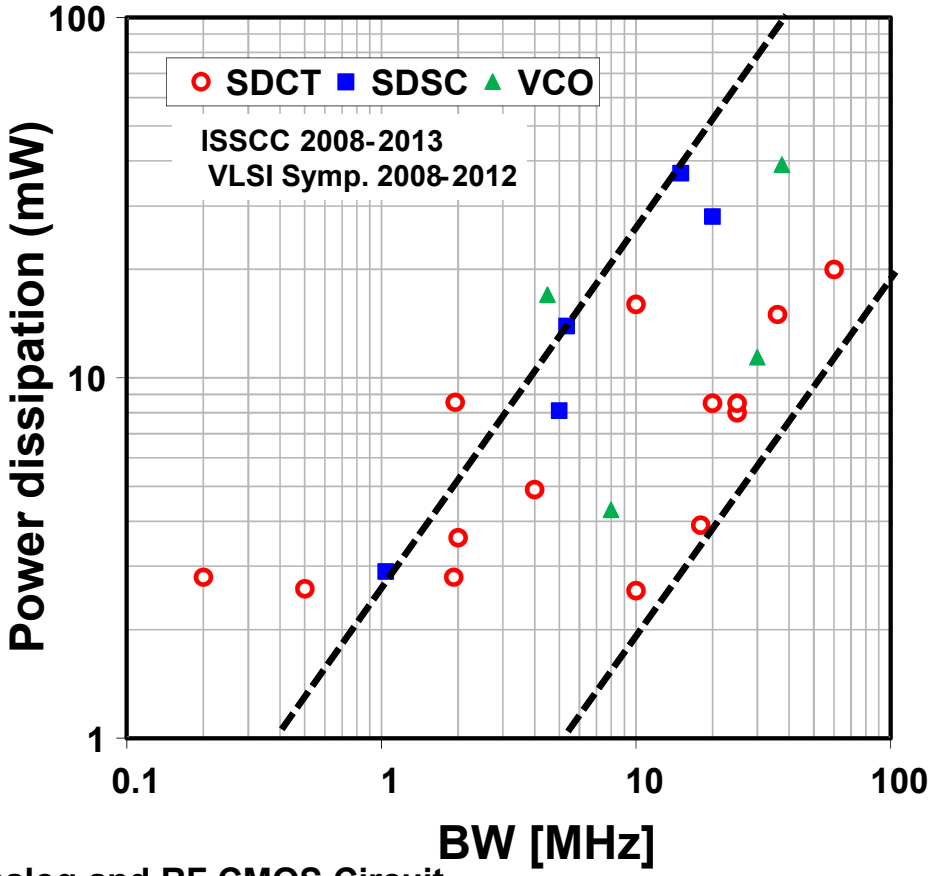
Scalable ADC

SNR can be increased by the reduction of BW, up to 84 dB.
SNR_0 should be higher than 143 dB.
P_d should be minimized and can be reduced by the reduction of BW.

$$SNR \approx SNR_0 - 10\log(BW) \qquad P_d \approx K_1 \cdot BW$$

K_1: 0.2 -- 3 (mW/MHz)





Matsuzawa, A. "Digitally-Assisted Analog and RF CMOS Circuit Design for Software-Defined Radio," Chapter 7, Springer 2011.

Basic idea for low energy and scalable analog

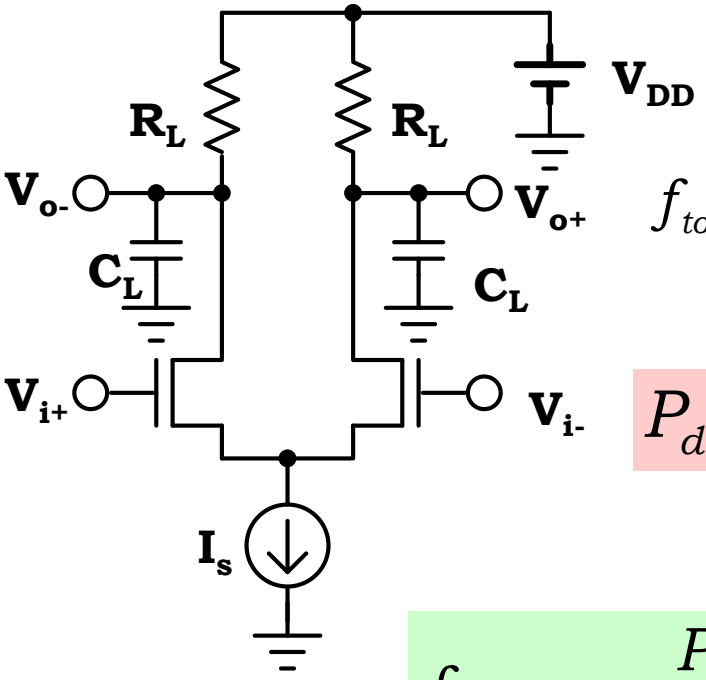
TOKYO TECH Pursuing Excellence

Conventional analog circuit consumes continuous current and results in larger energy consumption. **Not scalable P_d for operating frequency.**

Dynamic circuits doesn't consume larger energy.

CMOS: Consumed energy is independent of the delay time.
Scalable power consumption for the operating frequency.

CML, OpAmp

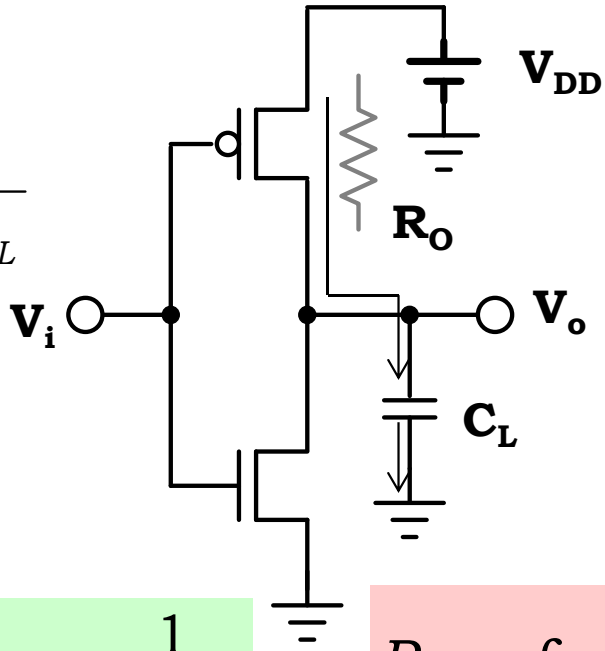


$$f_{togle} \propto \frac{I_s}{V_{DD} C_L}$$

$$P_d = V_{DD} I_s$$

$$f_{togle} \propto \frac{P_d}{C_L V_{DD}^2}$$

CMOS



$$f_{togle} \propto \frac{1}{T_r} \propto \frac{1}{R_o C_L}$$

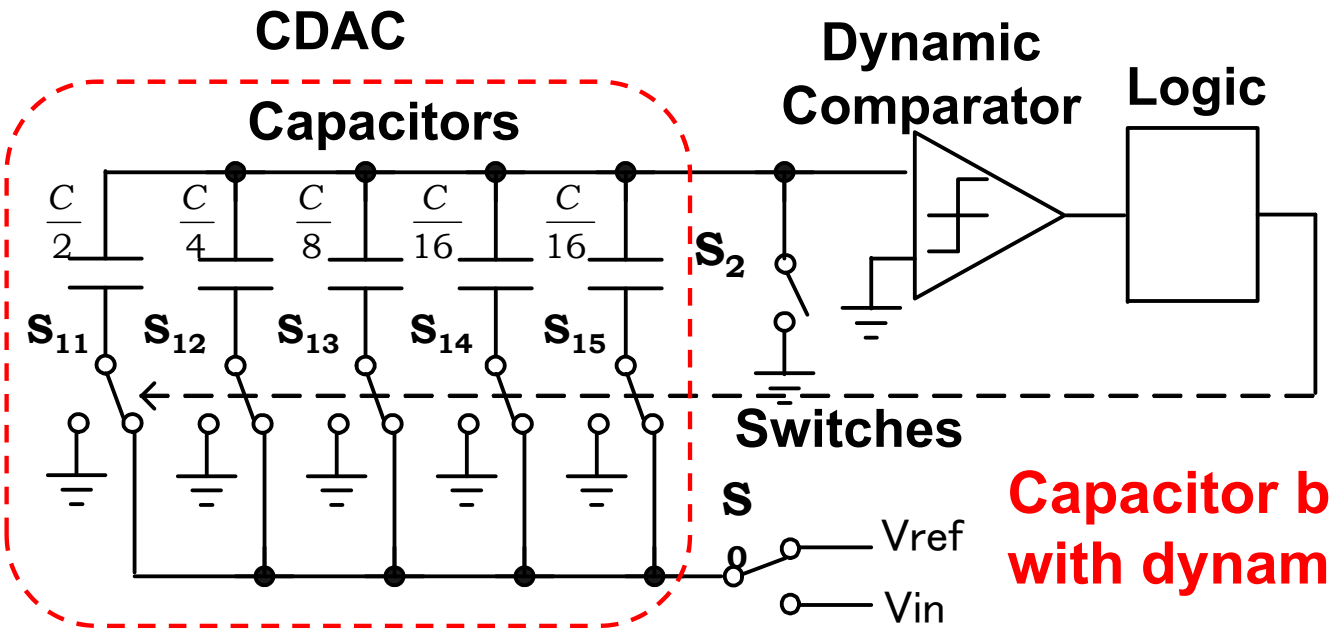
$$E_d = \frac{1}{2} C_L V_{DD}^2$$

$$f_{togle} \propto \frac{1}{R_o C_L}$$

$$P_d = f_{clk} E_d = \frac{1}{2} f_{clk} C_L V_{DD}^2$$

SAR ADC

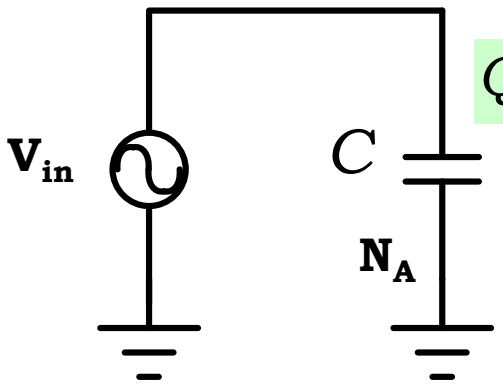
SAR ADC doesn't consume any static power and has no tradeoff between the speed and the energy consumption.



- No resistors
- No amplifier
- No static current !
- Potentially full swing

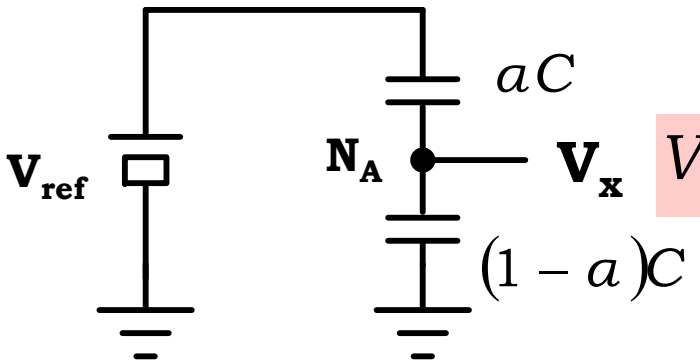
Capacitor based analog processing with dynamic comparator

Sample



$$Q = -CV_{in}$$

Generating subtracted signal



$$E_d \approx \frac{1}{2}CV_{ref}^2$$

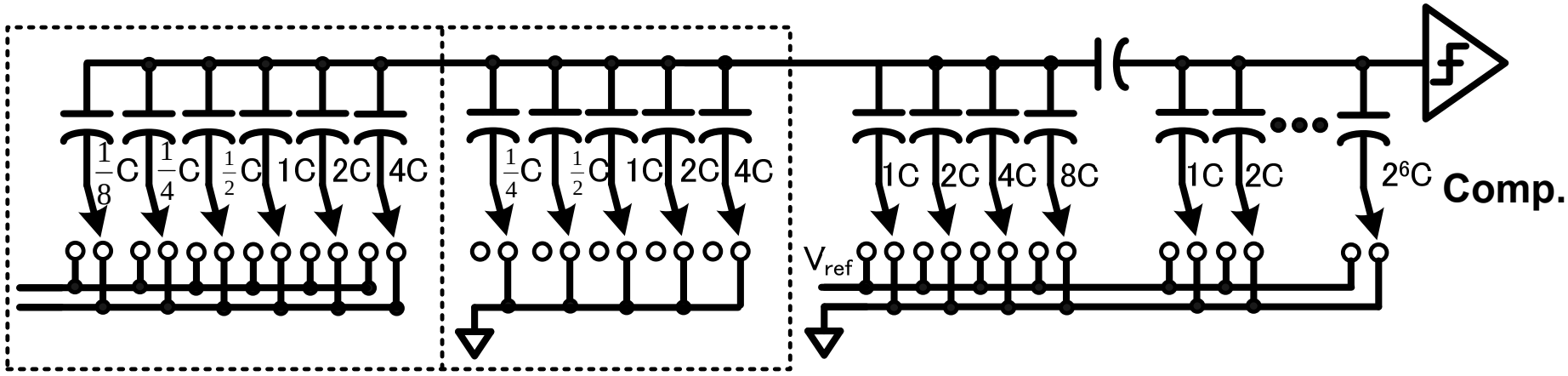
$$V_x = -\left(V_{sig} - a \cdot V_{ref}\right)$$

$$0 < a < 1$$

SAR ADC：Versatile ADC

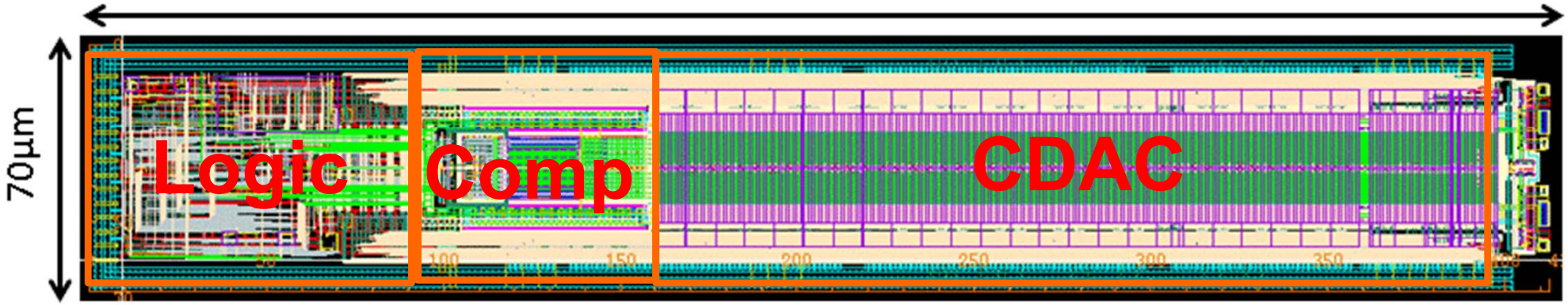
TOKYO TECH Pursuing Excellence

SAR ADC is the most energy efficient ADC.
It can be used for versatile applications.



Mismatch CAL. **Parasitic CAL.** **12bit, 65nmCMOS, 0.03mm²**

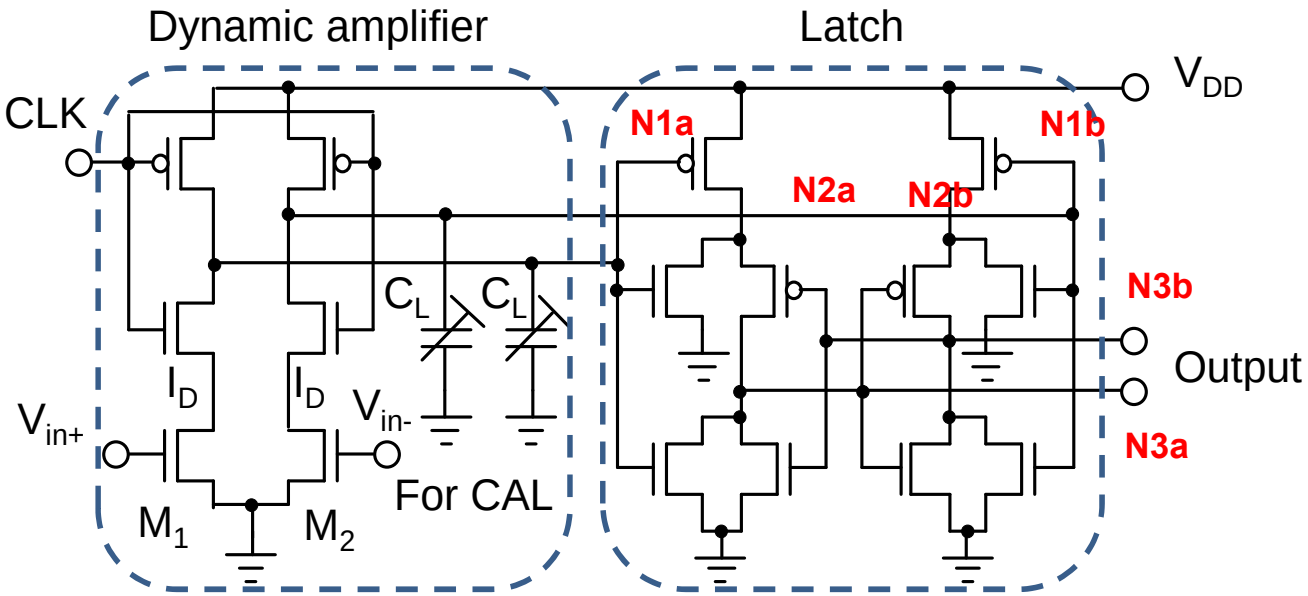
S. Lee, A. Matsuzawa, SSDM 2013

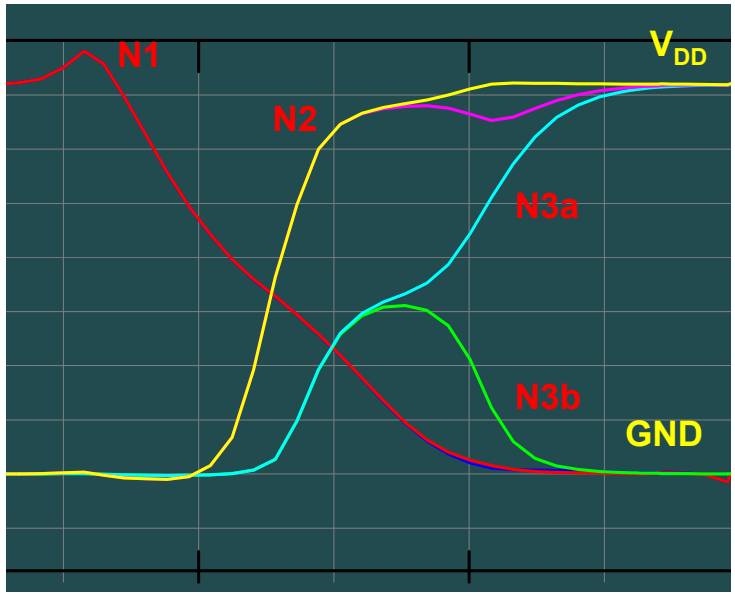


Dynamic comparator

TOKYO TECH Pursuing Excellence

Dynamic comparator doesn't consume any static power. Large noise was an issue, however improved by our proposed Circuit using CMOS inter-stage amplifier.





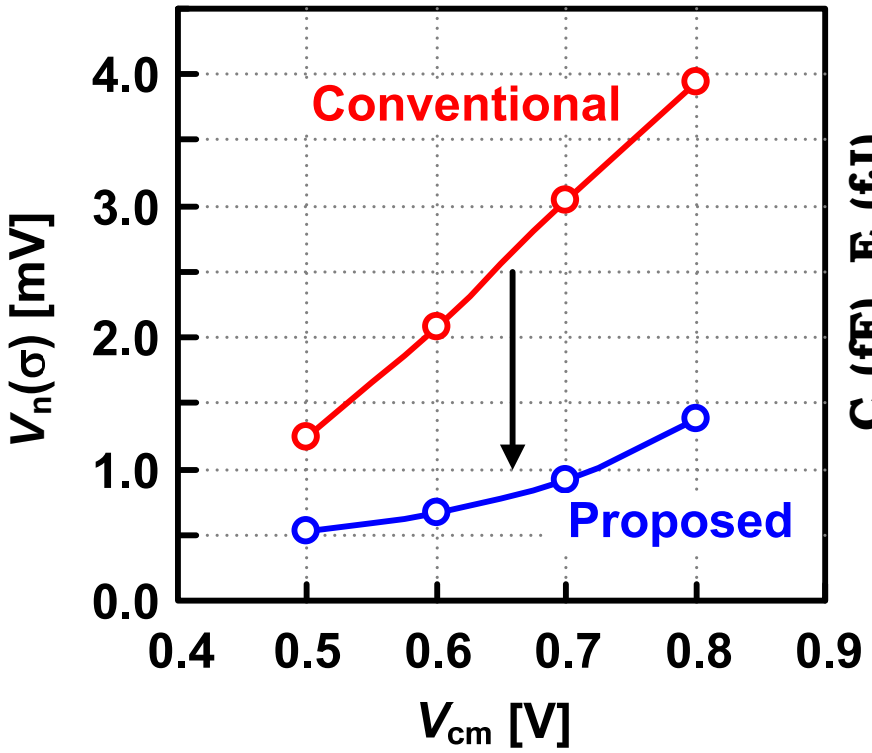
M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

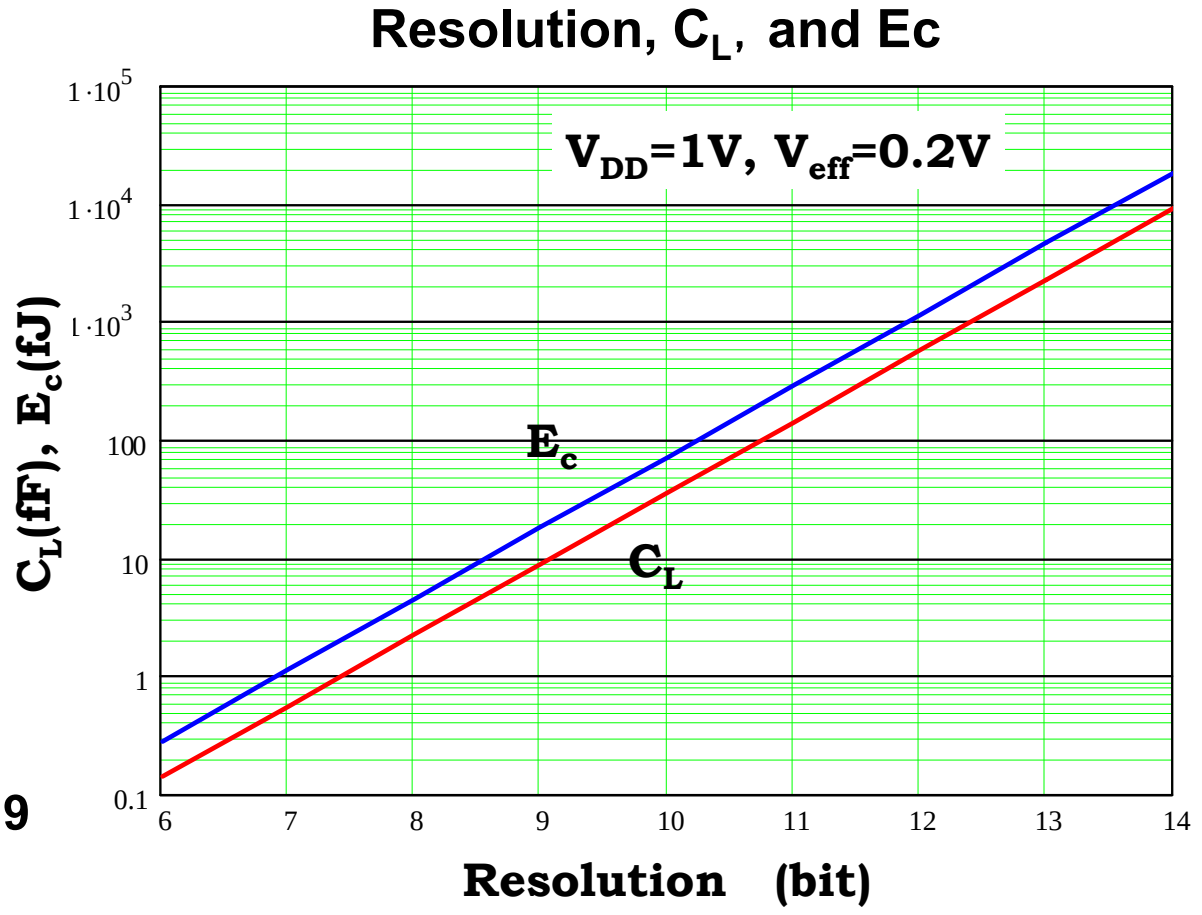
Yusuke Asada, Kei Yoshihara, Tatsuya Urano, Masaya Miyahara, and Akira Matsuzawa, "A 6bit, 7mW, 250fJ, 700MS/s Subranging ADC," A-SSCC, 5-3, pp. 141-144, Taiwan, Taipei, Nov. 2009.

Noise in dynamic comparator

Noise in dynamic comparator can be improved by CMOS inter-stage amplifier and it is basically determined by the output capacitance of the dynamic amplifier.

$$\overline{v_{ni}^2} = \frac{kT\gamma}{C_L}\frac{V_{eff}}{V_{os}}$$



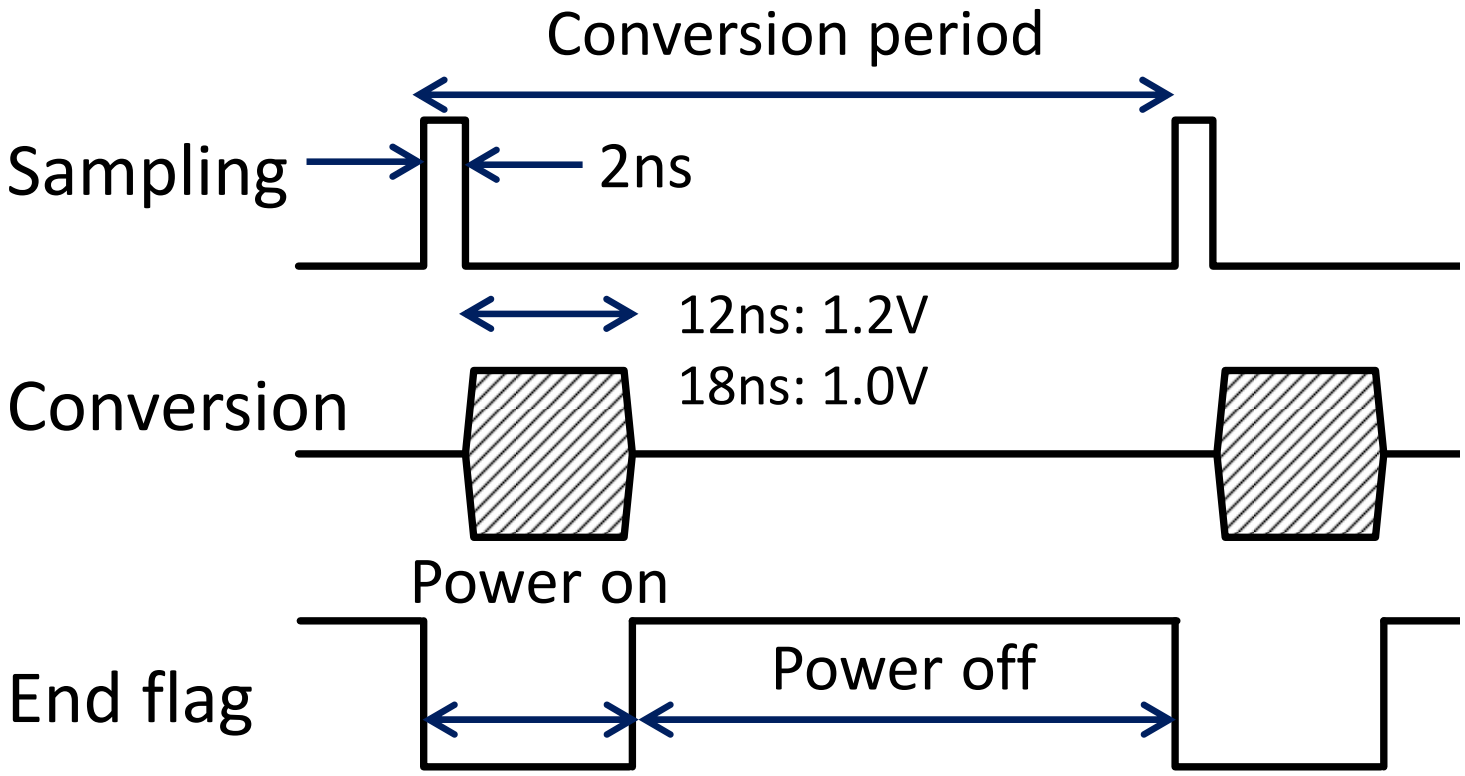


A. Matsuzawa, ASICON 2009, pp. 218-221, Oct. 2009.

Operating timing

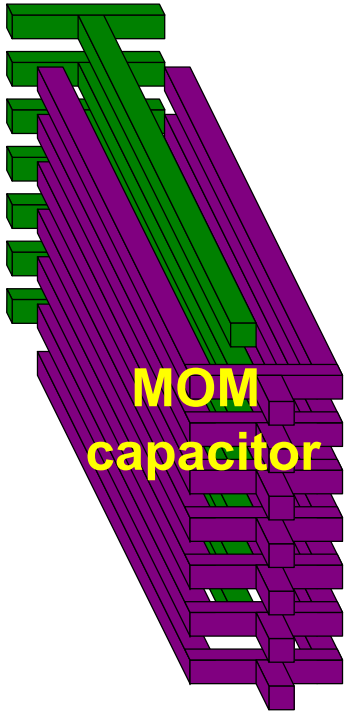
Successive comparison with binary search is started after the sampling period. The end flag becomes high when 12 conversion is completed. The conversion period is about 12 ns. The leakage current can be blocked by using power gating.

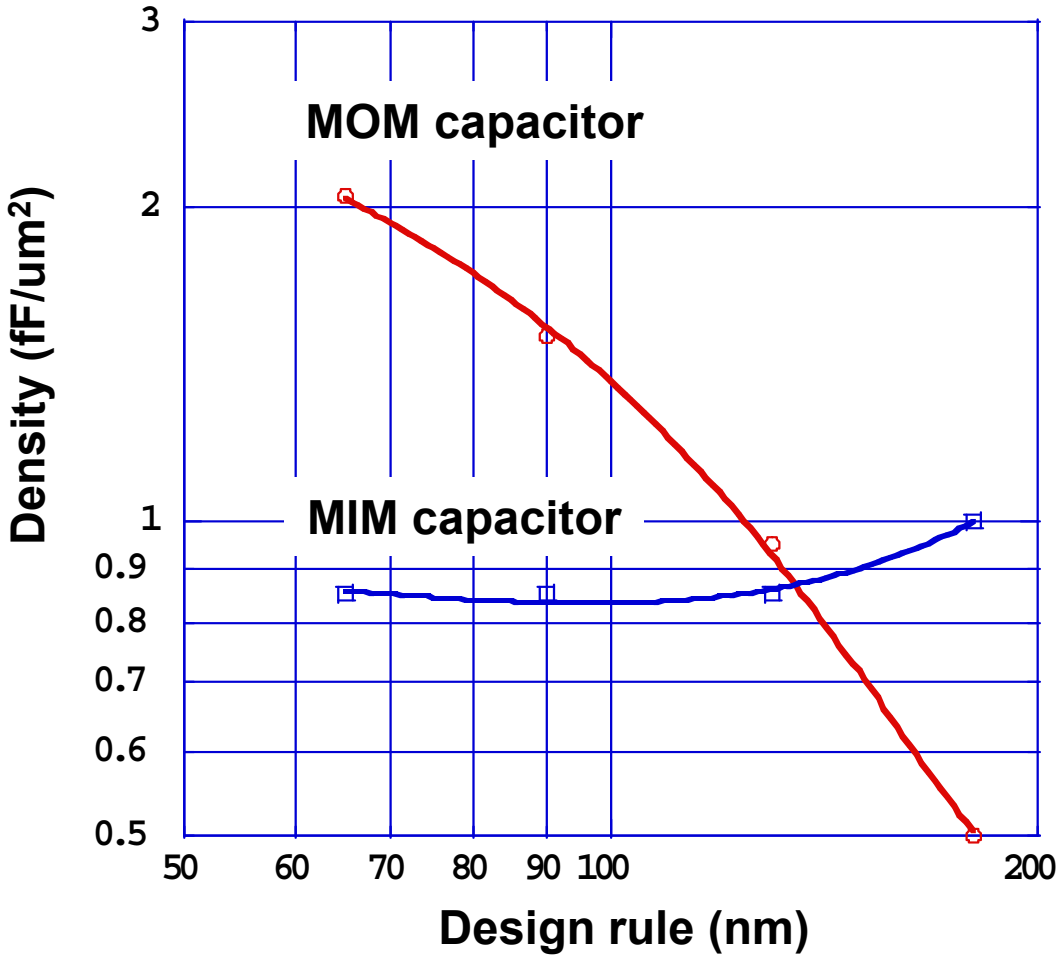
P_d is proportional to the sampling frequency. $P_d = f_s \times E_d$



Use of MOM capacitor

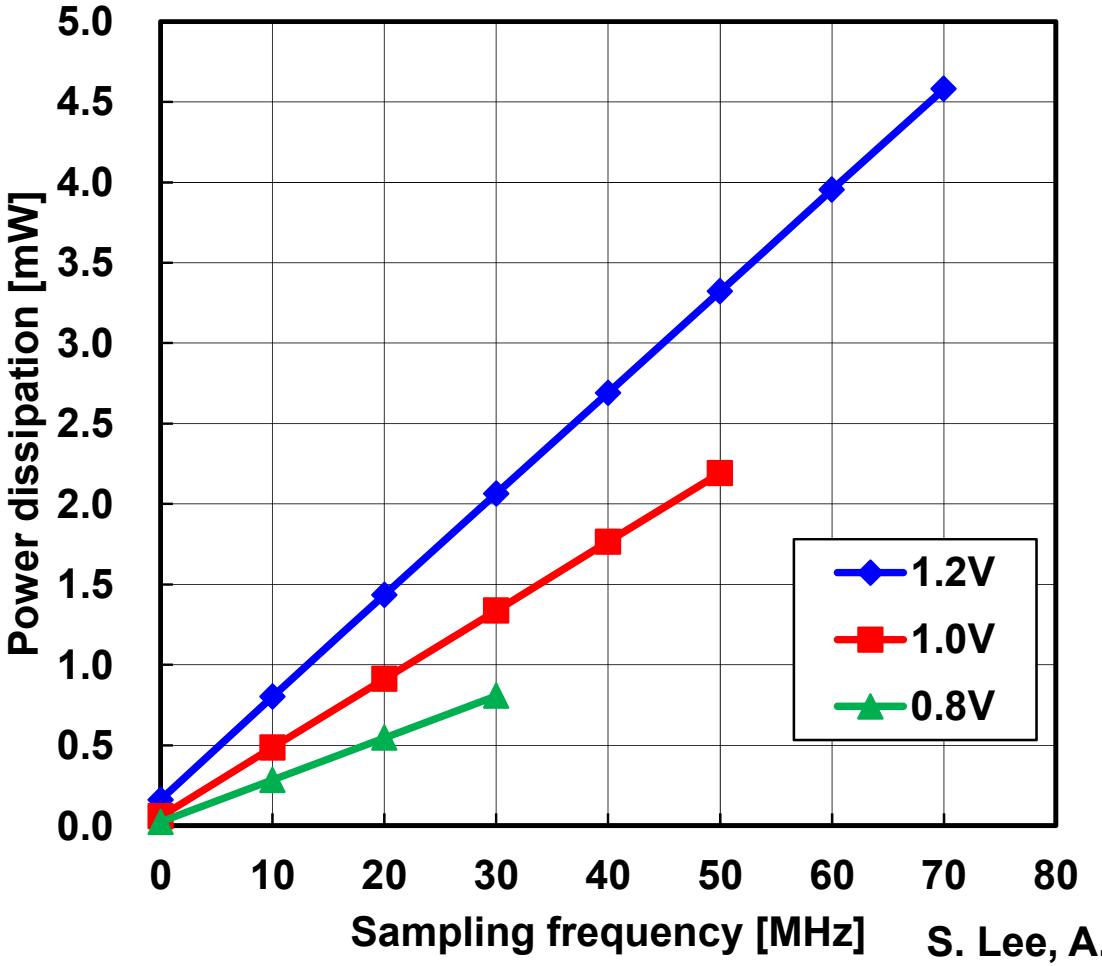
MOM capacitor uses the capacitance between the lateral interconnection.
The capacitor density can be increased by technology scaling.
Smaller occupied area (same C) can be expected by technology scaling.
Furthermore, parasitic capacitance can be controlled.





Scalable power dissipation

P_d is completely proportional to the sampling frequency.
Therefore an ultra-low power is possible at low speed operation.
Further low power is possible by using low voltage operation.



50MSps: 2mW
5MSps: 200uW
500KSps: 20uW
50KSps: 2uW
5kSps: 0.2uW

S. Lee, A. Matsuzawa, et al., SSDM 2013

Performance comparison

TOKYO TECH Pursuing Excellence

- Highest conversion rate：70MSps
- Lowest voltage：0.8V
- Lowest P_d：2.2mW at 50MSps
- Smallest FoM：28fJ
- Smallest area：0.03mm²

12bit SAR ADCs

	This work			[3]	[4]
Resolution (bit)	12			12	12
V_{DD} (V)	0.8	1	1.2	1.2	1.2
fsample (MHz)	30	50	70	45	50
Pd (mW)	0.8	2.2	4.6	3	4.2
SNDR (dB)	62	64	65	67	71
FoM (fJ) Nyq/DC	81/28	62/33	100/45	36/31	36/29
Technology (nm)	65			130	90
Occupied area(mm^2)	0.03			0.06	0.1

S. Lee, A. Matsuzawa, et al., SSDM 2013.
[3] W. Liu, P. Huang, Y. Chiu, ISSCC, pp. 380-381, Feb. 2010.
[4] T. Morie, et al., ISSCC, pp.272-273, Feb. 2013.

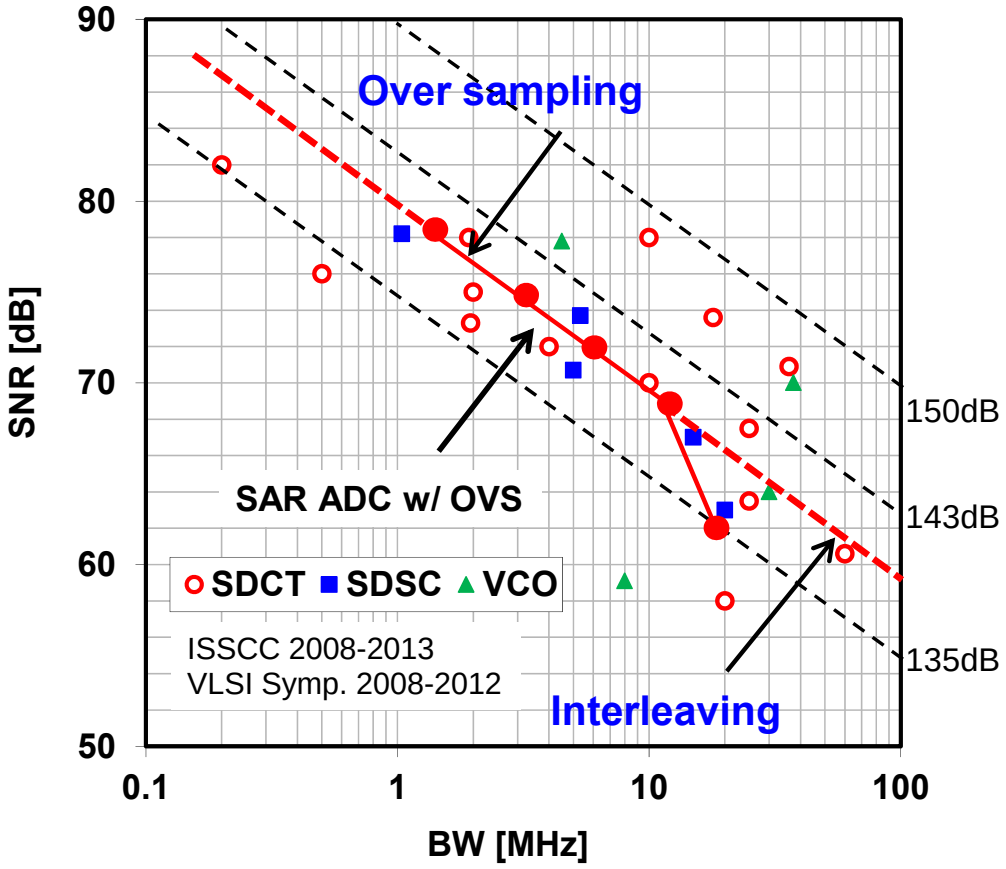
Performance scalable ADC ?

TOKYO TECH Pursuing Excellence

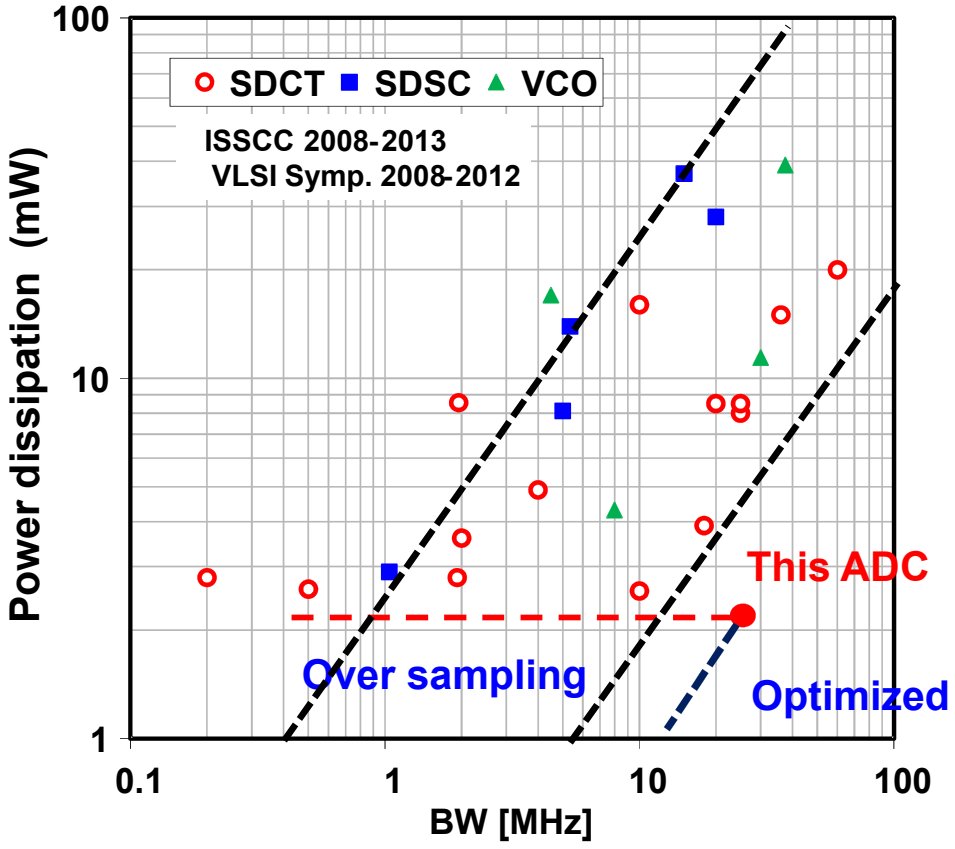
SNR can be increased up to 78 dB by reducing BW.
Smallest P_d among ADCs for wireless communication.

84 dB will be attained by dither and DEM method.
SNR_0 is 140 dB and it should be increased.

S. Lee, A. Matsuzawa, et al., SSDM 2013



1V, 50MSps Operation



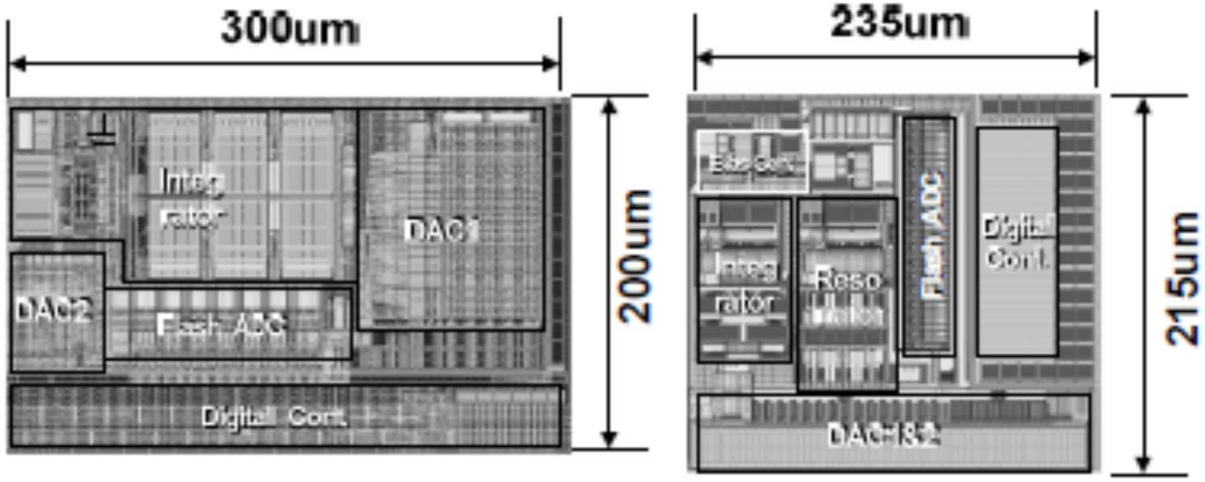
SAR ADC vs. SD ADC

TOKYO TECH Pursuing Excellence

SAR ADC must be better than the SD ADC
; Small area, low power, easy to design, and low voltage of LT. 1.0V.

SAR ADC: Area : 0.03mm^2 (65nm) f_b=25MHz P_d=2.0mW, SNDR=70dB
SDADC: Area : 0.05mm^2 (40nm) f_b=10MHz P_d=2.6mW, SNDR=70dB

Conference	Technology	Area (mm^2)	Power (mW)	SNDR (dB)	DR (dB)	BW (MHz)	Fs (MHz)	FOM (fJ/conv.)	FOM2
Modulator-B	40nm	0.051	2.57	70.0	70.6	10	300	50	166.5
Modulator-A	65nm	0.060	1.36	68.8	69.3	3	186	101	162.0
VLSI2011[4]	40nm	0.085	2.80	78.0	83.0	1.92	246	112	171.4
ISSCC2006[5]	130nm	1.2	20.0	74.0	76.0	20	640	122	166.0
ISSCC2011[6]	90nm	0.15	8.0	63.5	70.0	25	500	125	164.9
ISSCC2009[7]	65nm	0.084	4.52	79.1	80.0	2	128	153	166.5
CICC2010[2]	65nm	0.16	3.6	69.8	70.2	4	140	178	160.7



(a)Modulator-A (b) Modulator-B

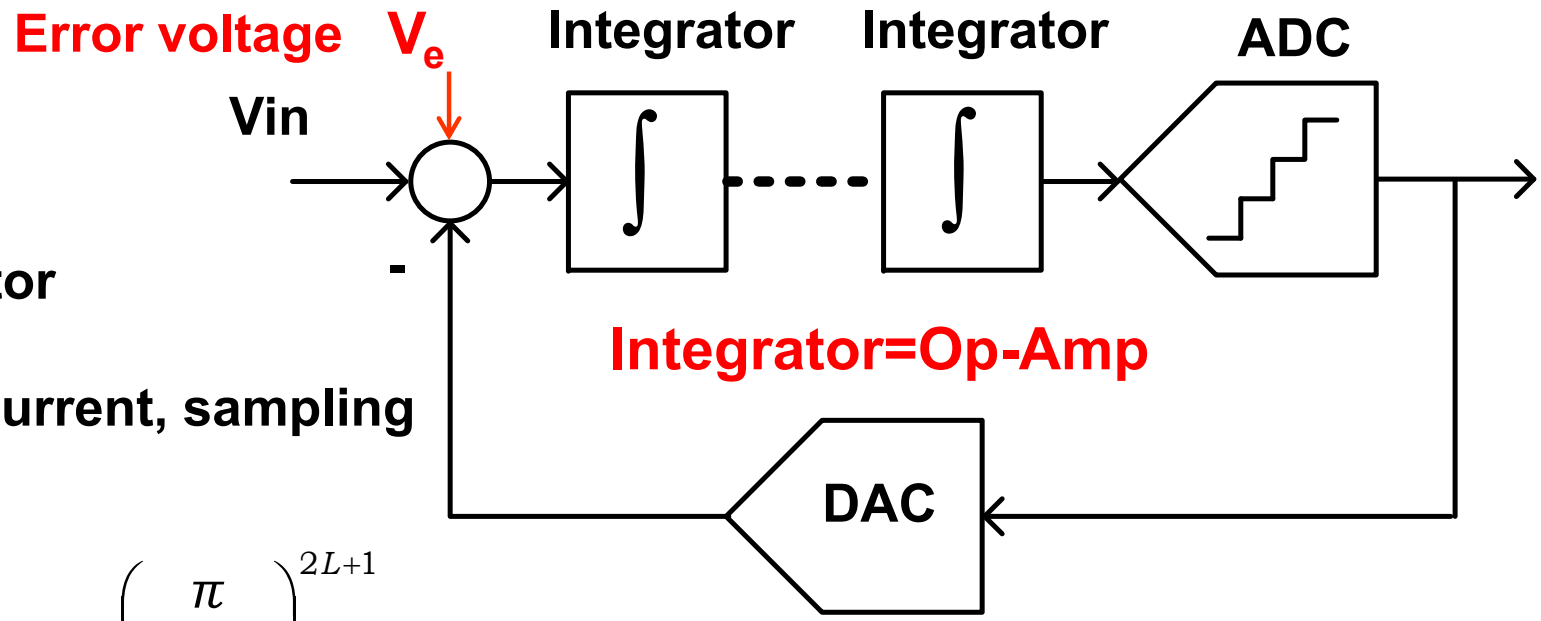
K. Matsukawa,
S. Dosho, VLSI 2012

Sigma-delta ADC

TOKYO TECH Pursuing Excellence

Sigma-delta ADCs are widely used for wireless communications. But….

Sigma delta ADC can suppress only the quantization noise of ADC.
The performance is limited by the input error voltage.
Op-Amp is needed for the integrator and consumes static power.



Error voltage
Noise of 1st integrator
Error of DAC
Noise of Resistor, current, sampling

$$N_q = \left(\frac{V_q}{2}\right)^2 \frac{1}{3\pi(2L+1)}\left(\frac{\pi}{OSR}\right)^{2L+1}$$

Quantization noise can be suppressed so much

$$V_{e\_eff} \approx \frac{V_e}{OSR}$$

Error voltage at input summing node can't be suppressed so much. Suppressed by only OSR.

TOKYO TECH
Pursuing Excellence

7bit 2.2GSps ADC

using time-domain signal processing

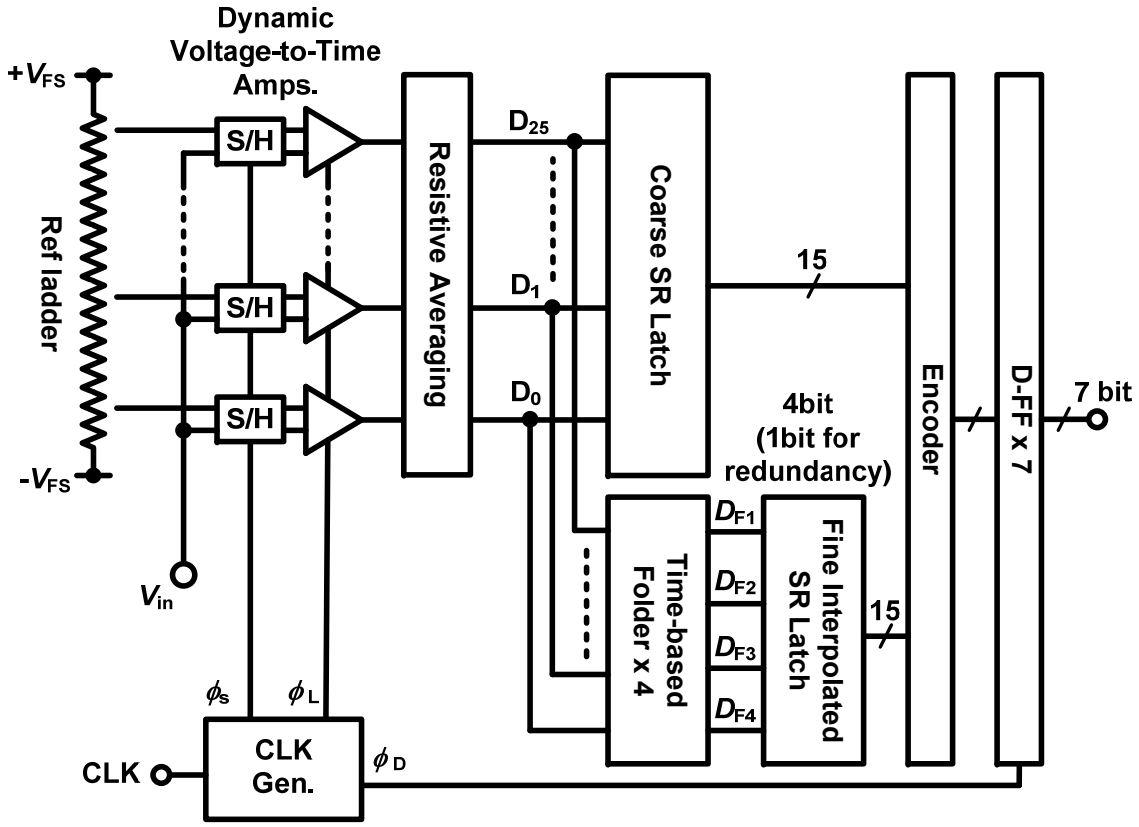
Matsuzawa & Okada Lab.

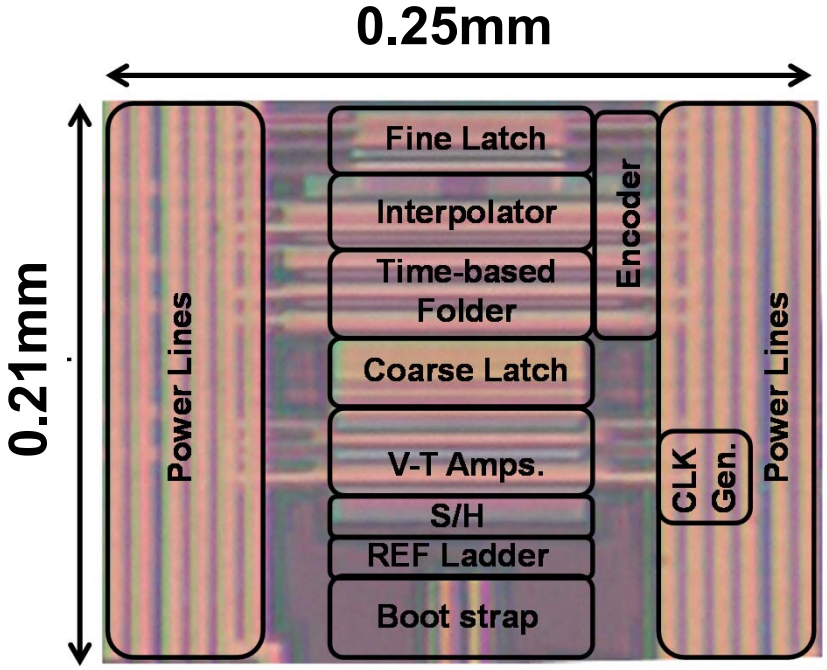
7bit 2.2GSps ADC for 60GHz ABB

TOKYO TECH Pursuing Excellence

- 7bit ADC for the 16QAM modulation
- Convert the voltage difference to the timing difference
- Folding and interpolation are realized by logic gates

M. Miyahara, A. Matsuzawa, ISSCC 2014



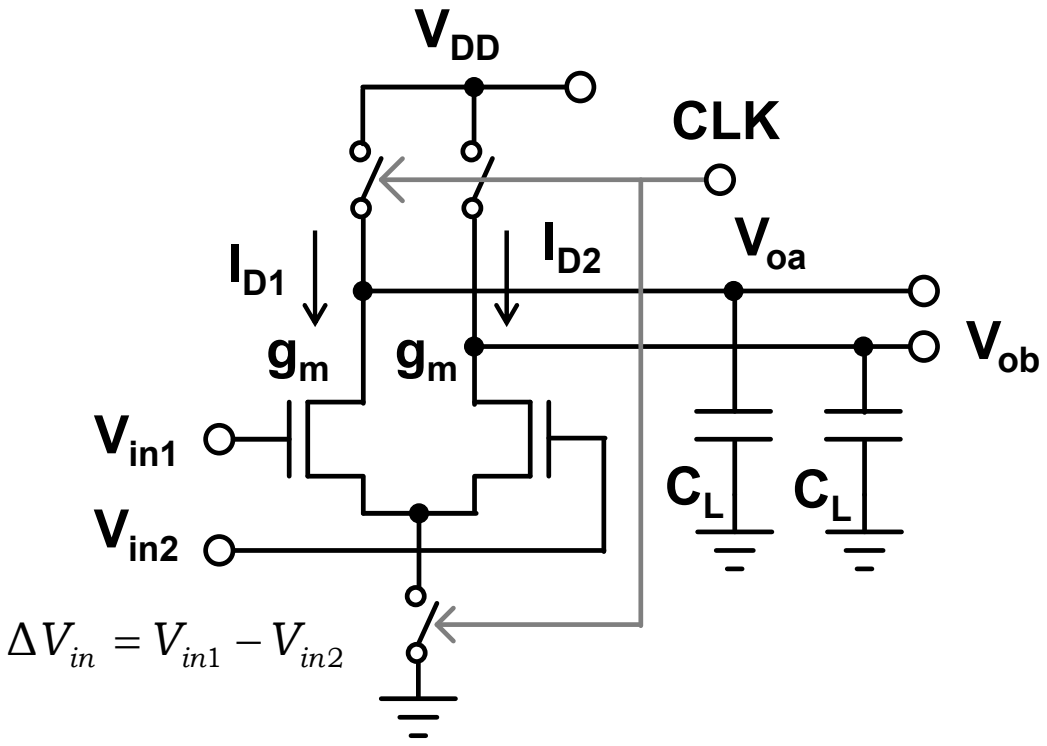


V to T conversion in dynamic amplifier

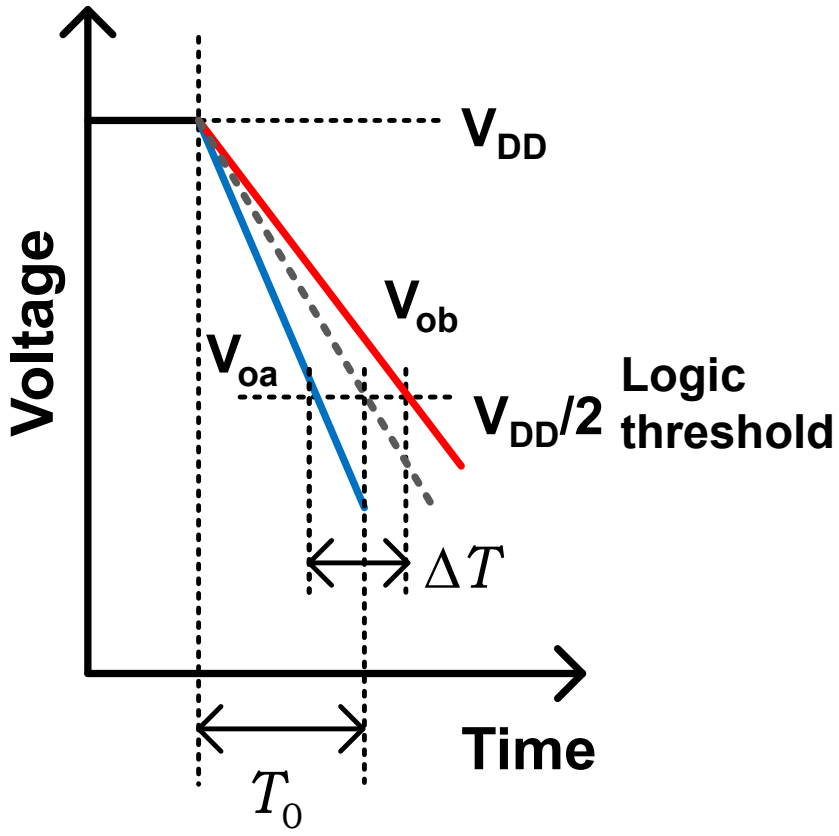
TOKYO TECH Pursuing Excellence

Voltage difference can be changed to time difference in a dynamic amplifier.

$$\Delta T \approx \frac{\Delta V_{in}}{V_{eff}} T_0$$



$$V_{eff} = V_{GS} - V_T$$

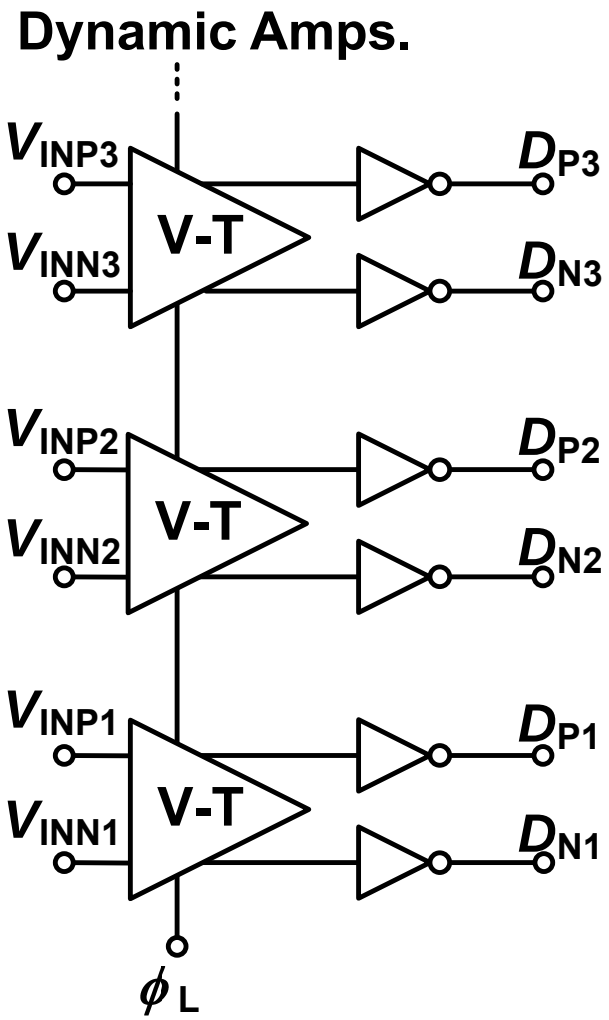


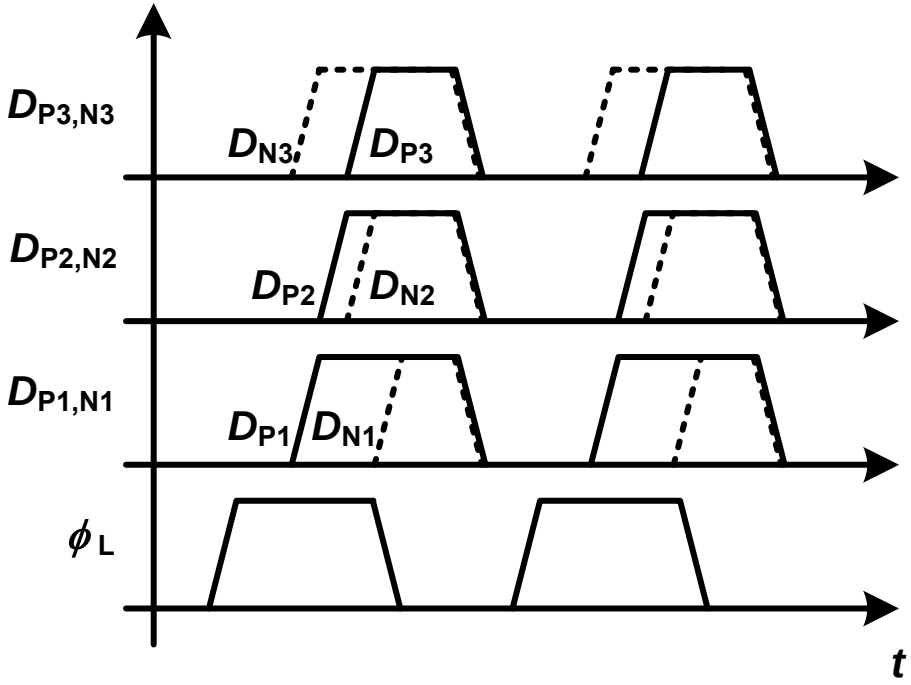
Matsuzawa & Okada Lab.

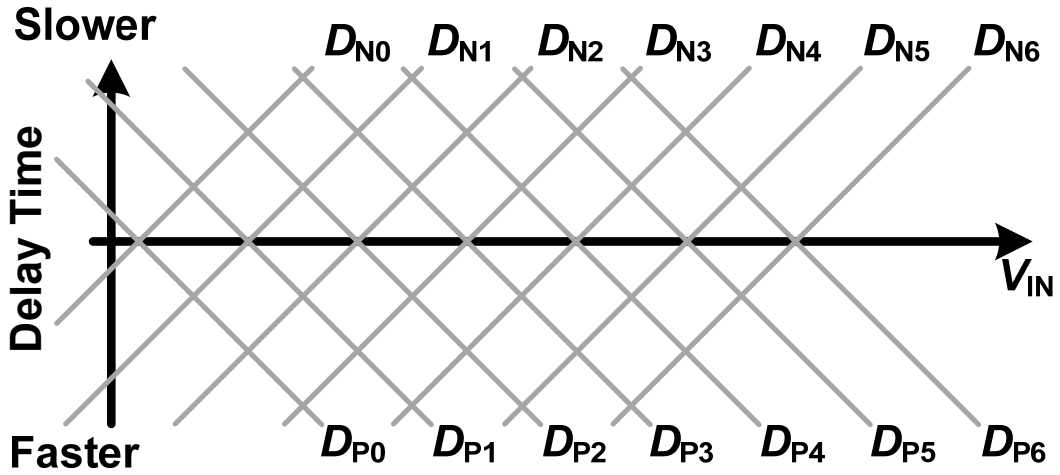
Conversion from the voltage to the timing

TOKYO TECH Pursuing Excellence

The signal generation of larger voltage difference is faster in the dynamic amplifier.



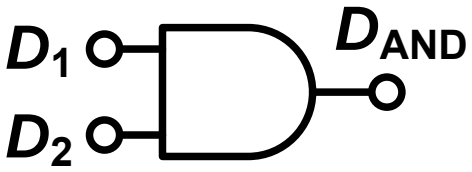


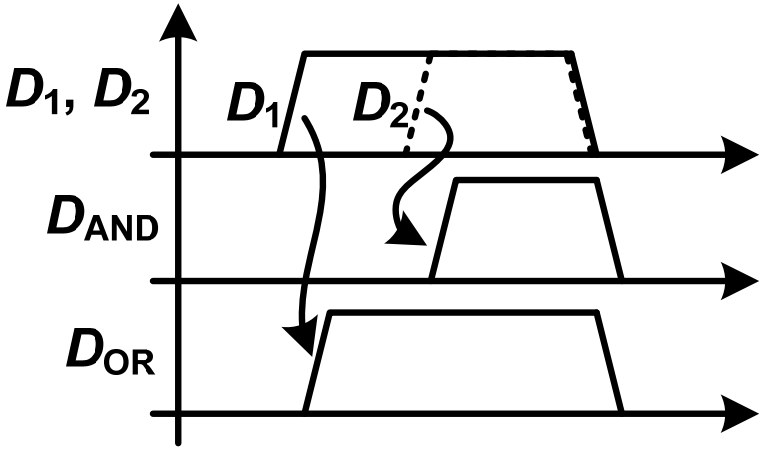


Signal folding in time-domain

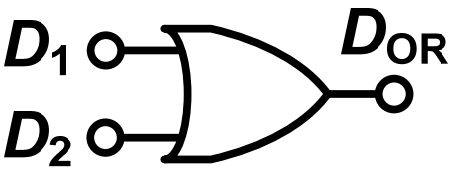
Signal folding in time-domain can be realized easily by simple logic gates.

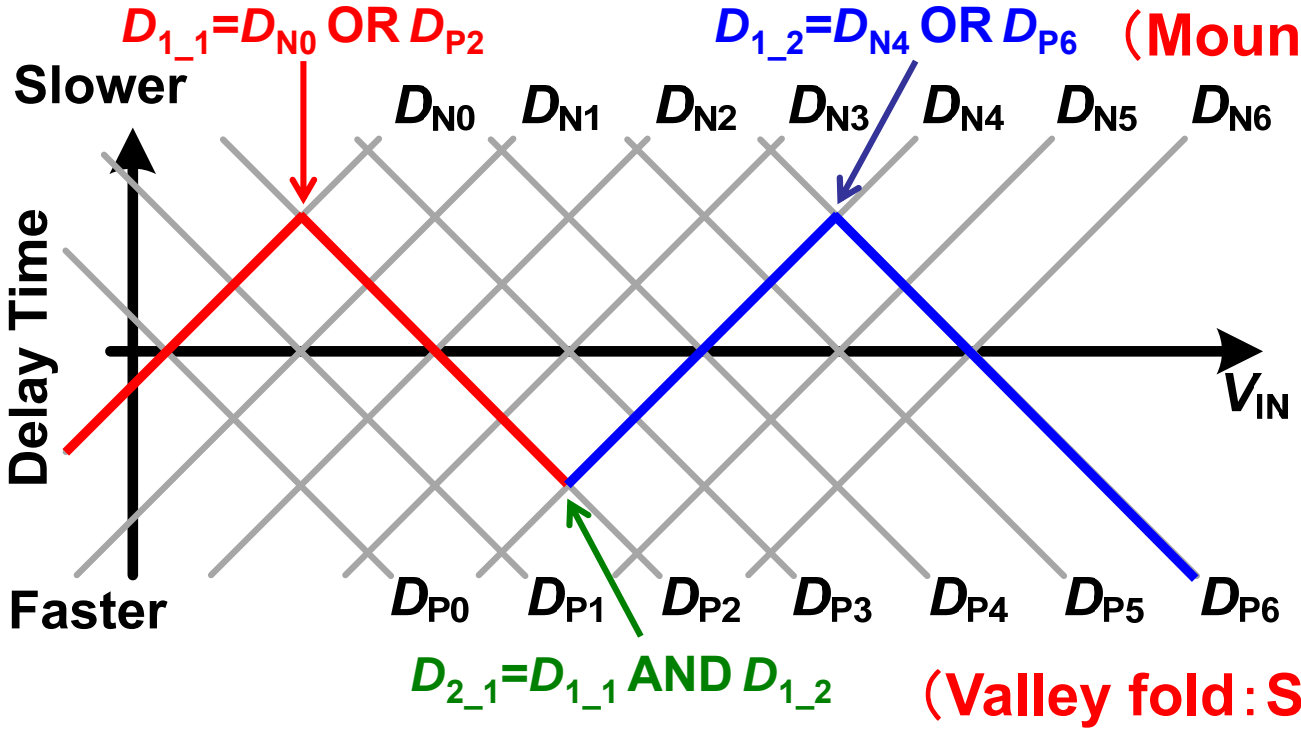
AND: Select late pulse





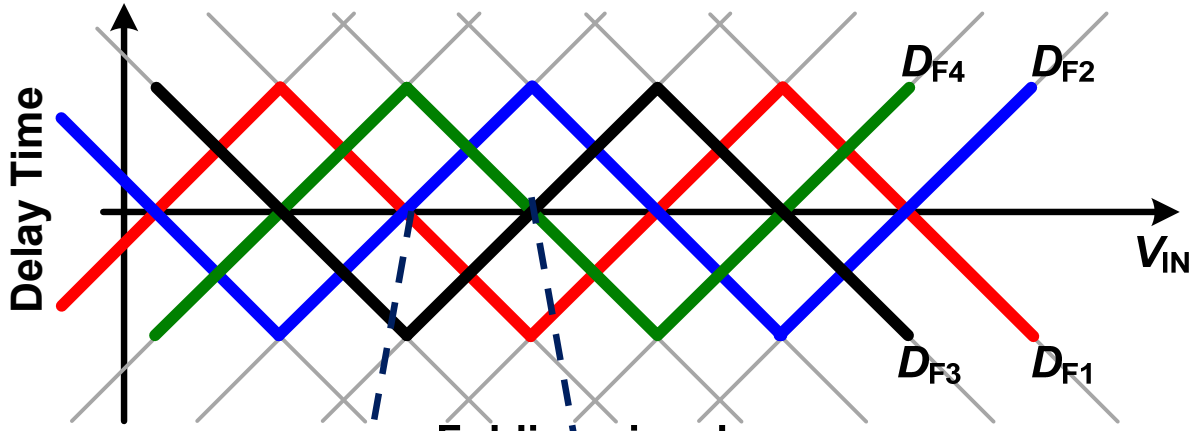
OR: Select early pulse



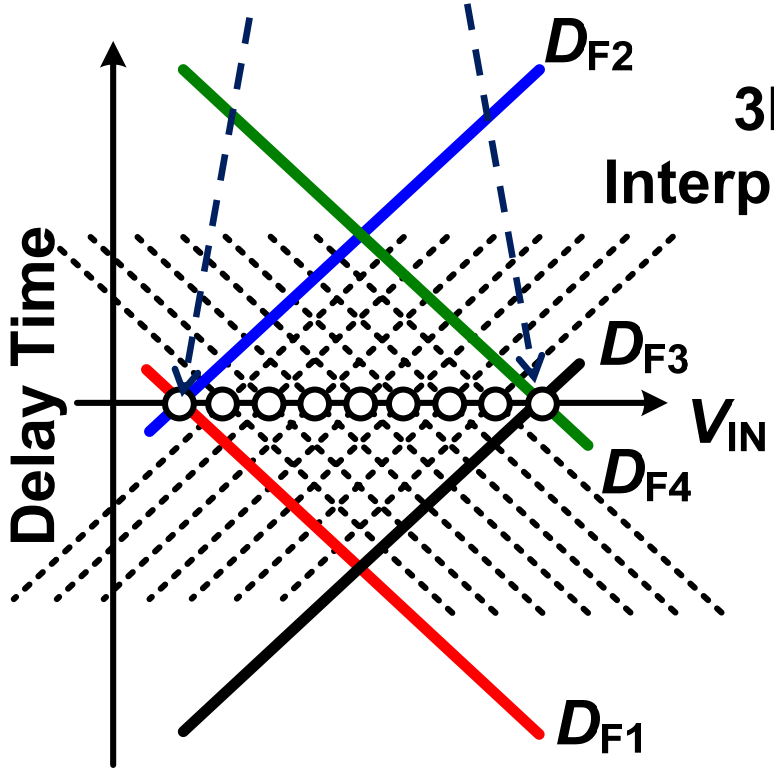


Interpolation between the folded signals

Higher resolution ADC can be realized by interpolating folded signals.

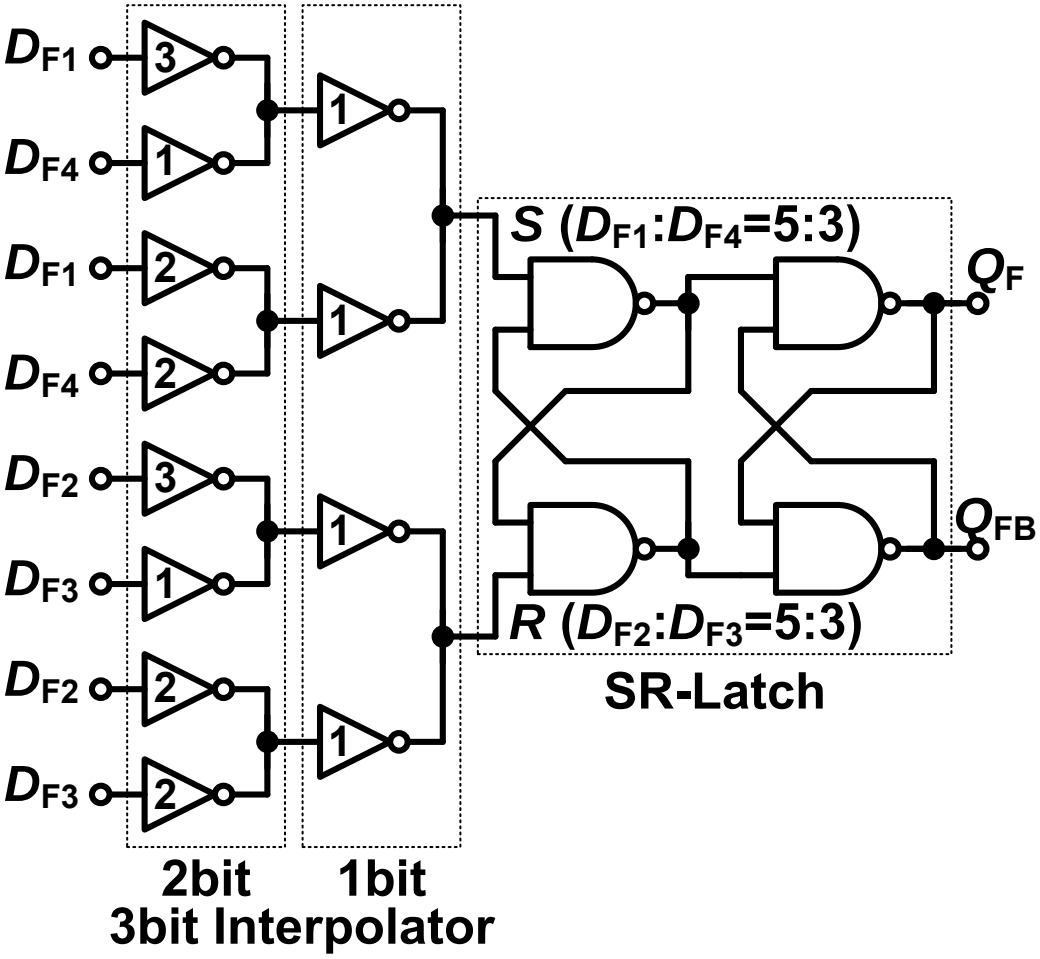


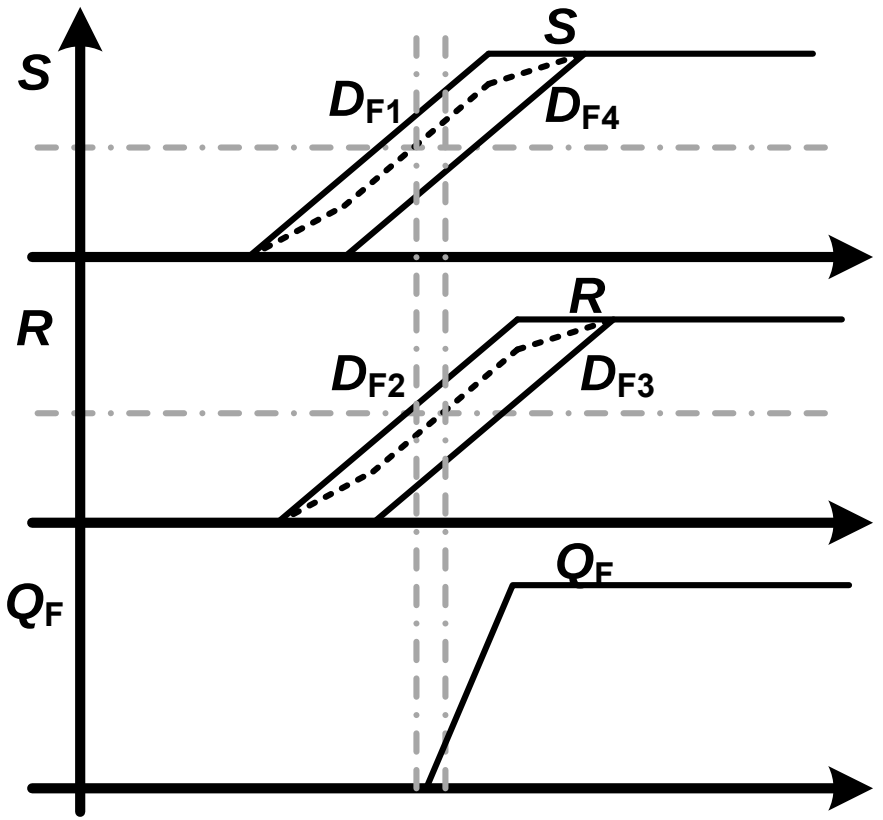
Folding signals



Comparator with interpolation

Interpolation can be made with gate-weighted inverters.
SR latch acts as a comparator by comparing pulse timing





SR-Latch response in the case of interpolation ratio of 5:3

[6] D. Miyashita, *et al*., VLSI symp. 2011

Performance comparison

TOKYO TECH Pursuing Excellence

Highest SNDR of 37.4 dB is attained in flash ADCs
No calibration circuits are required.
This ADC will contribute increase of data rate of 60 GHz transceivers.

P_d is large so far, however can be reduced by the optimization.

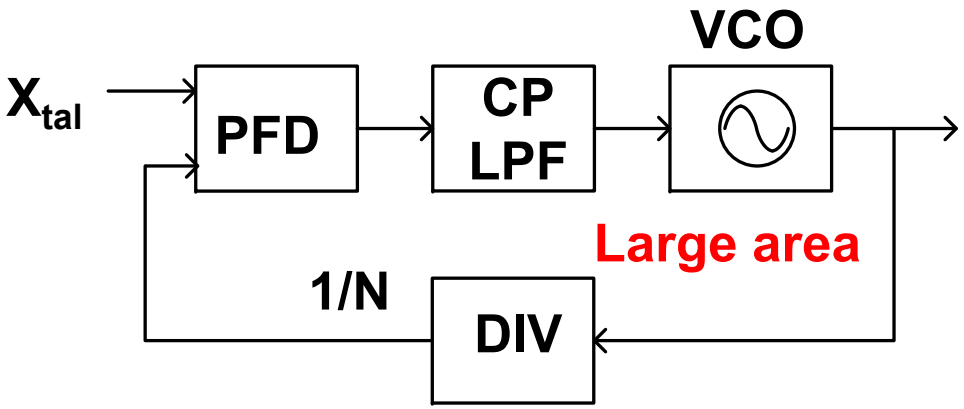
	ISSCC 2008 [3]	VLSI 2012 [8]	VLSI 2013 [9]	This work
Technology	90nm	40nm	32nm SOI	40nm LP
Resolution [bit]	5	6	6	7
Power Supply [V]	1	1.1	0.85	1.1
Sampling Frequency [GS/s]	1.75	3	5	2.2
Power Consumption [mW]	2.2	11	8.5	27.4
SNDR @Nyquist [dB]	27.6	33.1	30.9	37.4
FoMw [fJ/conv.-step]	64.5	99.3	59.4	210
FoMs [dB]	143.5	144.4	145.6	143.3
Core area [mm^2]	0.0165	0.021	0.02	0.052
Calibration	Off chip	Foreground	Off chip	No need

TOKYO TECH
Pursuing Excellence

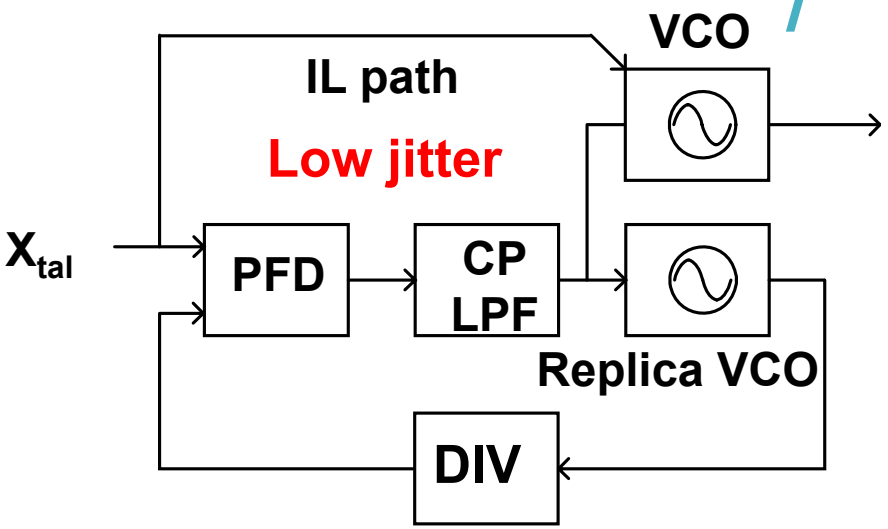
PLL

PLL that can generate accurate frequency and timing will be improved continuously.

Progress of PLL

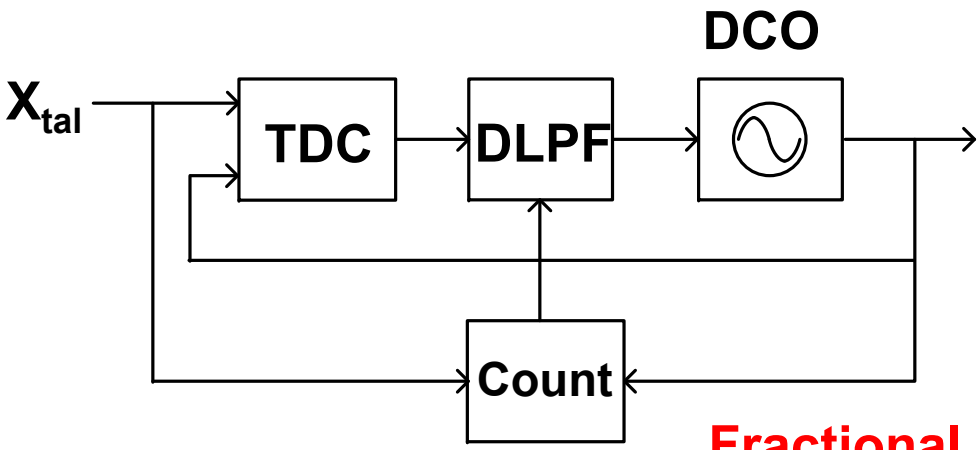


(a) Conventional Charge-pump PLL



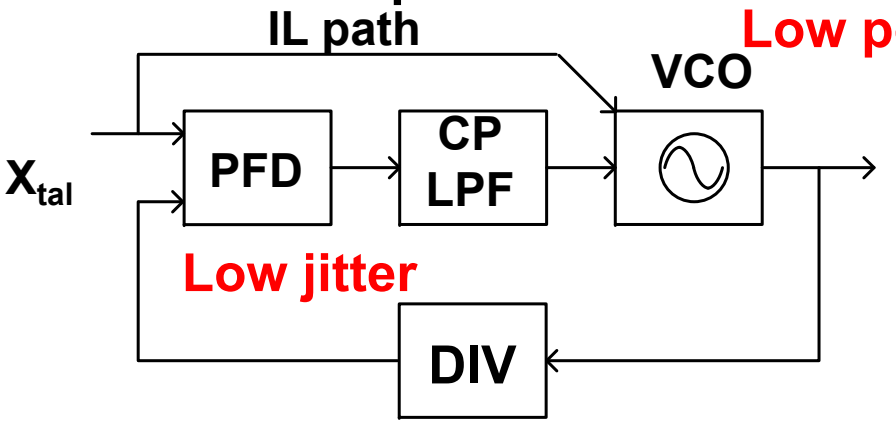
(b) Injection lock (IL) PLL
（with replica VCO）

Small area
Low power



(d) Full digital PLL

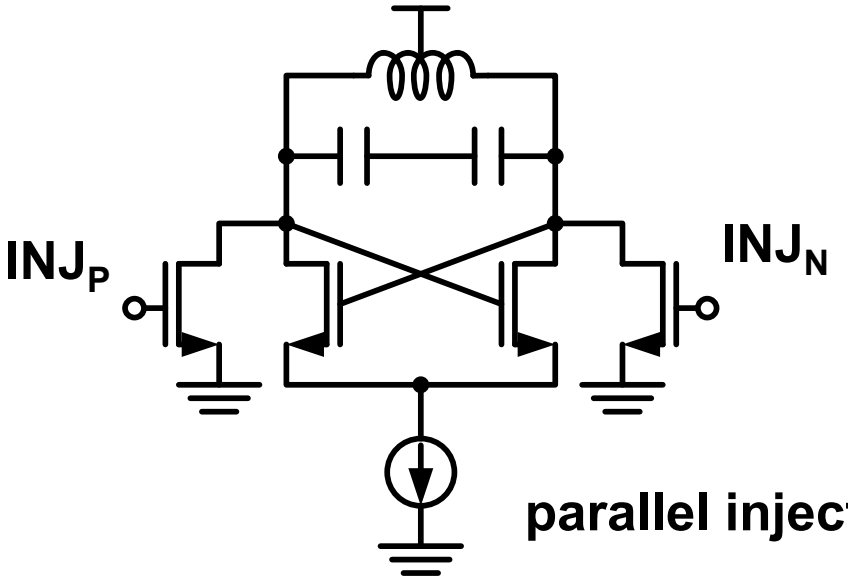
Fractional
Small area
Low jitter



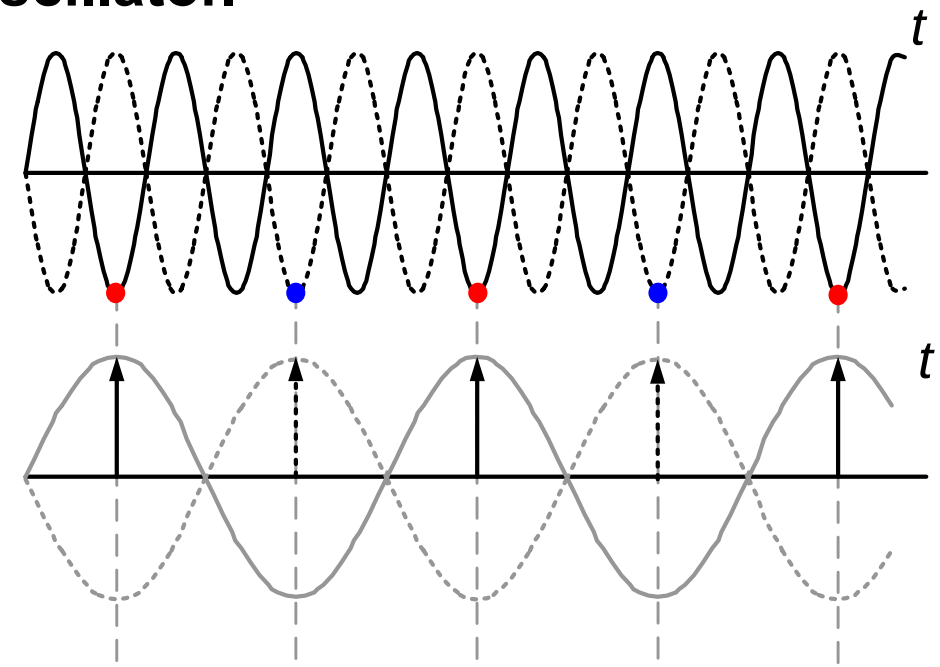
(c) Injection lock (IL) PLL
（ without replica VCO ）

Inject locking (IL) method

Injection locking method can control the phase of higher frequency oscillator by that of lower frequency oscillator.



parallel injection



•Phase noise (jitter) is mandated by the IL pulse

Phase noise of frequency multiplier

$$PN_{\mathrm{ILO}} = PN_{\mathrm{INJ}} + 20\log(N)$$

N: Multiply

Lock range

$$\Delta\omega_L = \frac{\omega_o}{Q} \cdot \frac{I_{inj}}{I_{OSC}} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{OSC}^2}}}$$

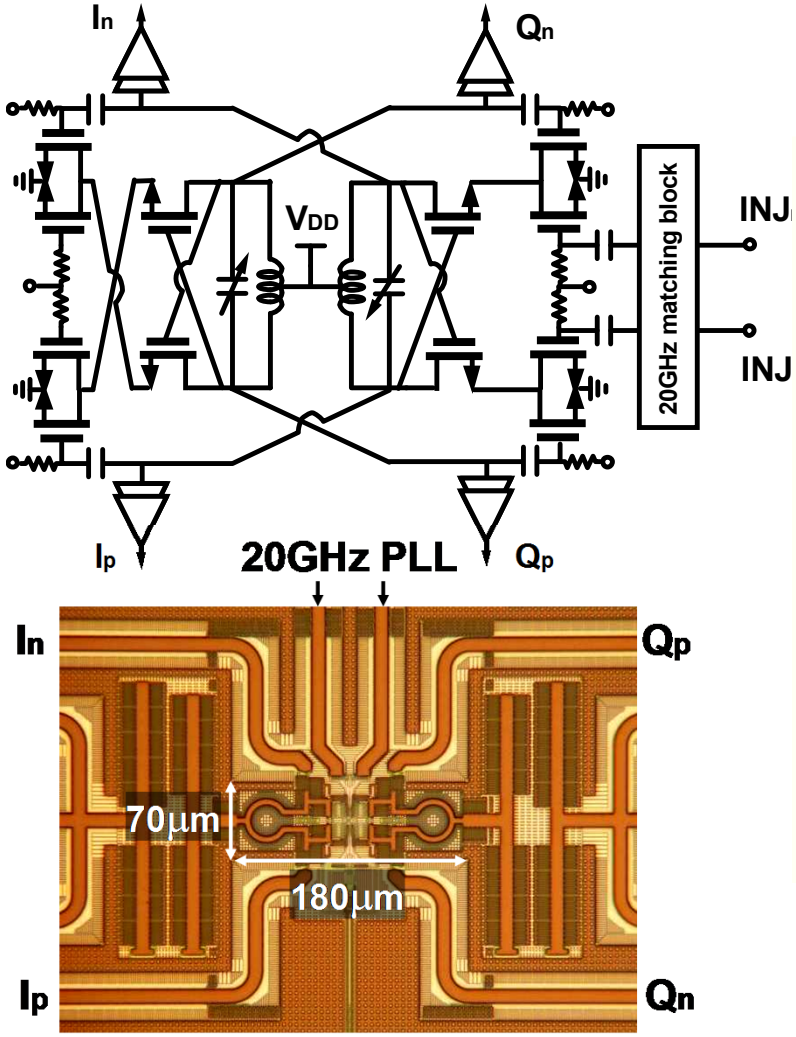
N=3のとき　9.5dB

Low phase noise 60GHz quadrature VCO

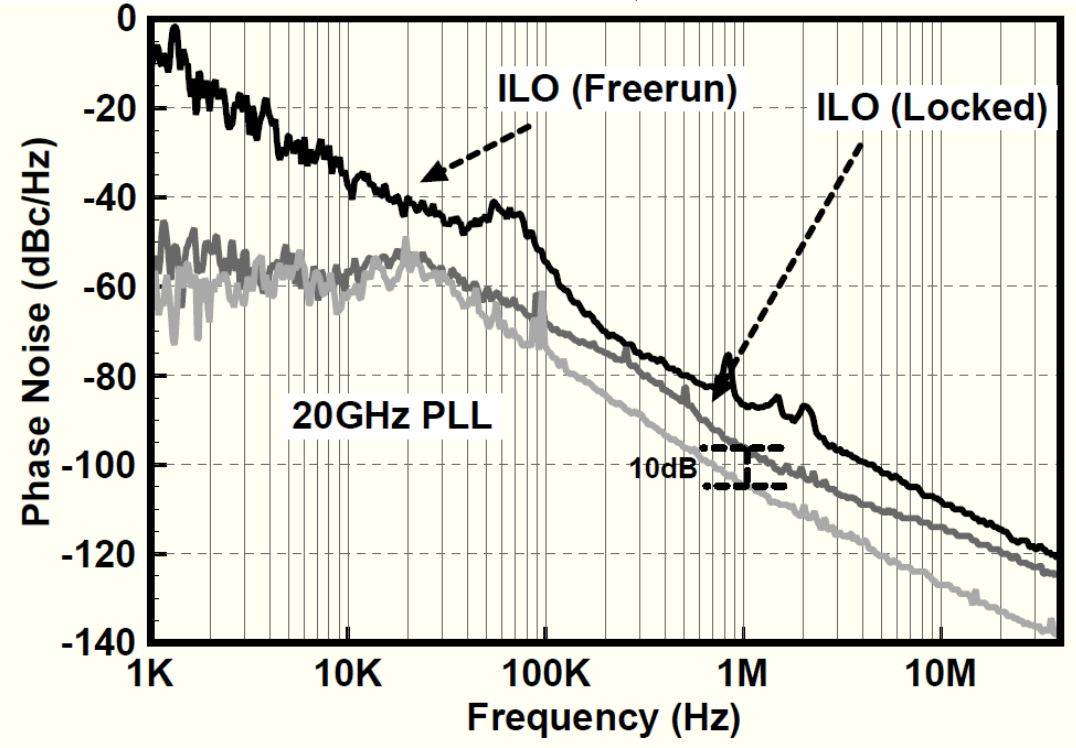
TOKYO TECH

Very low phase noise 60GHz Quadrature VCO has been developed.
60GHz I/Q VCO is locked by low phase noise 20 GHz PLL.

-96dBc/Hz@1MHz is attained. Previous one is -76dBc/Hz@1MHz



It can realize the direct conversion transceivers and 64 QAM.



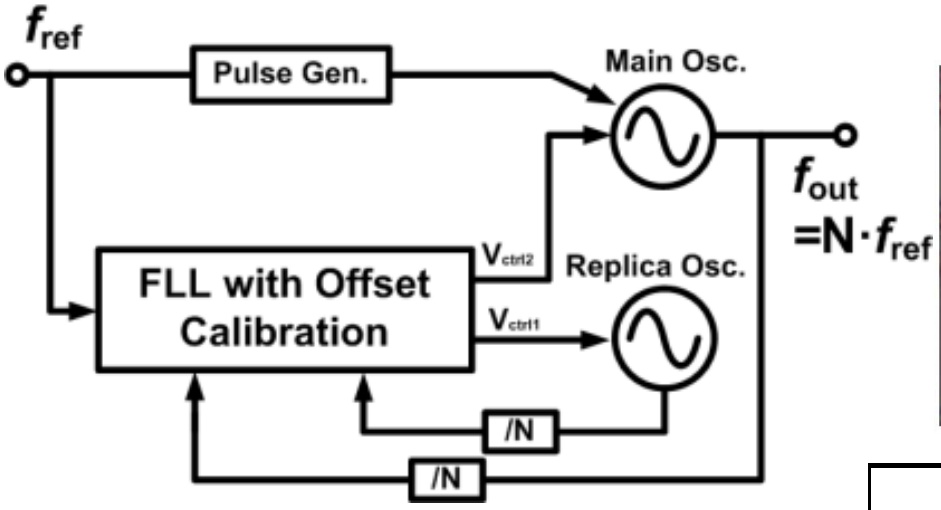
A. Musa, K. Okada, A. Matsuzawa, in A-SSCC Dig. Tech. Papers, pp. 101–102, Nov. 2010.

Small, low jitter, and low power OSC for SoC

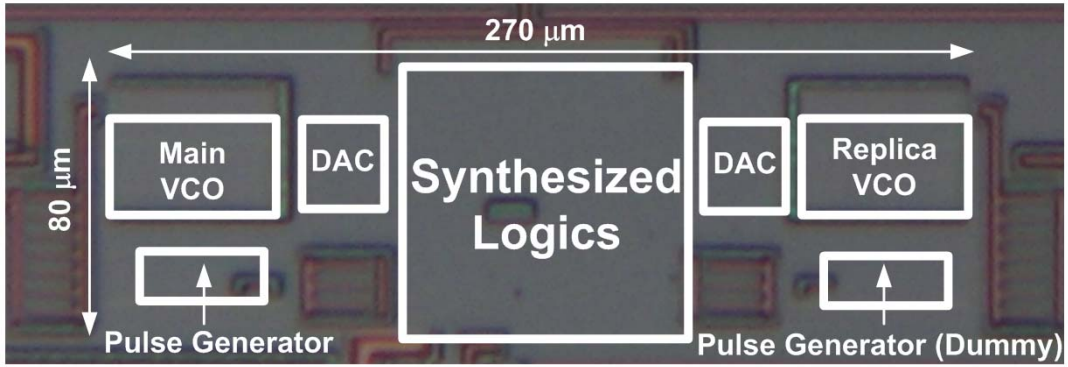
TOKYO TECH Pursuing Excellence

Small, low jitter, and low power ring OSC for SoC by using IL method

Tj=1.8ps, 1.0 mW, 0.02mm²



Automated circuit and layout design will be possible.



IL VCO Comparison

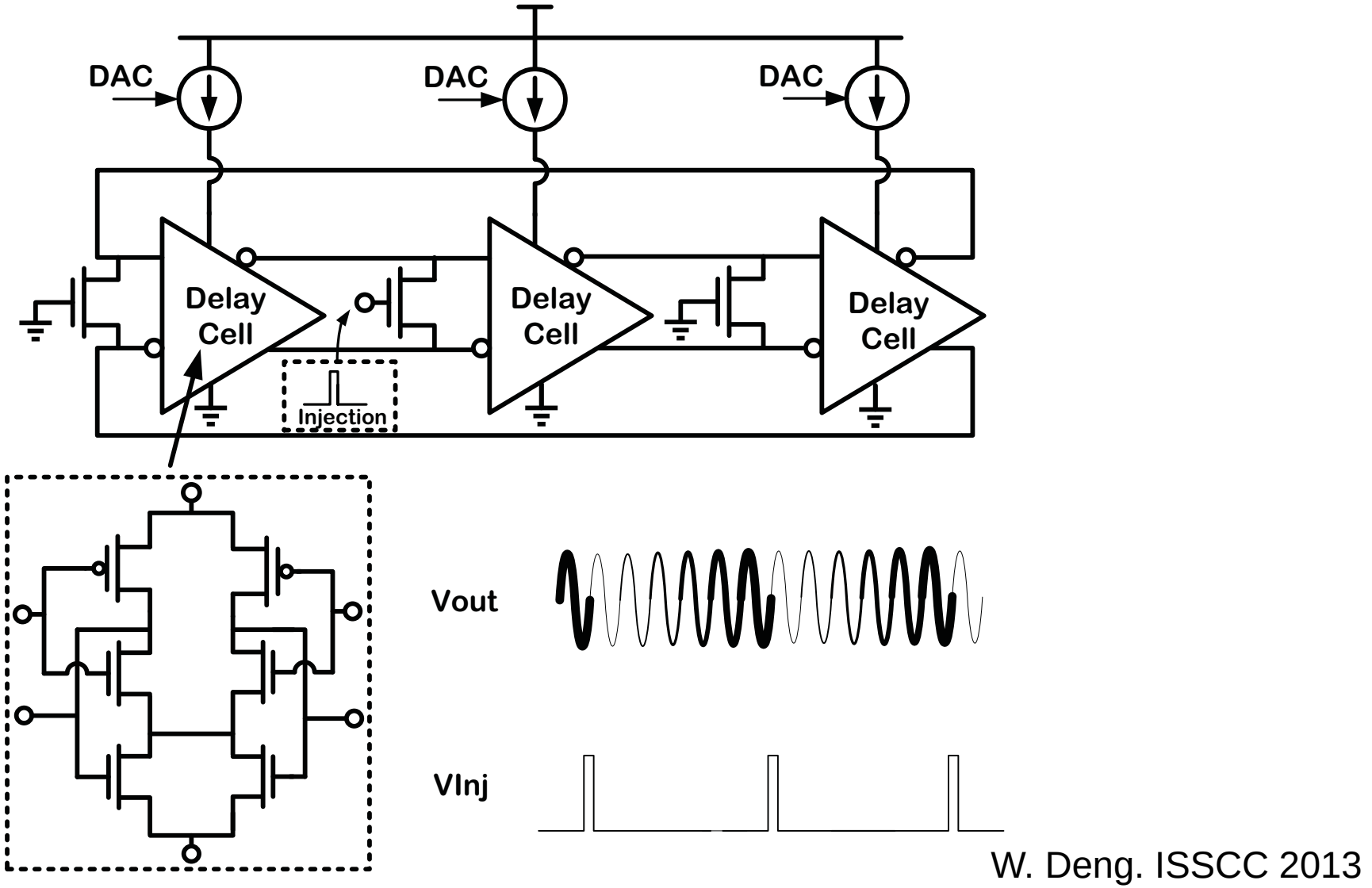
	This work	[1]		[2]	[5]
	IL-PLL	DMDLL	DPLL	MDLL	IL-PLL
Freq. [GHz]	1.2 (0.5-1.6)	1.5 (0.8-1.8)	1.5 (0.8-1.8)	1.6	0.216
Ref. [MHz]	300 (40-300)	375	375	50	27
Power [mW]	0.97	0.89	1.35	12	6.9
Area [mm²]	0.022	0.25	0.25	0.058	0.03
Integ. Jitter [ps]	0.7	0.4	3.2	0.68	2.4
Jitter RMS/PP [ps]	1.81/19.4 10M hits	0.92/9.2 5M hits	4.2/33 5M hits	0.93/11.1 30M hits	N.A.
FOM [dB]	-243	-248.46	-228.59	-233.76	-225
CMOS Tech.	65nm	130nm	130nm	130nm	55nm

W. Deng, K. Okada, A. Matsuzawa, ISSCC 2013

Injection-locked Ring Oscillator

TOKYO TECH Pursuing Excellence

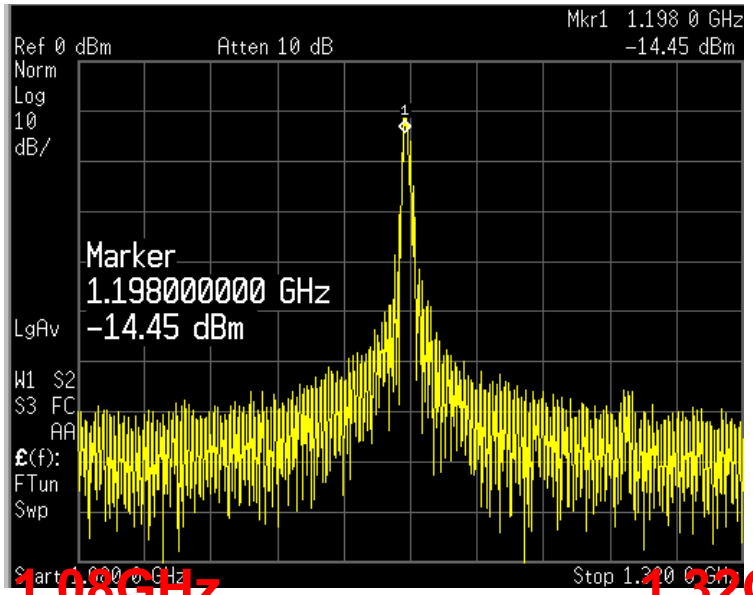
Differential ring VCO with injection locking



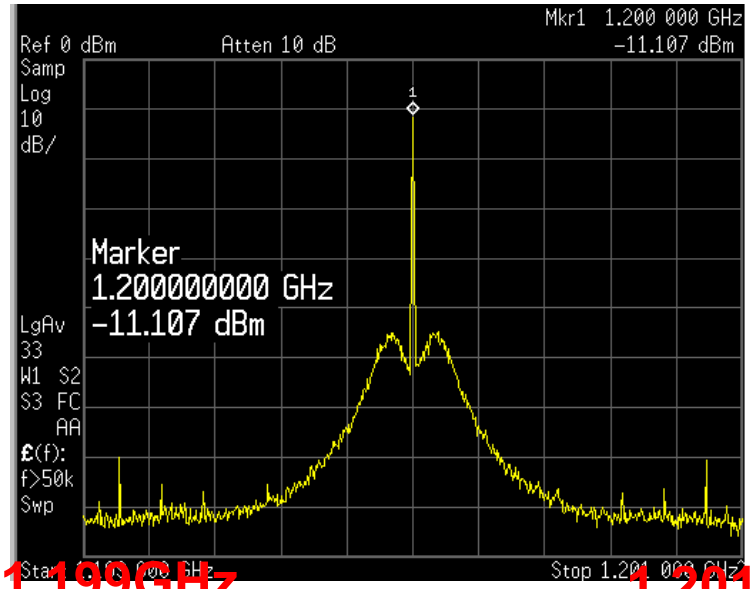
W. Deng. ISSCC 2013

Effect of the injection locking

TOKYO TECH Pursuing Excellence

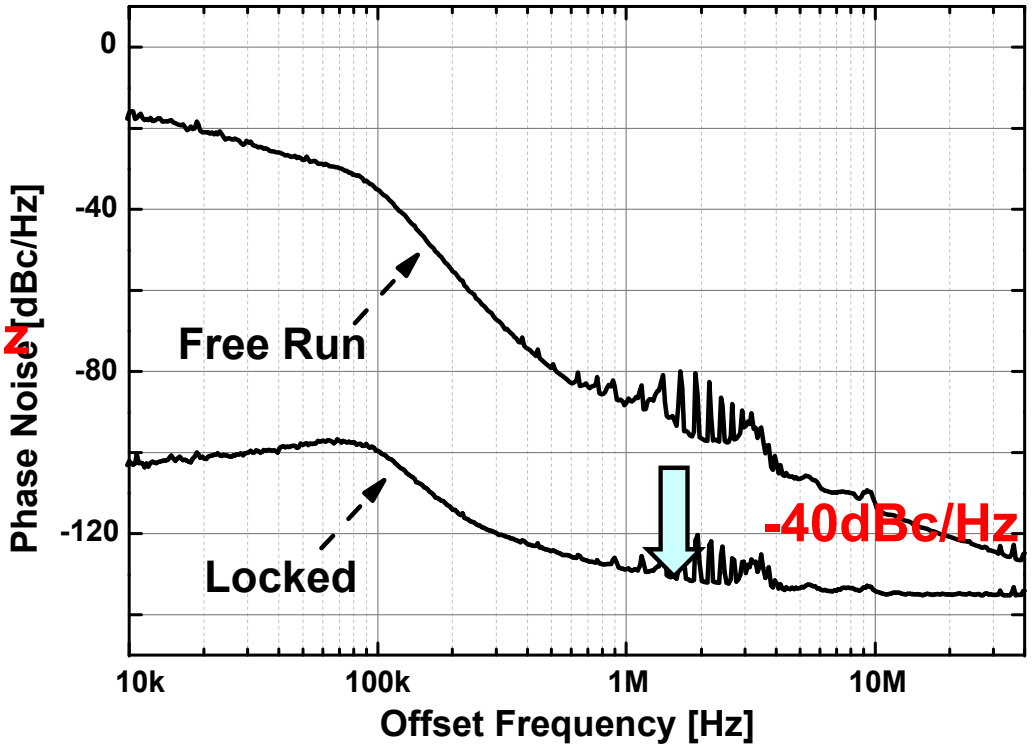


1.08GHz 1.32GHz



1.199GHz 1.201GHz

Phase noise is reduced so much by the injection locking



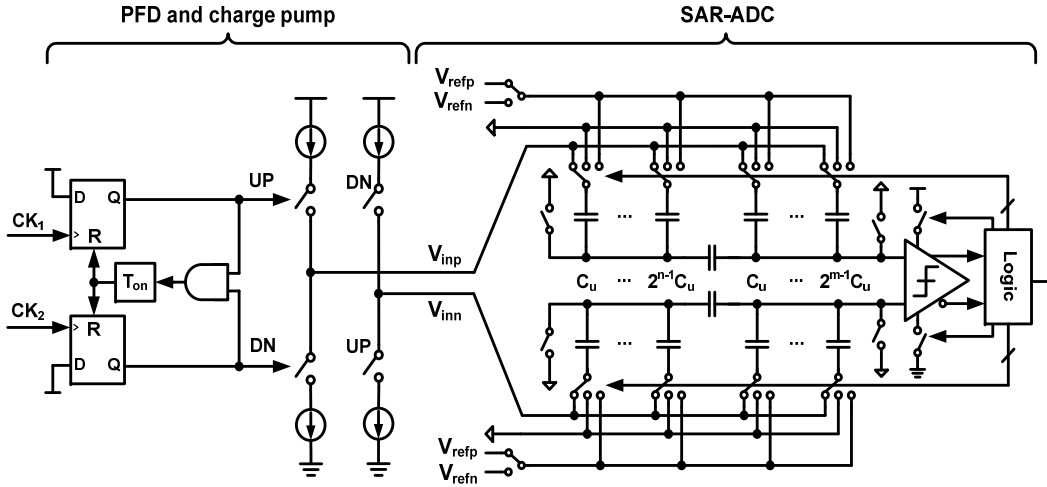
Ref.: 300MHz (40MHz-300MHz) Freq.: 1.2GHz (0.5-1.6GHz)
Integrated jitter: 0.7ps (10kHz-40MHz) Pdc: 0.97mW (1.2GHz)

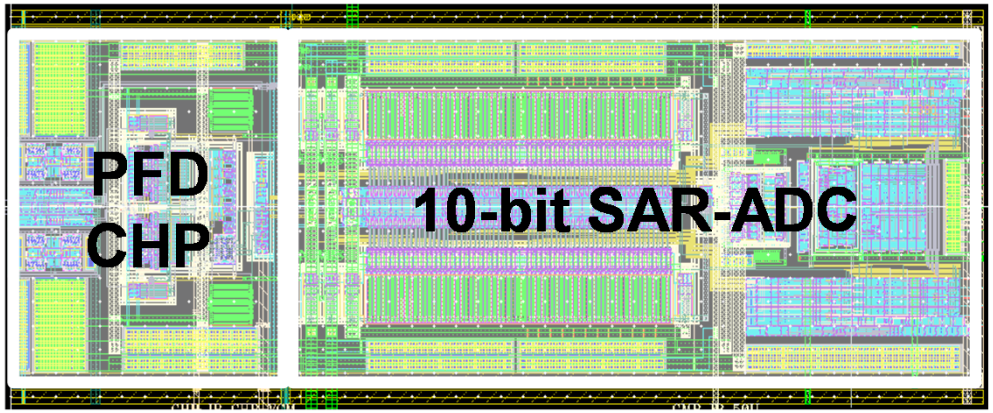
High precision Time to Digital Converter

TOKYO TECH Pursuing Excellence

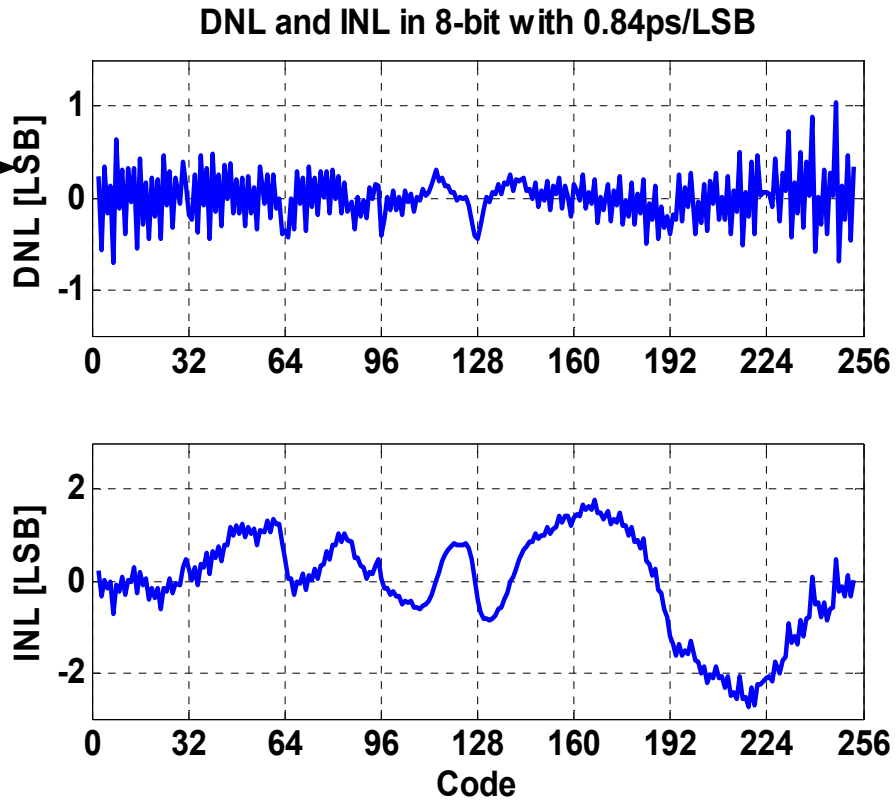
Charge pump + SAR ADC realizes sub-ps TDC
Resolution of conventional inverter based TDC is 10 ps at most.

Low phase noise fractional PLL
On-chip jitter measurement
Sub-mm laser radar





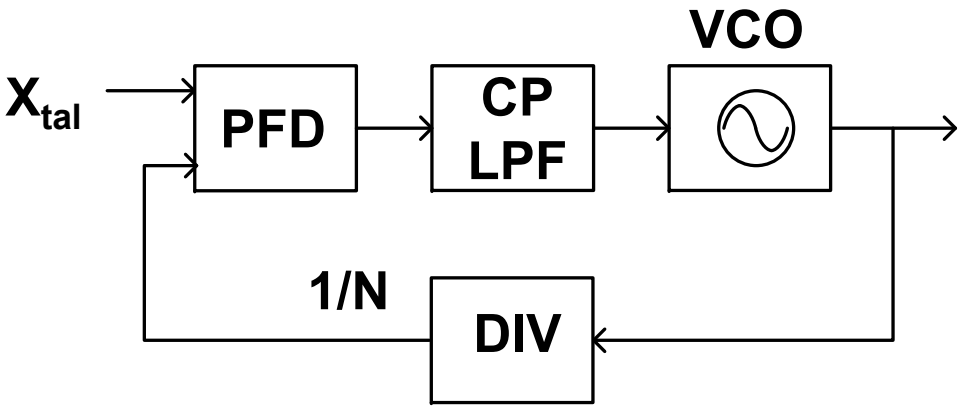
0.8ps, 10bit, 100Msps, 4mW, 0.02mm^2



Z. Xu, A. Matsuzawa, CICC 2013.

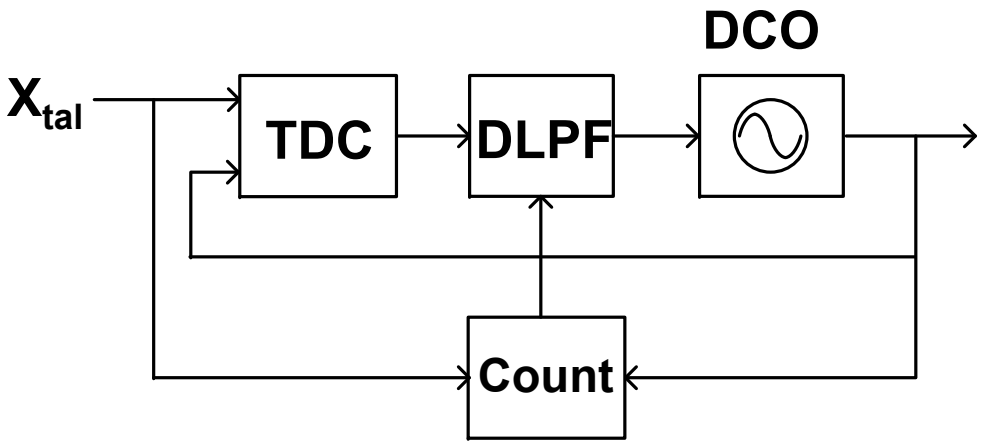
Expectation of full digital PLL

PLL is one of the rare area that digital technology is not used.
Conventional charge pump PLL has an essential limitation, however high precision TDC has not been developed.
The success of high precision TDC will realize high performance Full Digital PLL.



Large area
Not adaptive

Conventional Charge-pump PLL



Full digital PLL

Fractional
Small area
Adaptive
Low jitter

TOKYO TECH
Pursuing Excellence

Layout-driven circuit design and programmable analog circuit technique

Why automated analog design?

TOKYO TECH Pursuing Excellence

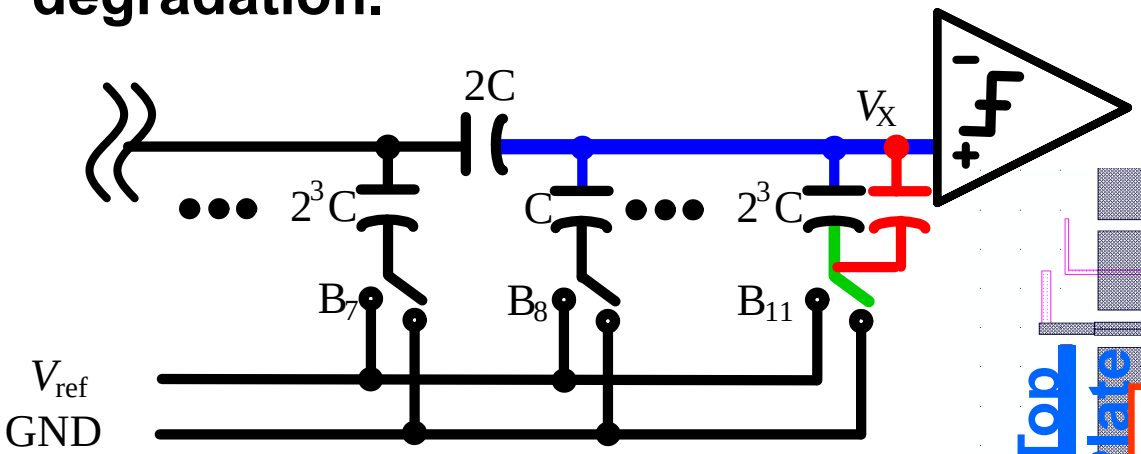
- **Motivation**
  - Lack of analog circuits designers
  - Analog circuits design will continue to be difficult
    - Less margin for low voltage operation
  - Short development time and cost saving are required

- **Solution**
  - Regular structure layout
    - Can realize small area, low power, high speed
    - Can control parasitic components
    - Can use automated layout design
  - Select circuits that have high robustness

Issue of current design method

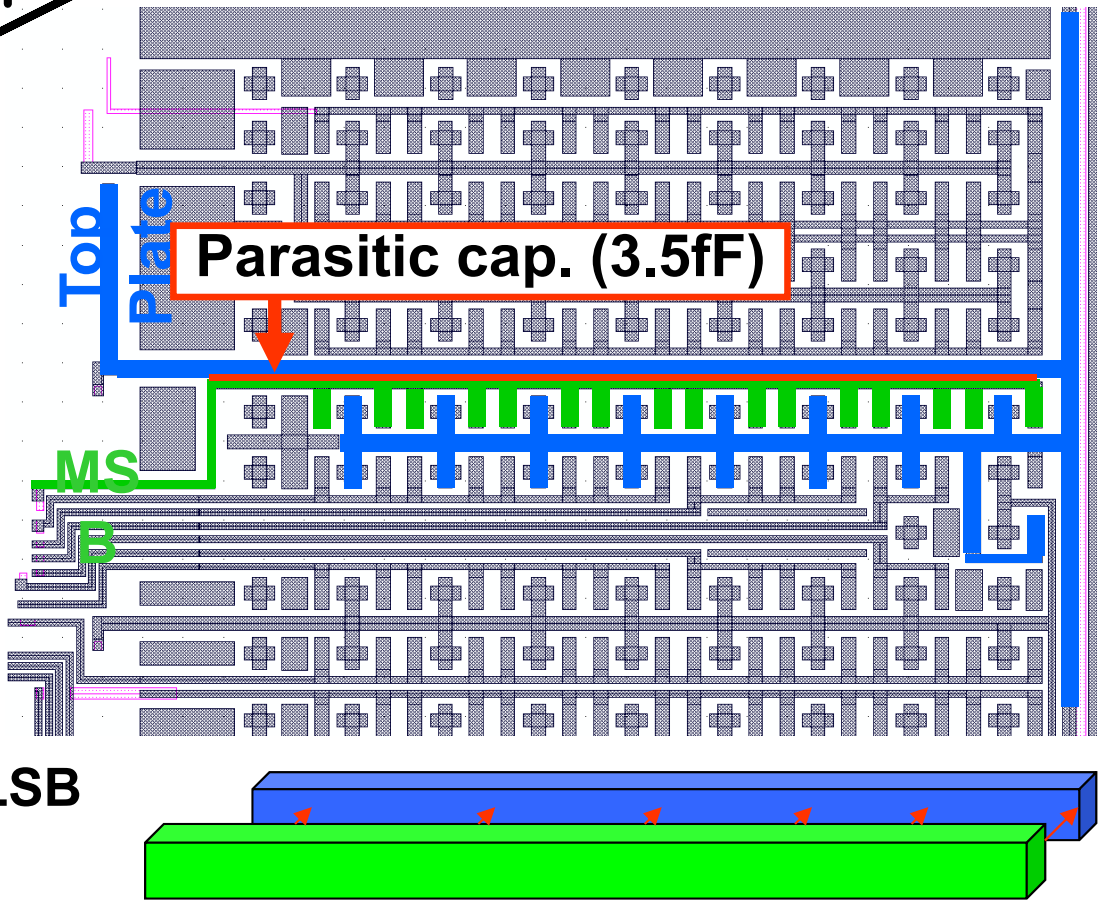
TOKYO TECH Pursuing Excellence

A conventional layout idea of Place the components and Route them causes parasitic components essentially and it results in performance degradation.



CDAC

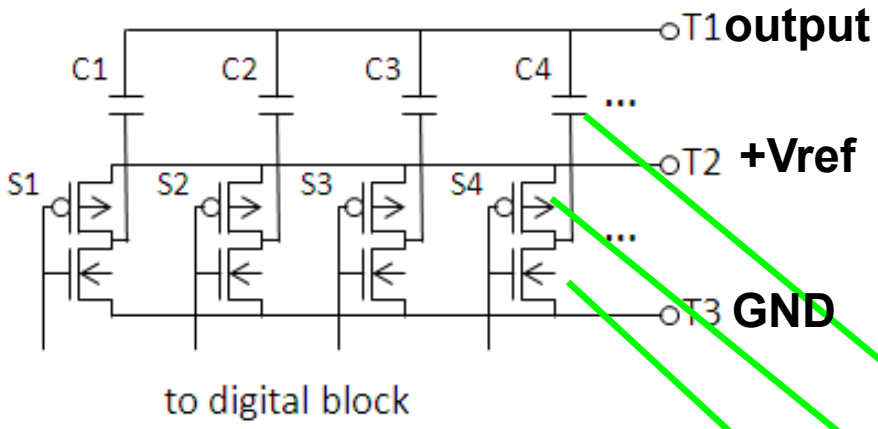
Layout of CDAC



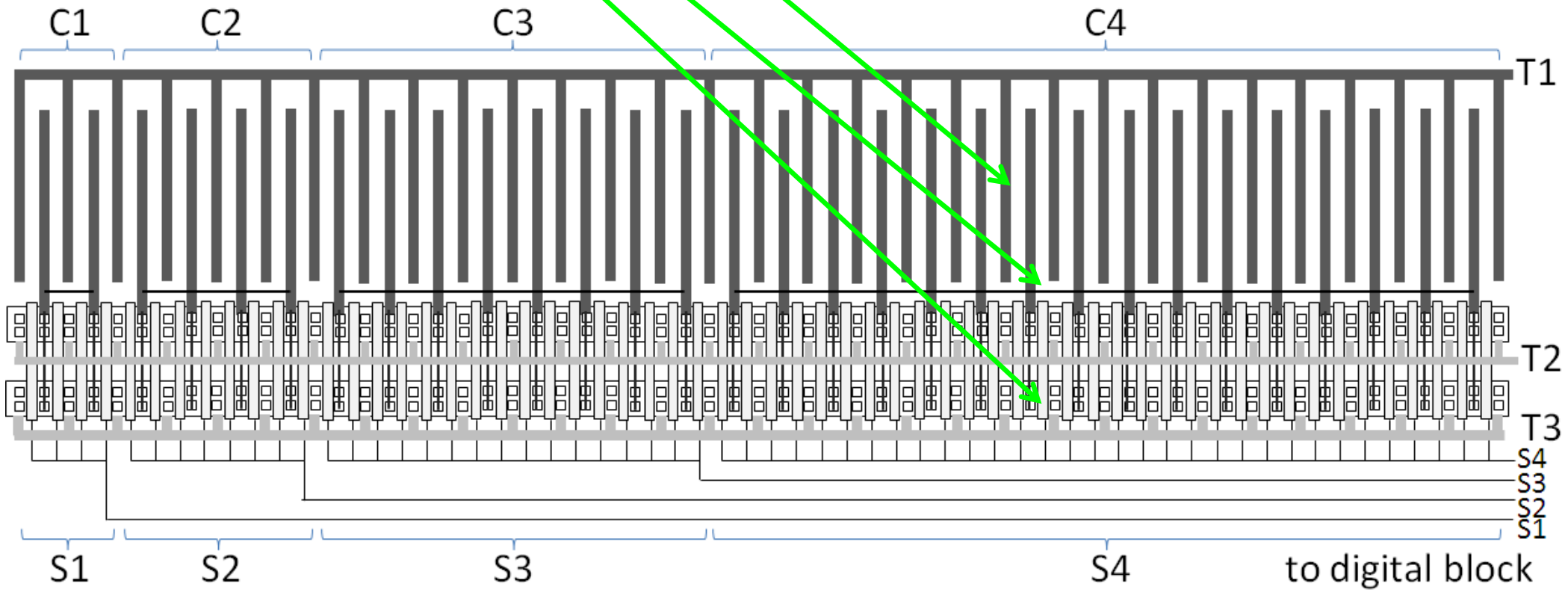
Parasitic capacitance (3.5 fF)
Between top prate and bottom plates
Causes large conversion error of 50 LSB (12 bit).

Regular layout driven design

TOKYO TECH Pursuing Excellence



Avoid wires between components
Wire itself is the component
Respect the regularity
Pitch should be aligned

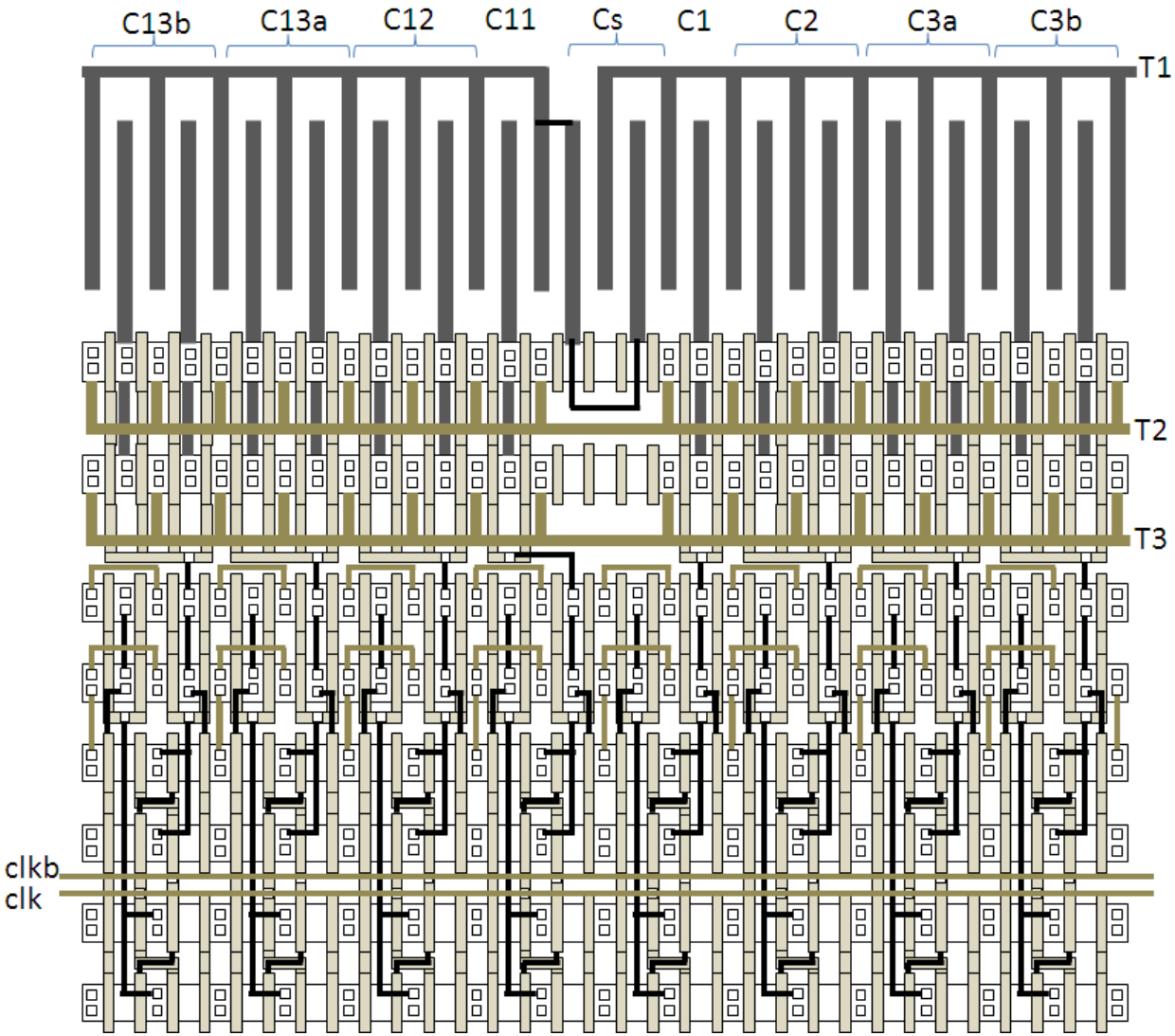


菅原，松澤　他，アナログRF　研究会，2013年11月

Ideal layout design

TOKYO TECH Pursuing Excellence

Pitch is aligned.
It minimizes parasitic component , wire length, delay and capacitance.
Low power, high speed, small area, and high robustness can be realized.



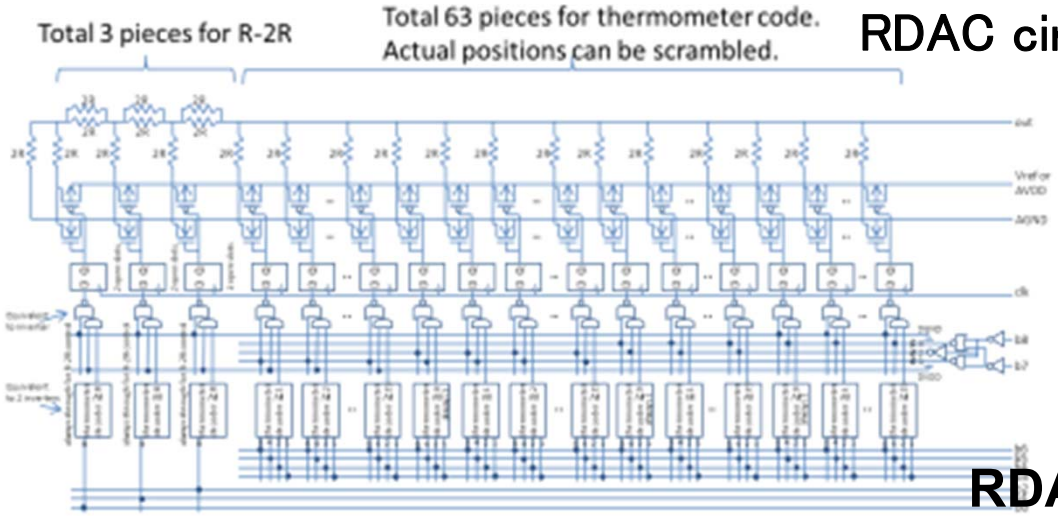
SAR ADC

菅原，松澤　他，
アナログRF　研究会
2013年11月

Automated layout

TOKYO TECH Pursuing Excellence

We can compose analog layout automatically with SKILL language

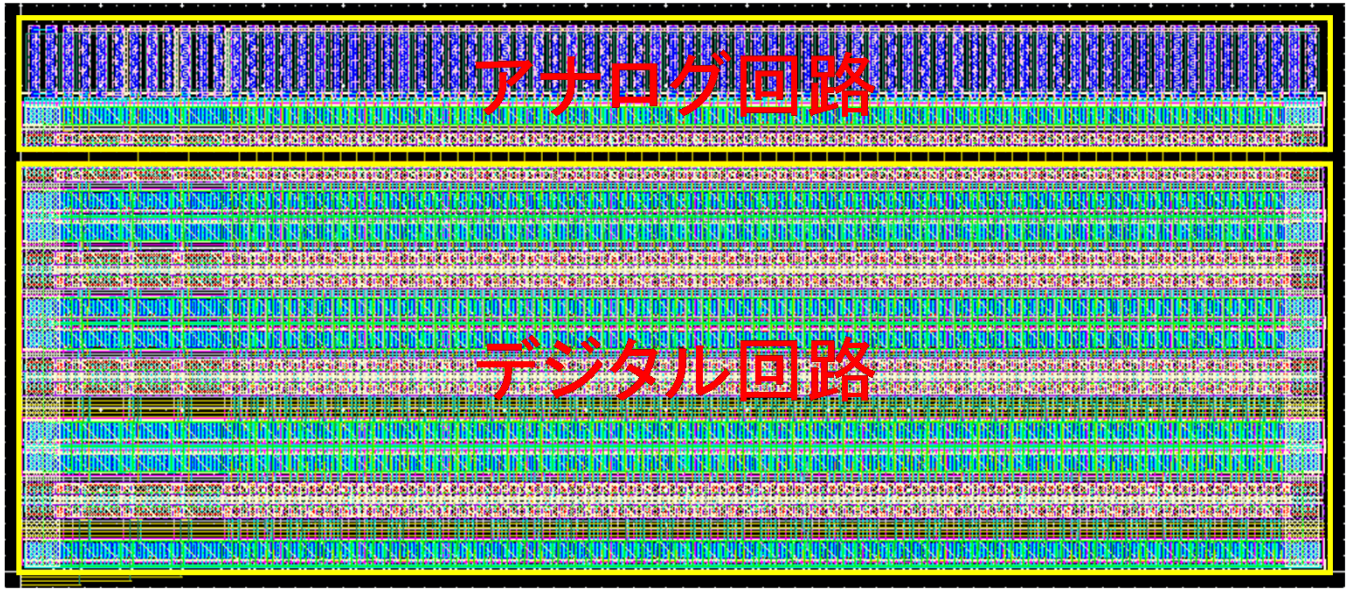


RDAC circuit

盛，松澤　他，”9ビットRDACの自動合成”
アナログRF　研究会，2013年8月

Automated optimization
Automated layout with SKILL language

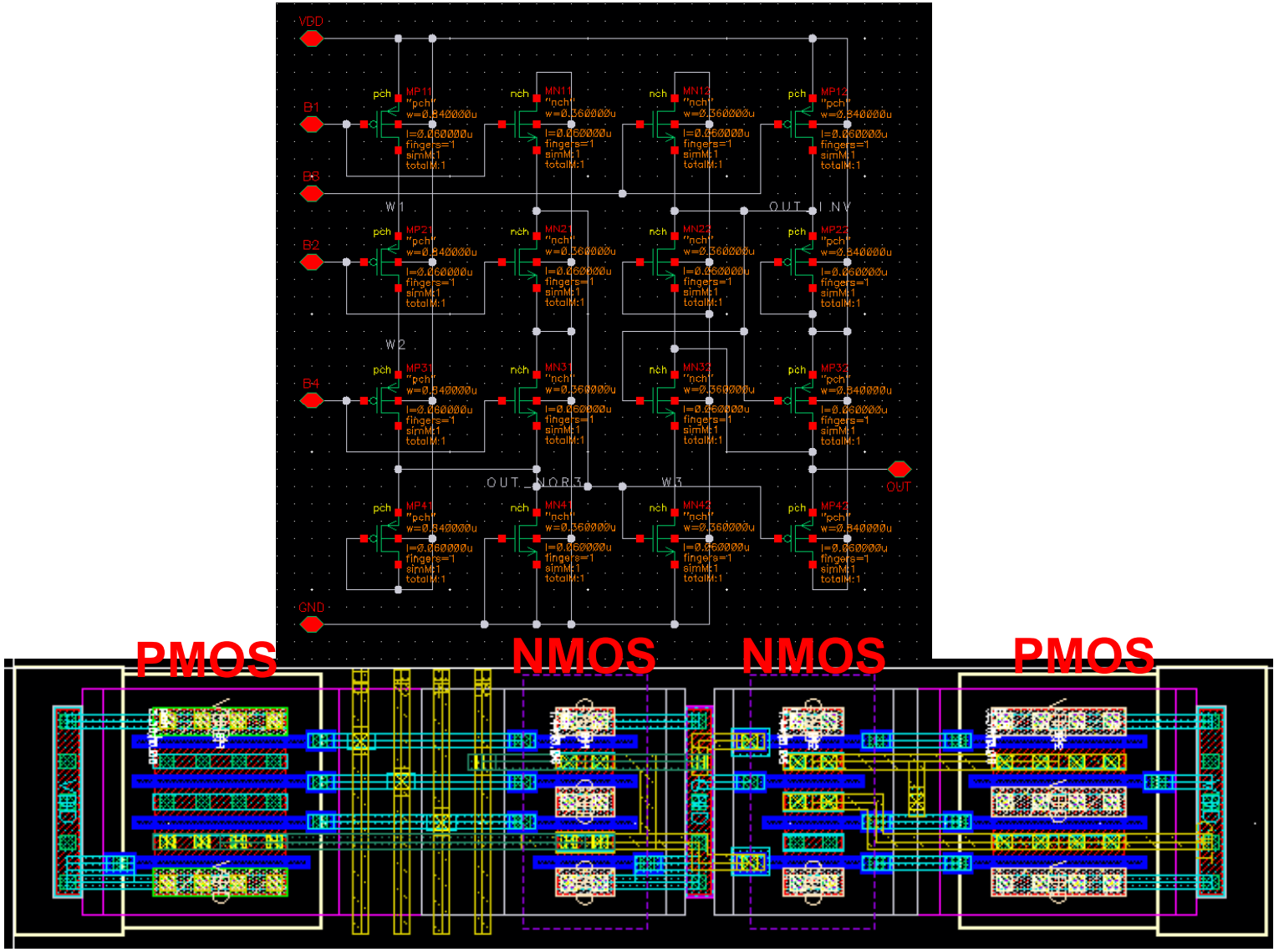
RDAC layout composed by skill language



Circuit schematic and layout（LOGICpn01）

TOKYO TECH Pursuing Excellence

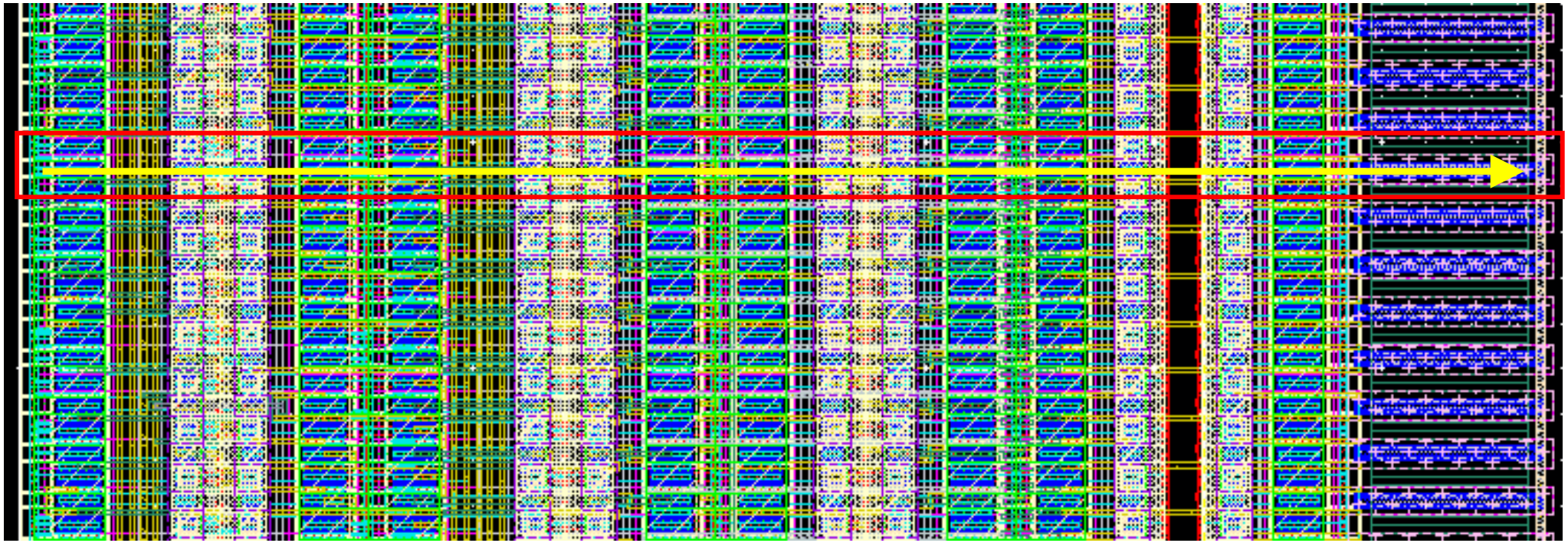
Logic gates should have regularity and launch the automated layout.



Align the layout pitch

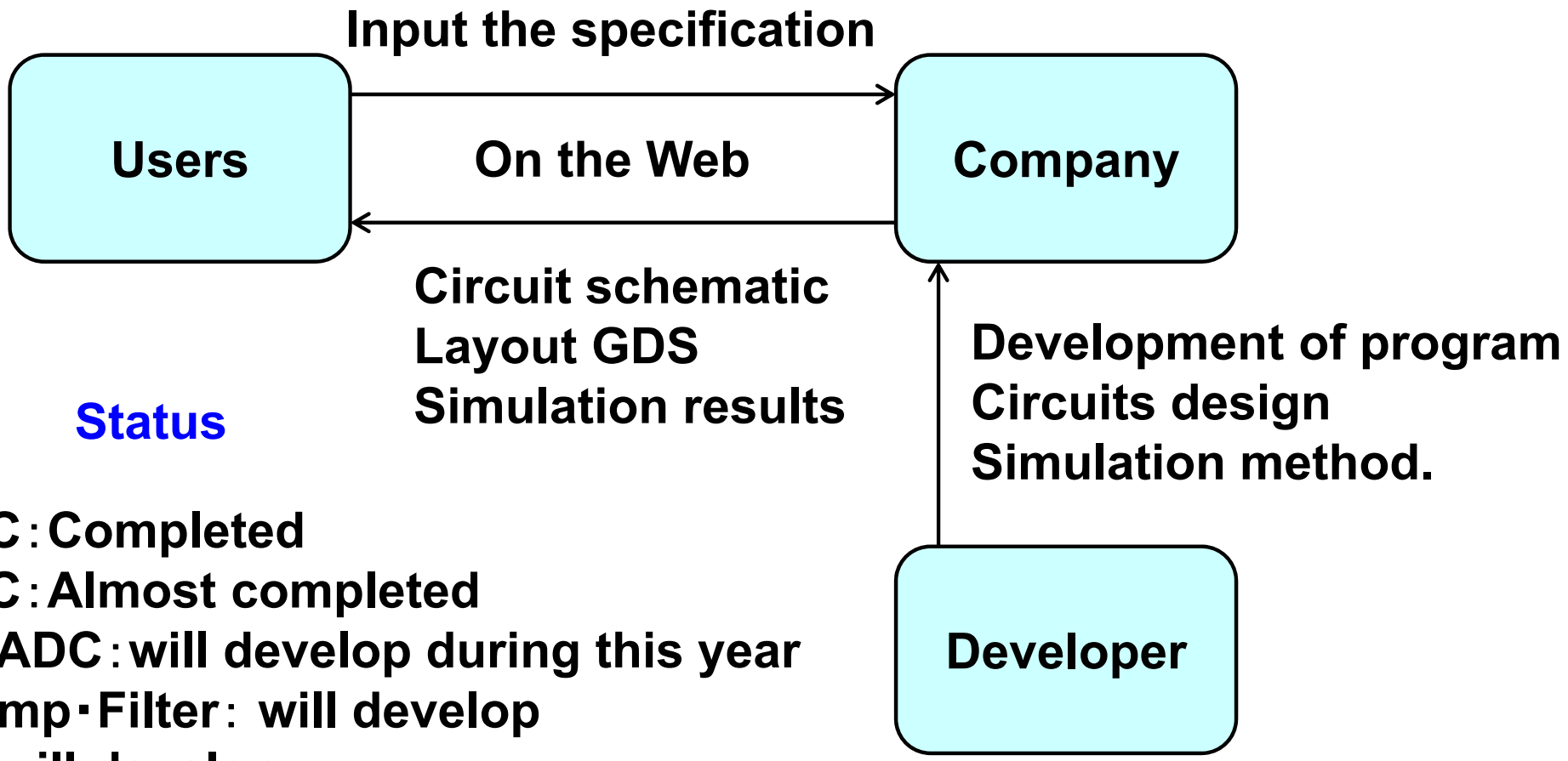
TOKYO TECH
Pursuing Excellence

Logic gates, DFFs, switches, and resistors are aligned



Future of analog circuits design

Circuit should be composed automatically.
Developers develop the technology itself.



Status

RDAC：Completed
CDAC：Almost completed
SAR ADC：will develop during this year
OP Amp・Filter： will develop
PLL：will develop

Summary

TOKYO TECH Pursuing Excellence

- We have realized the world's first 64QAM and attained the world's fastest 28Gbps.
  - Not only increase BW but also increase SNDR
  - MIMO is the next step
- Developed 12b SAR ADC can cover almost all the performance area for wireless communication with the lowest power.
  - Dynamic capacitance and comparator
  - MOM capacitance
  - Over sampling, Dither, and DEM
- 7bit 2.2 GHz ADC with time-domain signal processing
  - Time-domain processing can realize folding and interpolation with simple logic gates. Suitable for low voltage operation
- PLL will be progressed and finally use digital techniques
  - Injection locking method
  - Full digital PLL using fine TDC
- Regular layout driven automated design will be developed.