Lessons and Challenges for Future Mixed-Signal, RF, and Memory Circuits

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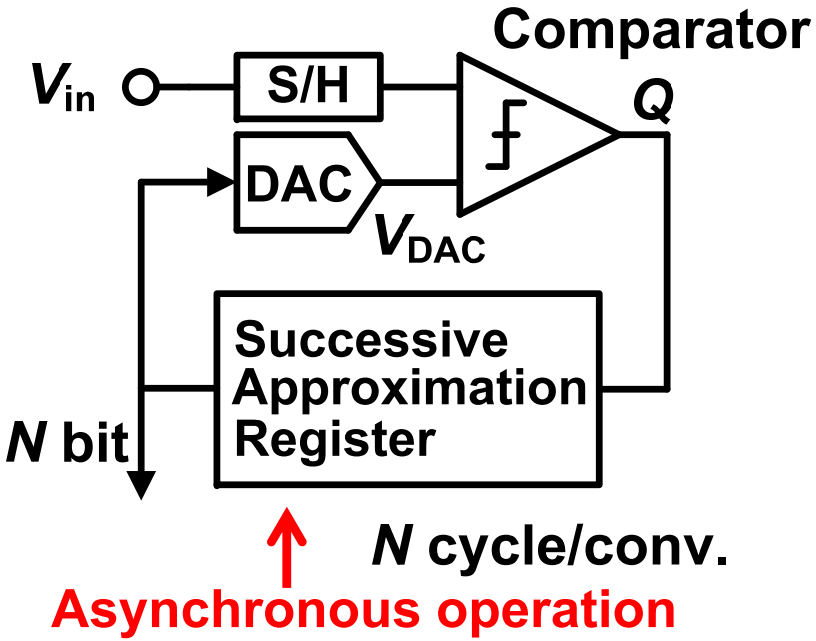
Can we verify the analog circuits perfectly by circuit simulator?

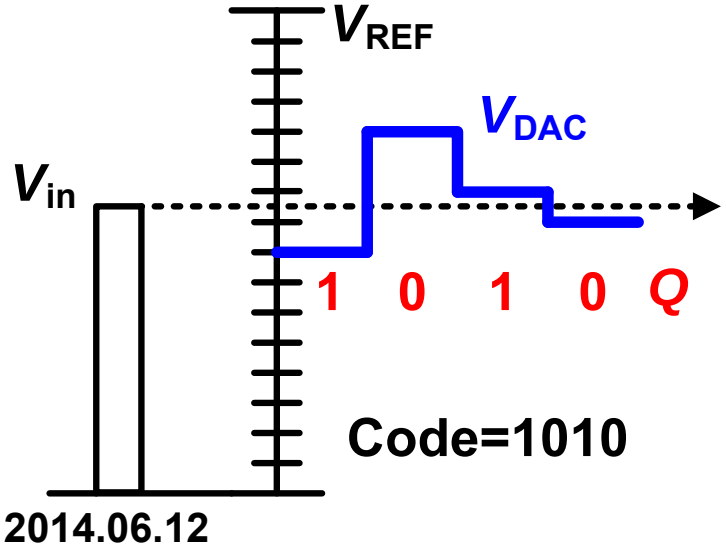
Pitfalls of Analog IC Design

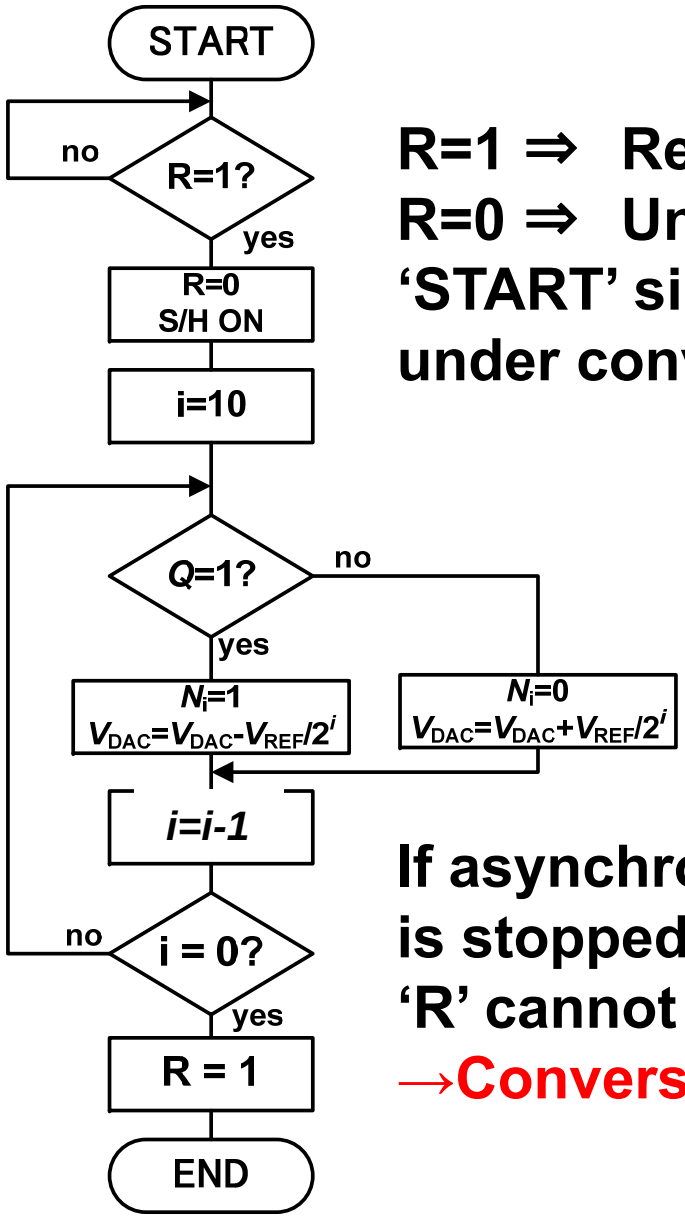
- Bugs of system level design
- Lack of well device models
- Wrong circuit simulation
- Effects of parasitic components
  - Not only in IC but also external components (package, PCB, etc.)
- Influences of EM fields

Ex.1 Hung-up: wrong system level design

50MS/s SAR ADC suddenly stopped after 1 hour from power-on .
Error rate: 10^{-11} ← Can we simulate?





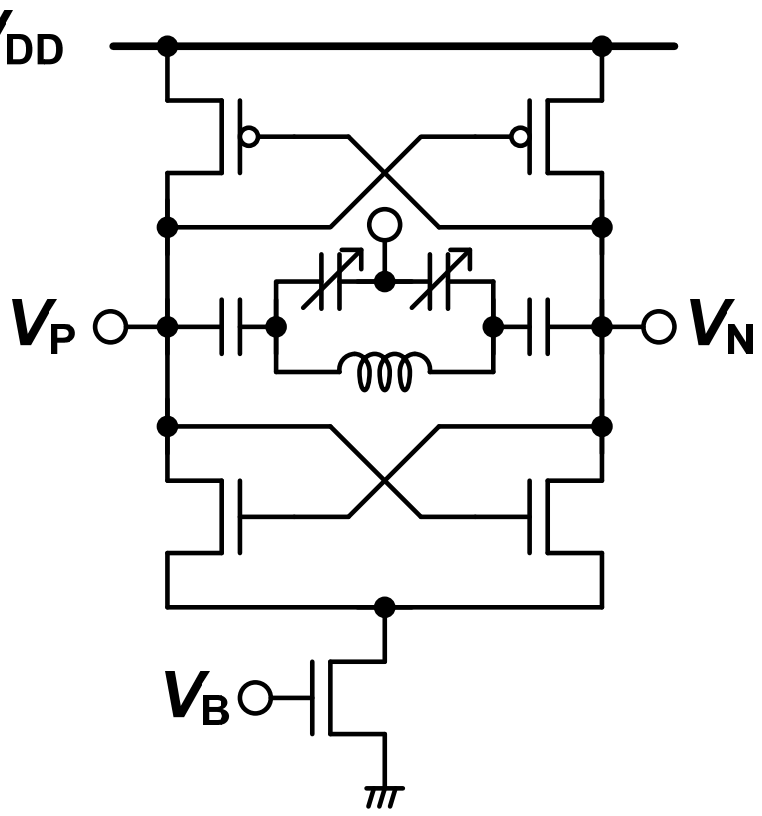


R=1 ⇒ Ready
R=0 ⇒ Under Conversion
'START' signal is ignored under conversion.

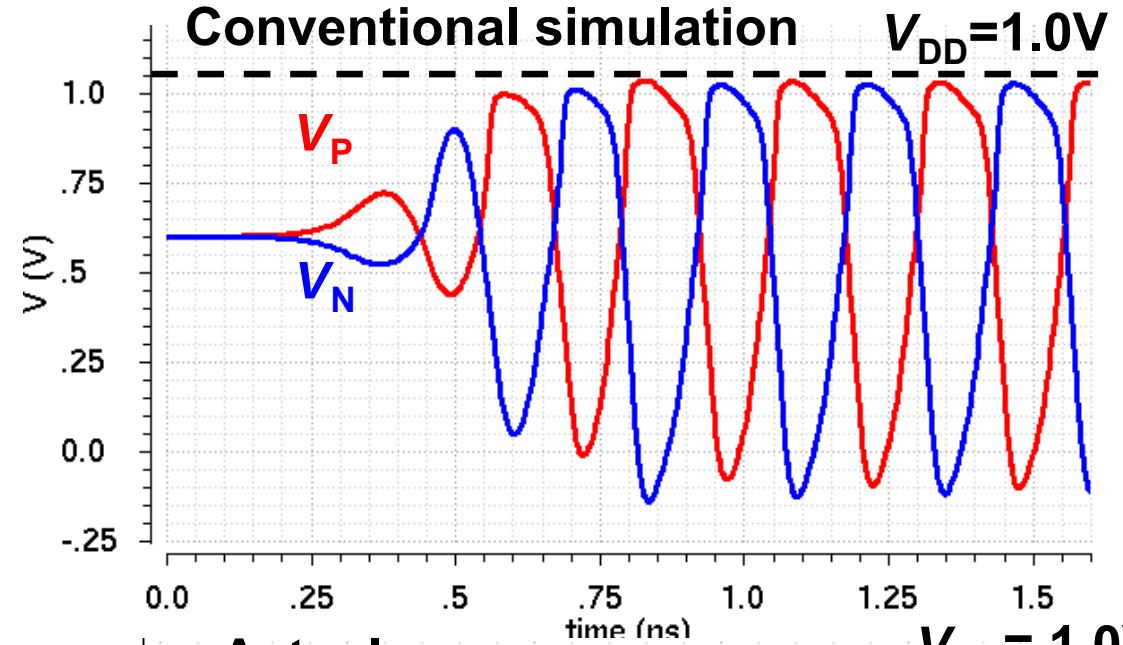
If asynchronous operation is stopped,
'R' cannot be '1' .
→Conversion is stopped.

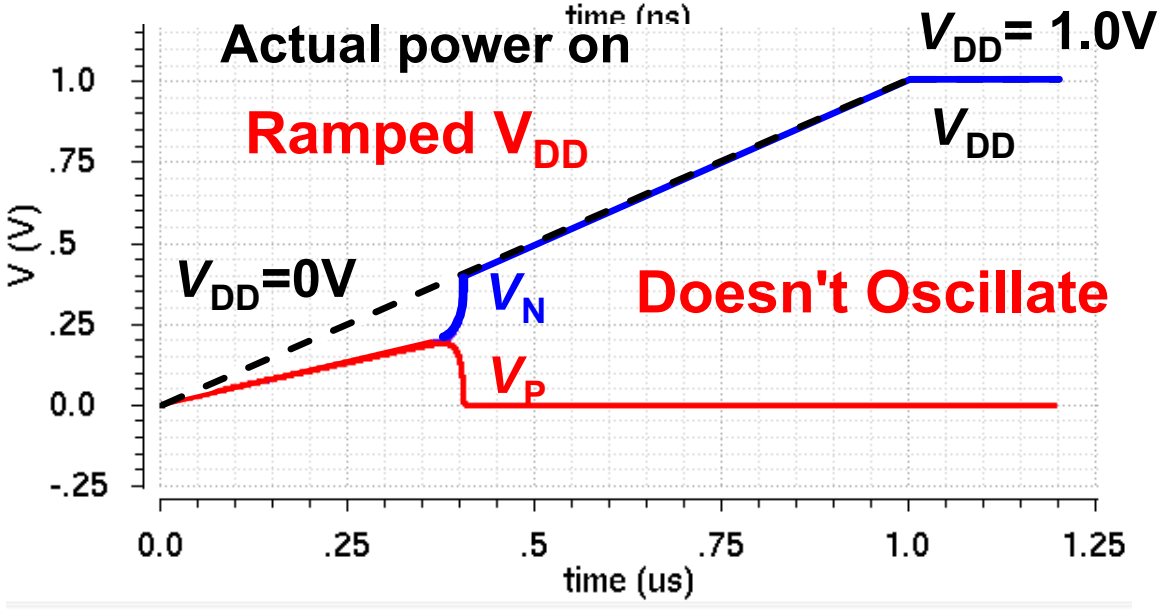
Ex.2 Wrong circuit simulation

Sometimes circuits have two steady-states.
Designers have to set a initial condition carefully.



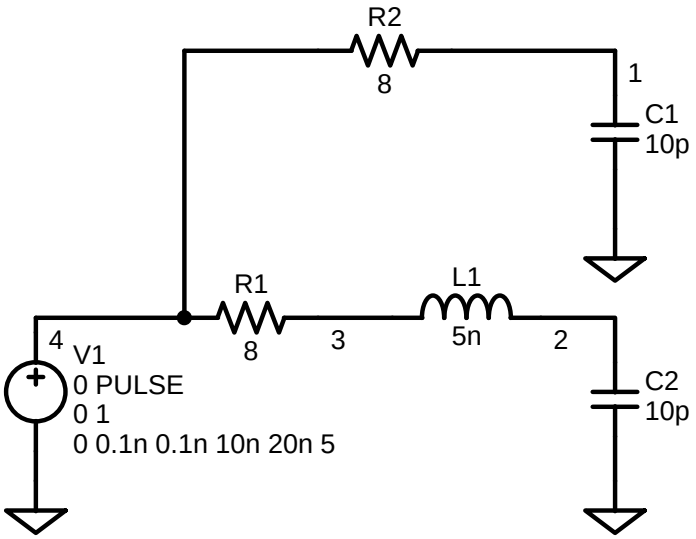
CMOS oscillator with DC-cut LC tank

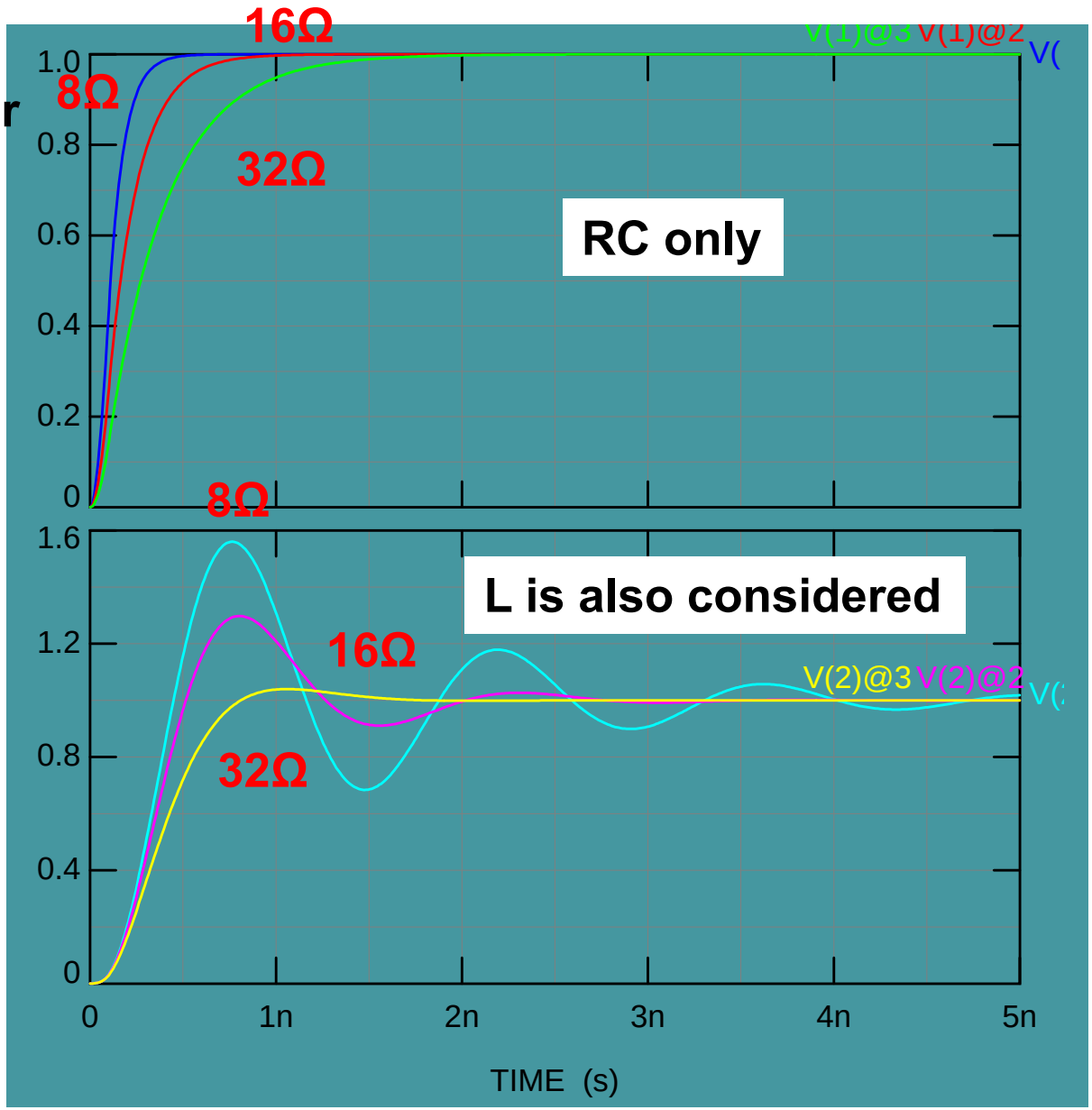




Ex.3 Different result: Effect of inductance

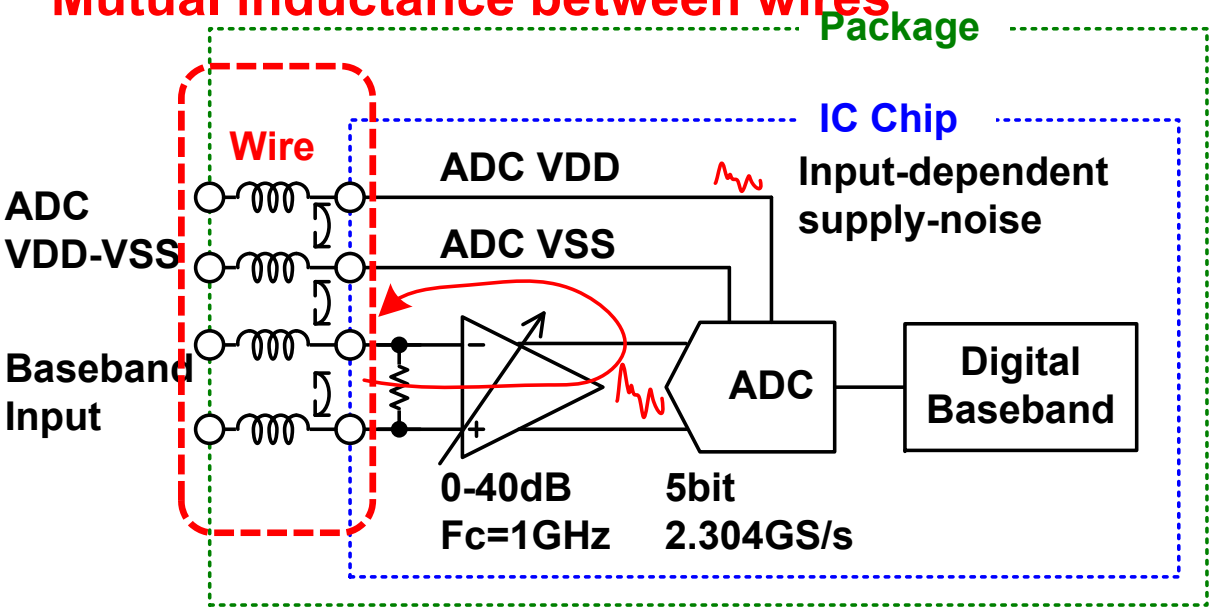
If inductance is neglected,
The smaller resistance is the better for fast settling.
However, actual circuit contains Inductive component; wires.
If it is considered,
Smaller resistance makes large Ringing. The optimum resistance exists.



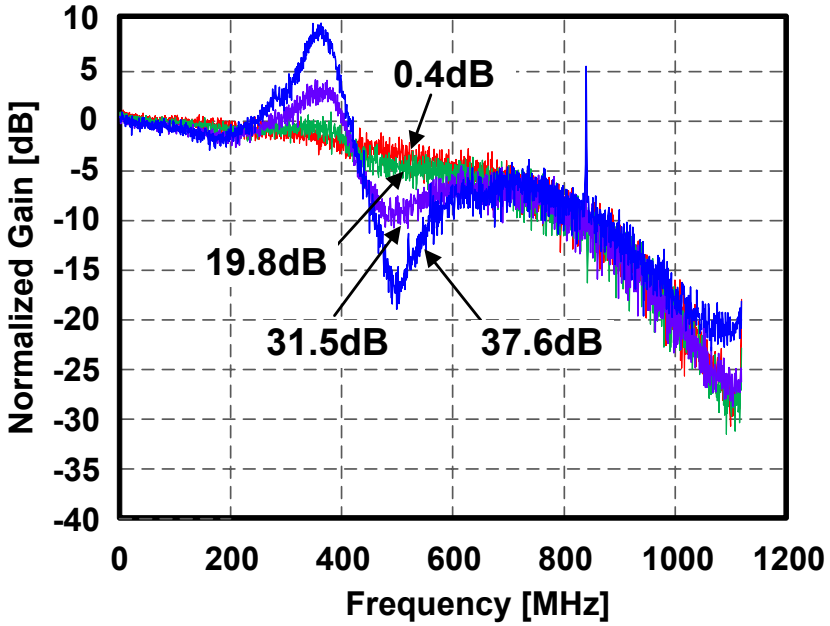


Ex.4 Parasitic components

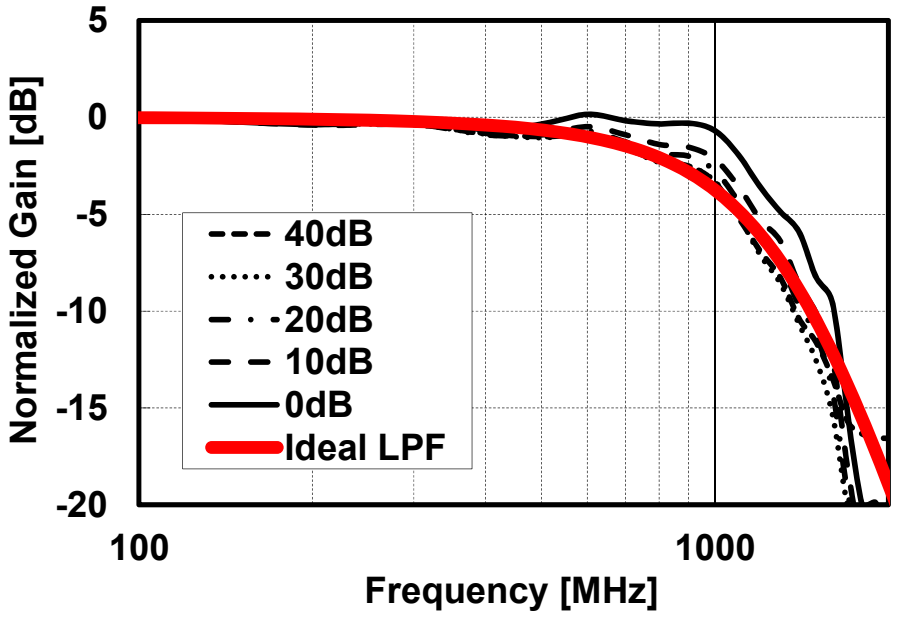
Mutual inductance between wires



Mutual inductance of package wire often forms feedback loop resulting in oscillation.



Wire coupling effect

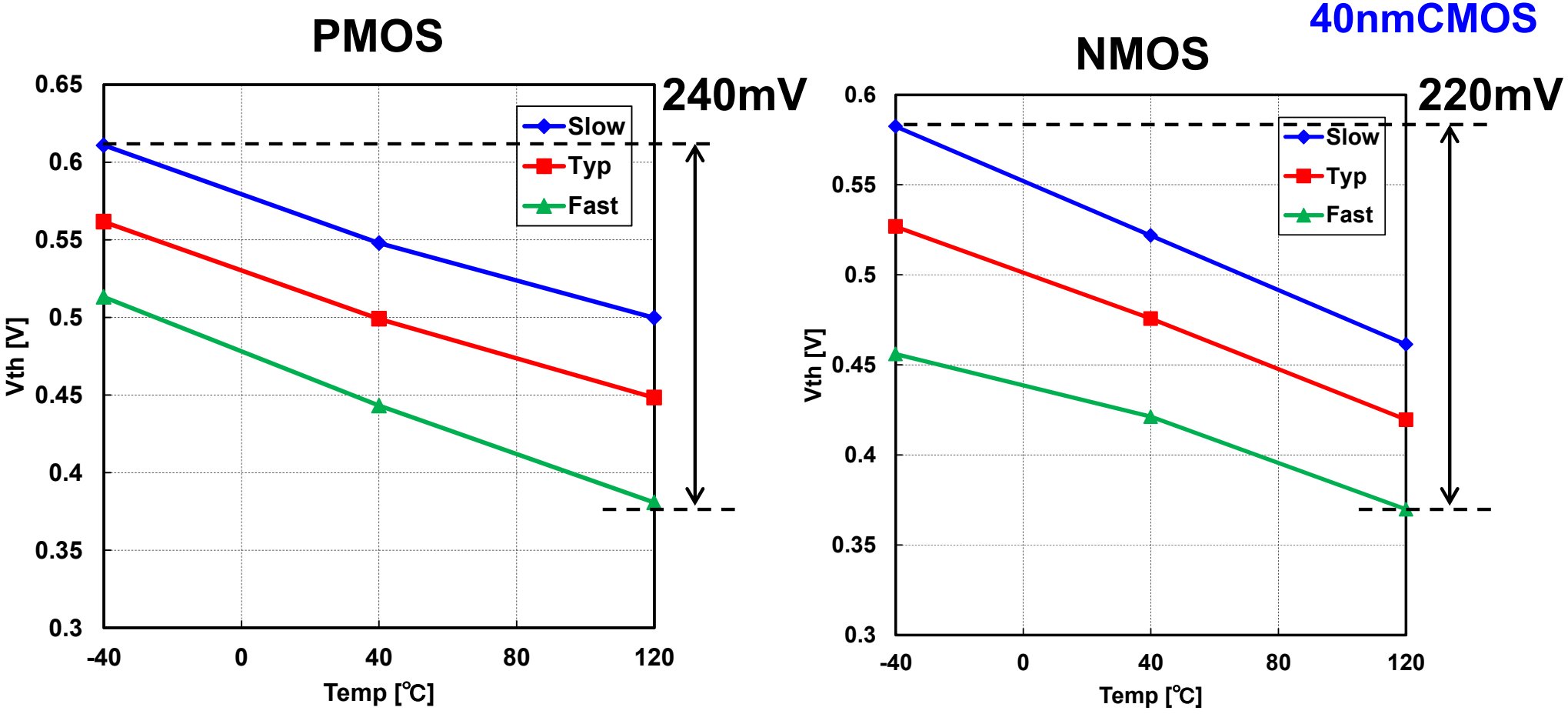


Revised version

Small design margin: VT of transistor

VT of 40nm CMOS transistor is quite high of 0.6V. (V_{GS}=0.8V)
PVT variation is 220-240mW.
Therefore it is quite difficult to realize 1V operation with 40nm CMOS.

40nmCMOS



Reality of analog& mixed signal LSI

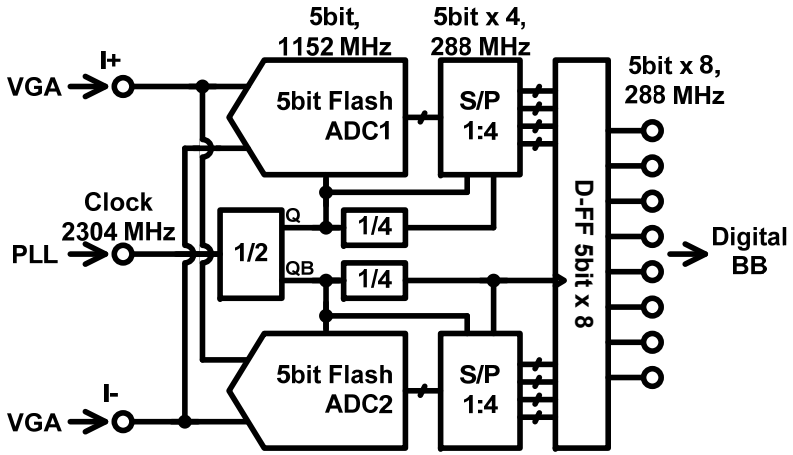
- **Circuit design**
  - **Almost no margin for low voltage design.**
  - **Can’t simulate every performance with every condition.**
  - **Calibration technique is needed, however it can’t guarantee the optimum performance.**
- **Layout design**
  - **Analog performance is strongly affected by layout design.**
  - **Package and board design affects the performance.**
  - **Not acceptable time for LPE simulation.**
- **Testing and embedding**
  - **No testing method for perfect verification.**
  - **Strongly affected by package or probe.**
  - **Affected by embedding to Mixed signal LSI.**

Development procedure of M/S SoC

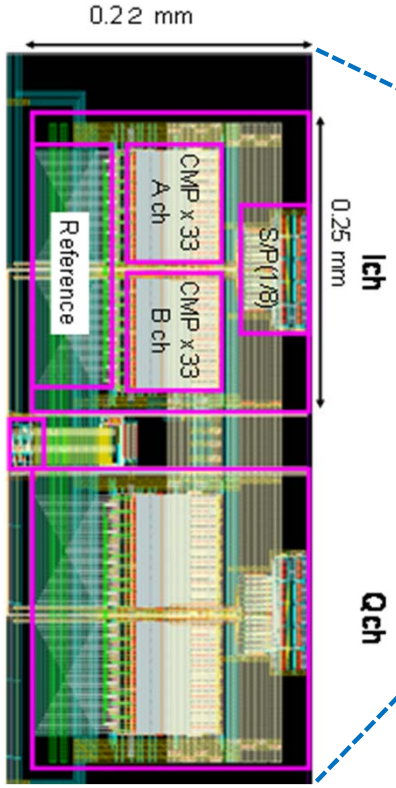
TEG test and rework are necessary before embedding to the M/S SoC.

Circuit design

Layout design



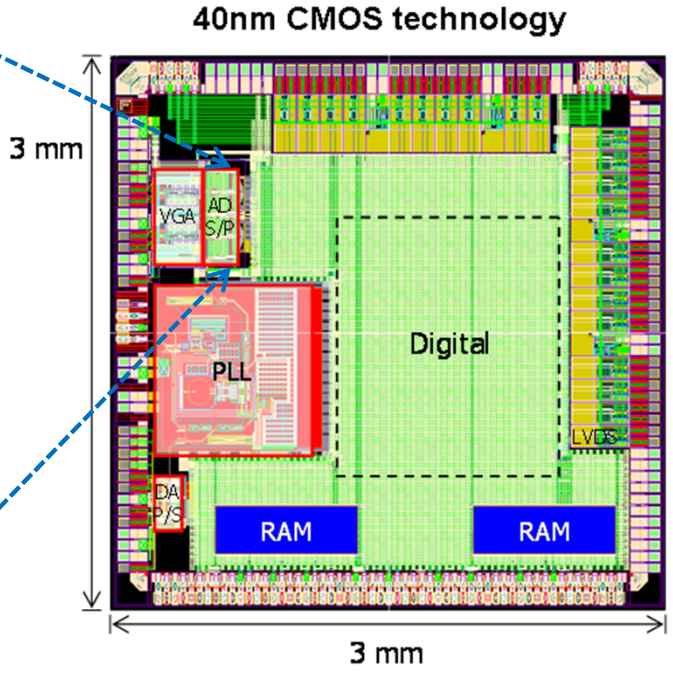
TEG Test & Rework



5b, 2.3GSps ADC

Simulation with package

Embeding to the SoC



BB SoC for 60GHz CMOS Transceiver