Potential and limitation of RF CMOS Technology and expectation for new passive devices

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Current status of RF CMOS chip

RF CMOS was an university research theme, however currently becomes major technologies in the wireless world.

- **Current products**
  - **Bluetooth: 2.4GHz, CSR etc., major**
  - **Wireless LAN: 5GHz, Atheros etc., major**
  - **CDMA : 0.9GHz-1.9GHz, Qualcomm, becomes major**
  - **Zigbee: 2.4GHz, not yet, however must use CMOS**
  - **TAG: 2.4GHz, Hitachi etc., major**

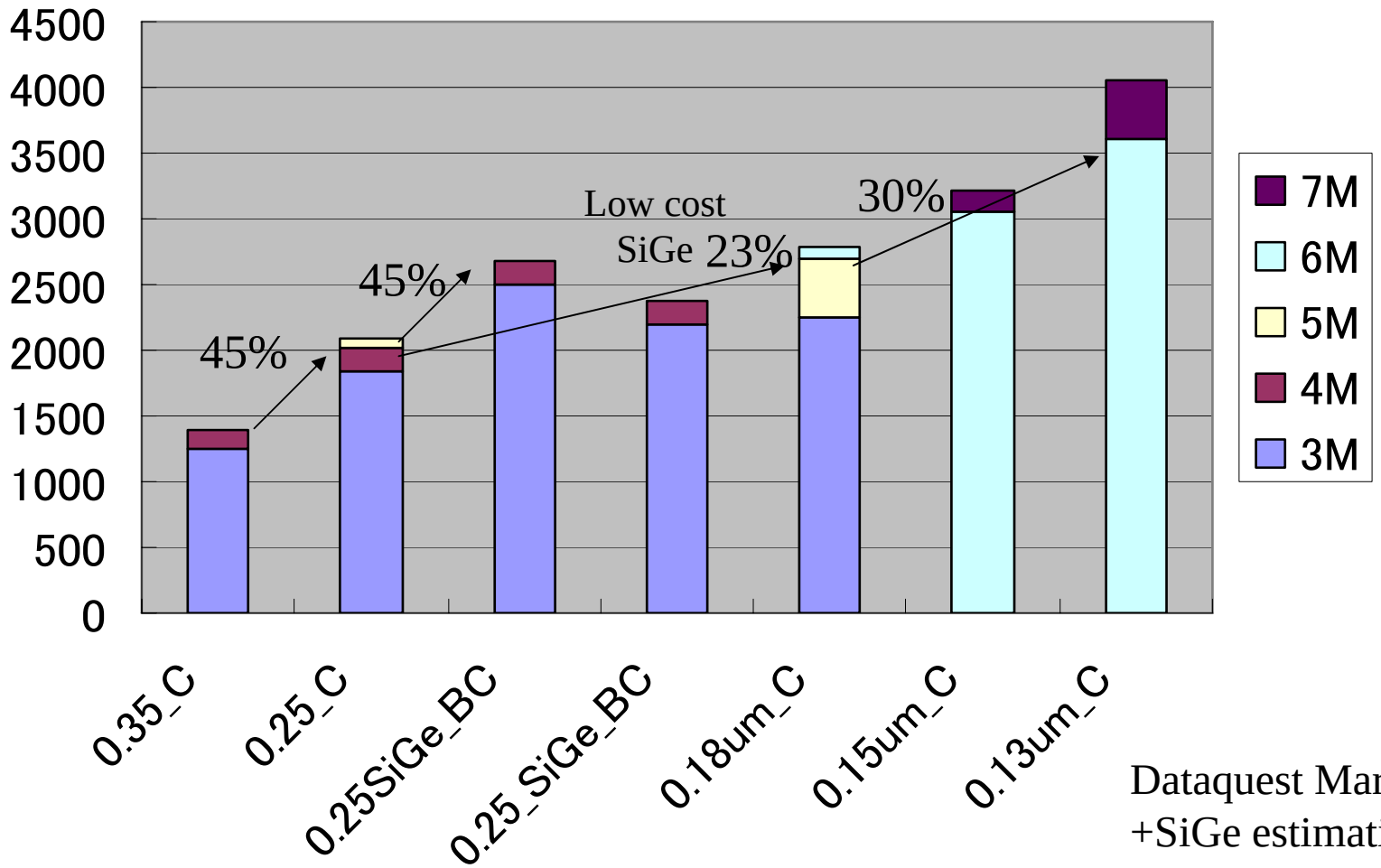
Major Cellular phone standard, GSM uses SiGe-BiCMOS technology

Why CMOS?

- **Low cost**
  - **Must be biggest motivation**
  - **CMOS is 30-40% lower than Bi-CMOS**
- **High level system integration**
  - **CMOS is one or two generations advanced**
  - **CMOS can realize a full system integration**
- **Stable supply and multi-foundries**
  - **Fabs for SiGe-BiCMOS are very limited.**
    → Slow price decrease and limited product capability
- **Easy to use**
  - **Universities and start-up companies can use CMOS with low usage fee, but SiGe is difficult to use such programs.**

Wafer cost example

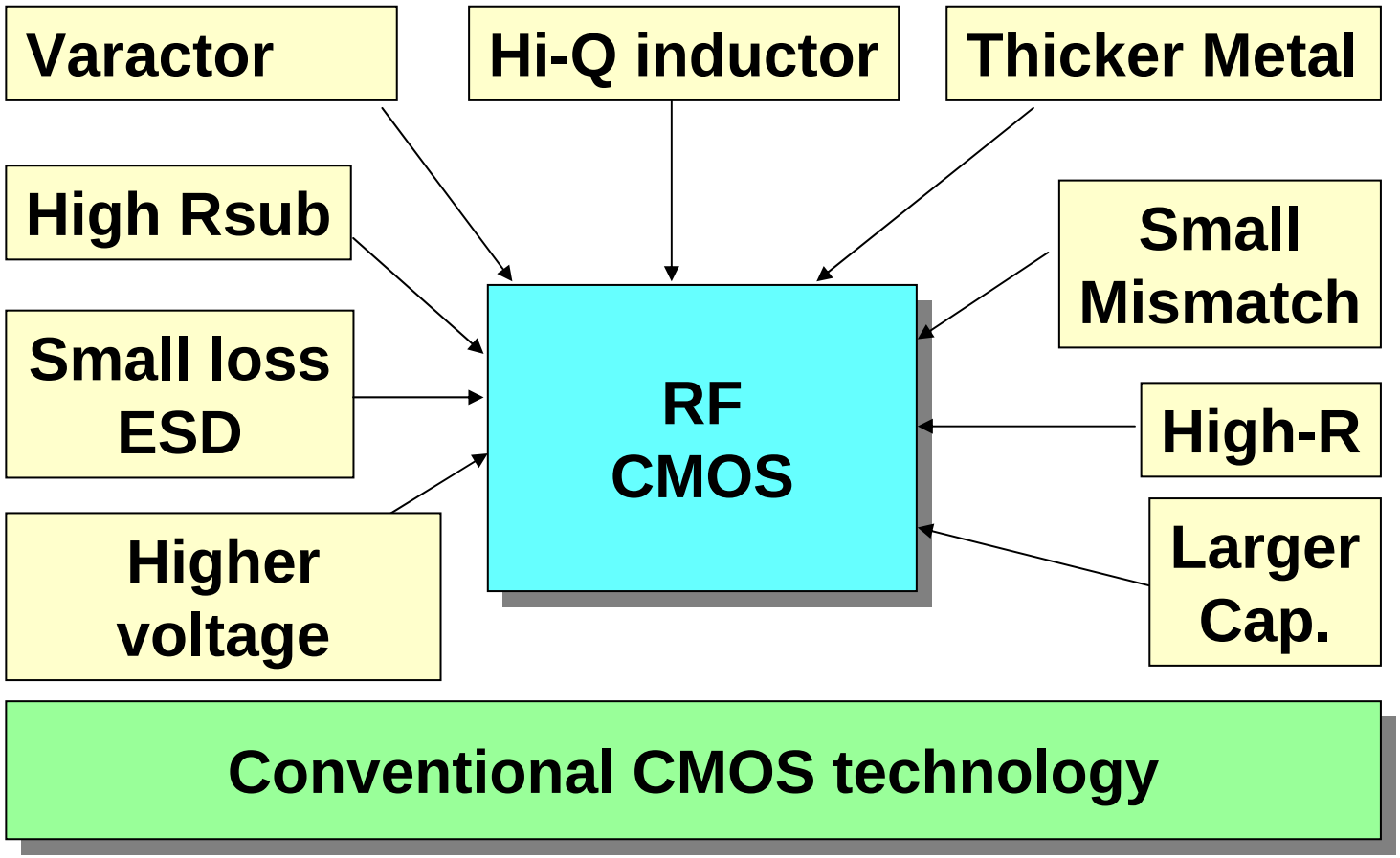
The wafer cost of SiGe BiCMOS is 30-40% higher than CMOS at the same generation, however almost same as one generation advanced CMOS.



Dataquest March 2001
+SiGe estimation

RF CMOS device technology

RF CMOS needs some process options,
however significant cost increase can't be accepted.



MOS vs SiGe-Bip

	MOS		SiGe-Bip
Gm	$\frac{Ids}{\left(\frac{V_{eff}}{2}\right)} \approx \frac{Ids}{100mV}$	4x ⇒	$\frac{Ids}{U_T} \approx \frac{Ids}{26mV}$
f_{Tpeak}	$\approx \frac{1}{W_b{}^2}$	Almost same ⇔	$\propto \frac{v_{sat}}{L_g}$
F_{min}	$\approx 1+2\sqrt{\frac{2Gp}{gm}+0.7\left(\frac{f}{f_T}\right)^2}$	Lower and low Id ⇒ (larger gm)	$\approx 1+2\sqrt{\frac{Gp}{2gm}+0.25\left(\frac{f}{f_T}\right)^2}$
V*fT	100VGHz	2x ⇒	200VGHz

MOS vs SiGe-Bip

	MOS		SiGe-Bip
Rg,Rb		Same ⟷	
1/f noise		Much better →	
Mismatch	$mV \approx \frac{Tox(nm)}{\sqrt{LW}\ (um)}$	Better →	
Cost		←	(SiGe-BiCMOS)

Low gm or larger current
Voltage lowering
Geometry dependence

High gm or smaller current
Low noise and mismatch
Less geometry dependence

Low performance and low cost?

High performance and high cost?

Feature of CMOS technology

- **Pros**
  - **Can use a switch and a voltage controlled conductance**
  - **Smaller distortion**
  - **No carrier accumulation**
  - **Can use switched capacitor circuits**
  - **Can increase f_T by scaling**
  - **Easy use of complementally circuits**
  - **Easy integration with digital circuits**
- **Cons**
  - **Low gm/Ids**
  - **Larger mismatch voltage and 1/f noise**
  - **Lower operating voltage with scaling**
  - **Difficult to enable impedance matching**
  - **Easily affected by substrate**

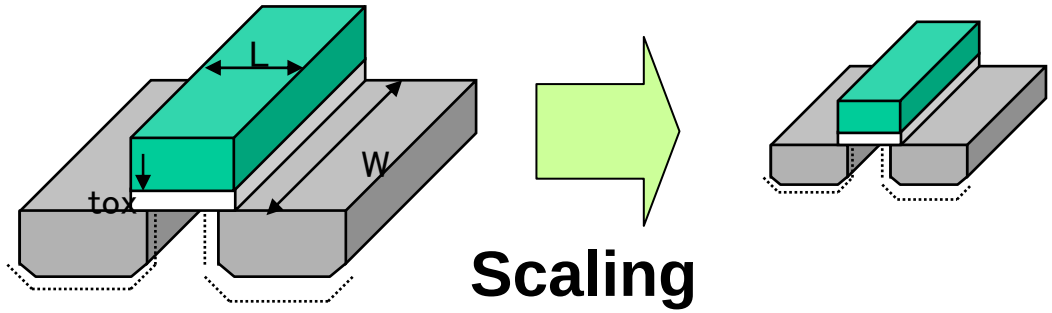
Principal design for RF CMOS

- **Use small size devices and compensate the accuracy and 1/f noise degradation.**
  - **Small parasitic capacitance is imperative.**
    - **Smaller capacitance is needed to keep higher cutoff frequency under the lower gm condition**
  - **Small size results in increase of the mismatch voltage and 1/f noise**
    - **Should be addressed by analog or digital compensation, not by increase of device size.**
- **Keep the voltage swing on ahigh as possible to realize higher SNR**
  - **The noise level is higher and gm is lower than those of bipolar.**
- **Use digital technology rather than analog technology**
  - **Performance increase and power and area decrease are promised by scaling. Analog is not so.**

Scaling Rule: Basic principle of LSI technology

Scaling rule can improve almost all the performances of LSI

Scaling also realizes higher integration and lower LSI cost.



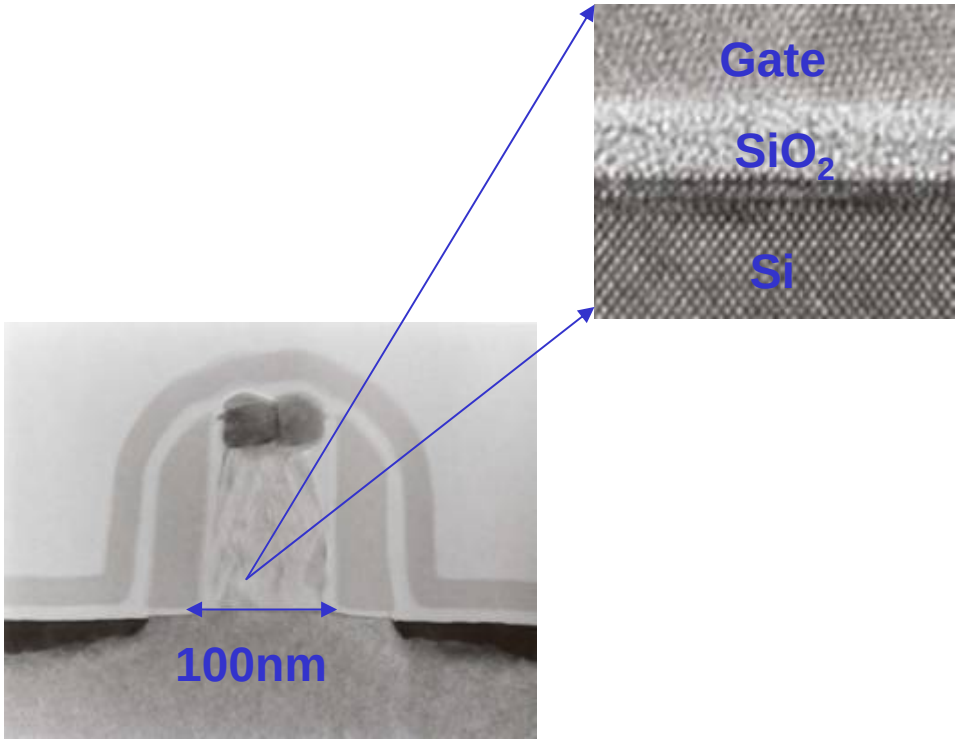
Device/Circuit parameter	Scaling Factor
Device dimensions L, W, Tox	1/S
Doping concentration	S
Voltage	1/S
Field	1
Current	1/S
Gate Delay	1/S
Power dissipation/device	$1/S^2$

$$S \approx \sqrt{2}$$

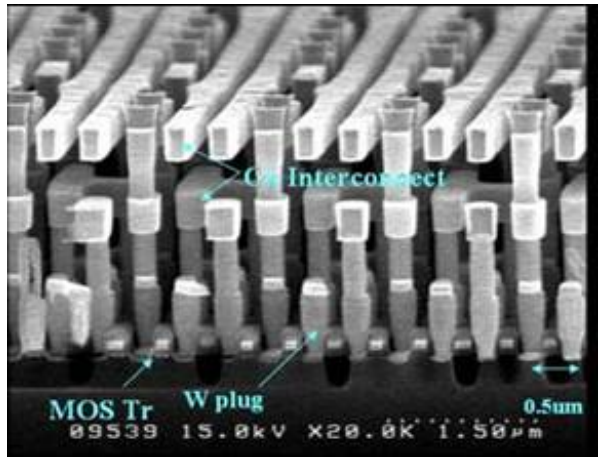
Scaled CMOS technology

Current Scaled CMOS technology is very artistic.

Matsushita's 0.13um CMOS technology



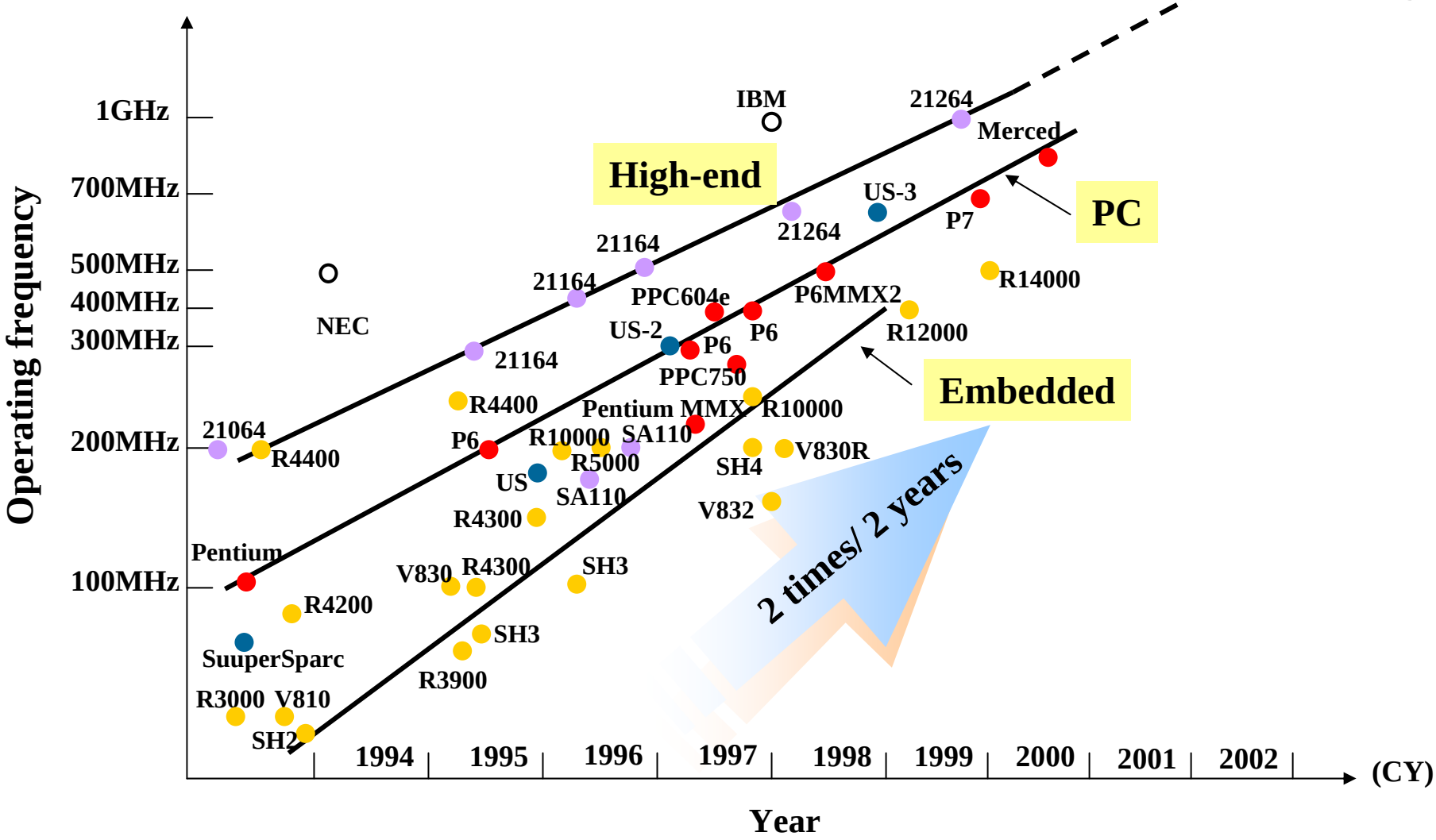
Transistor



Cu Interconnection

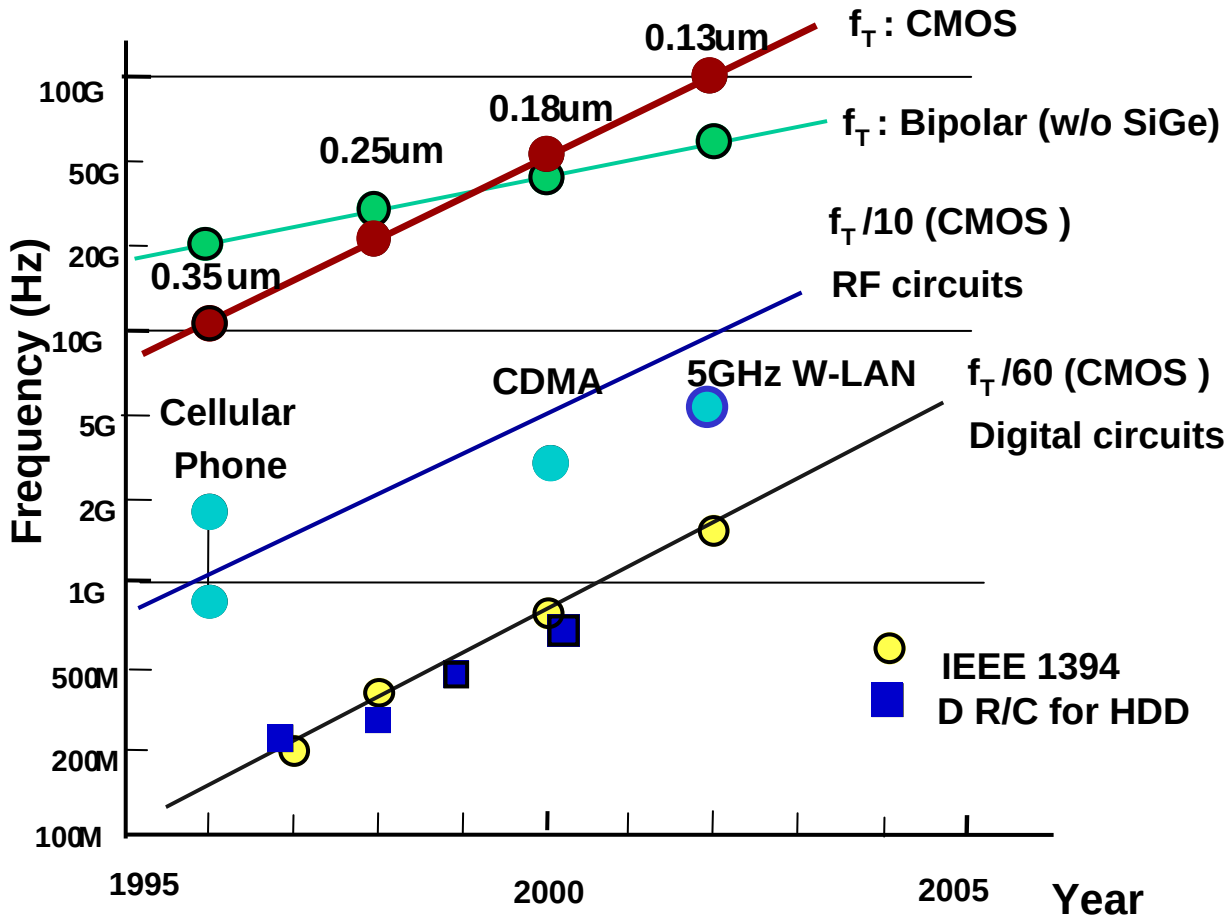
Performance trend of micro-processors

Performance of micro-processors has increased with device scaling.



GHz operation by CMOS

Cutoff frequency of MOS becomes higher along with technology scaling and now attains over 100GHz.

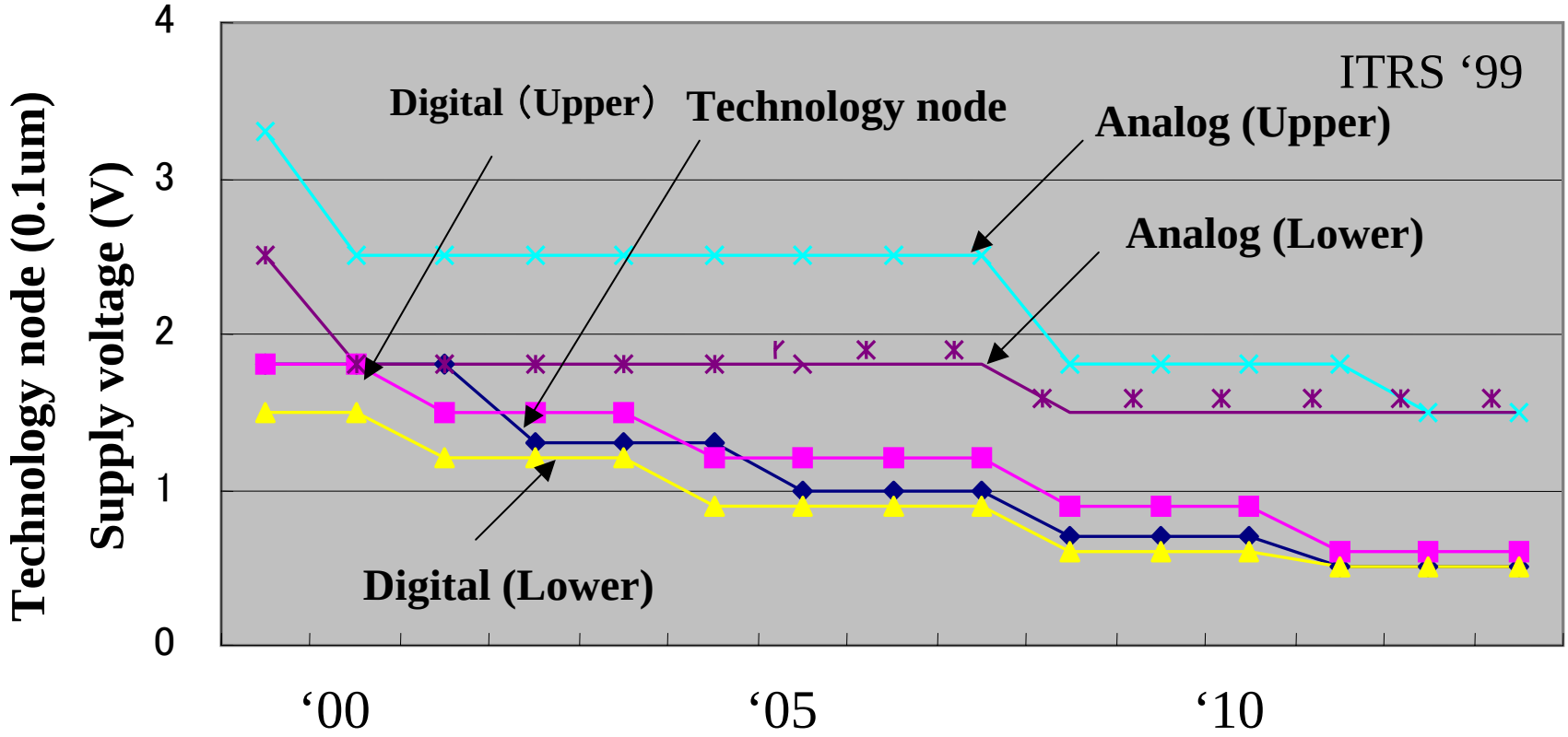


$$f_T \equiv \frac{gm}{2\pi C_{in}}$$

$$f_{Tpeak} \approx \frac{v_{sat}}{2\pi L_{eff}}$$

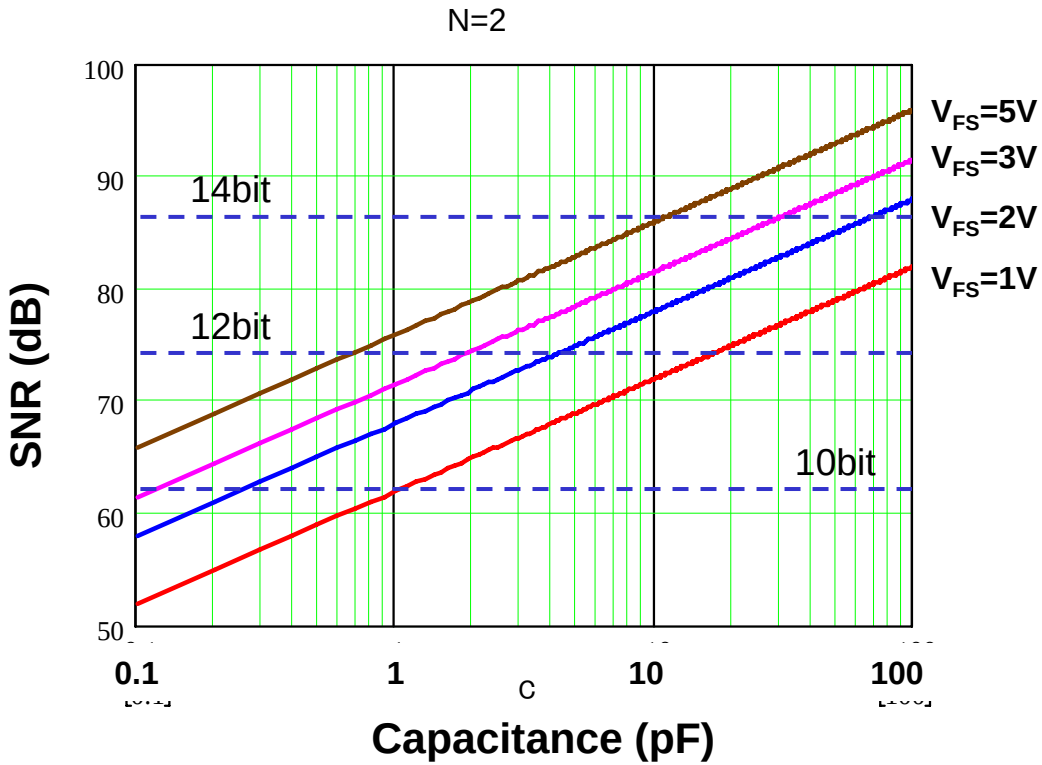
V_{dd} and CMOS scaling limits

Lowest analog operating voltage is 1.2V -1.8V.
Thus 0.18um – 0.13um must be a scaling limit for analog.
50 GHz-100 GHz is an available f_T in CMOS technology.



Difficulty of low voltage analog

Low voltage swing results in low SNR, because noise can't be scaled.



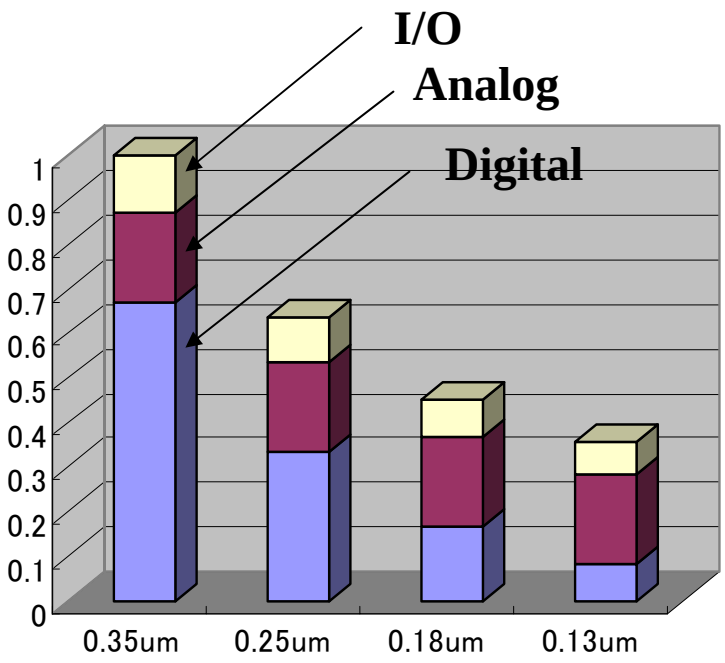
$$V_n^2 = \frac{nkT}{C}$$

$$SNR_{(dB)} = 10\log\left(\frac{CV_{FS}^2}{8nkT}\right)$$

Cost up issue by analog parts

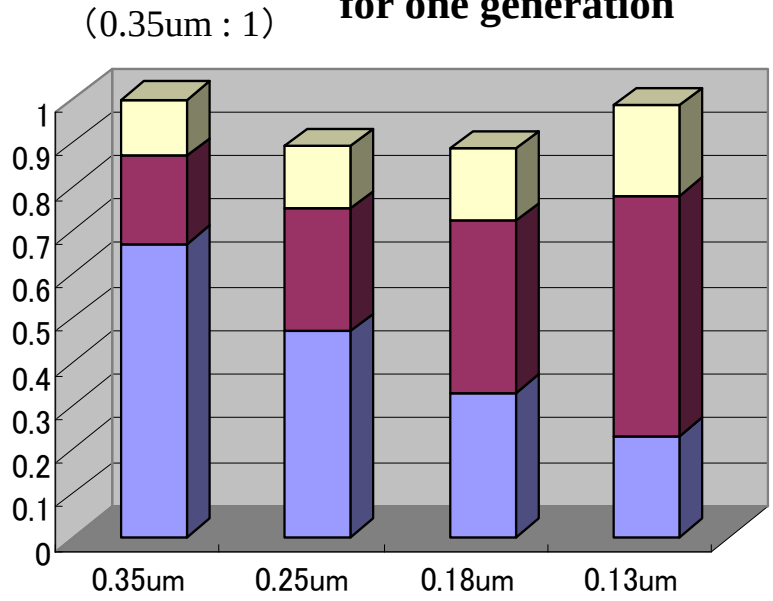
The cost of mixed A/D LSI will increase when using deep sub-micron device, due to the increase of the cost of non-scalable analog parts.

Large analog may be unacceptable.
Some analog circuits should be replaced by digital circuits



Chip area

Wafer cost increases 1.3x for one generation



Chip cost

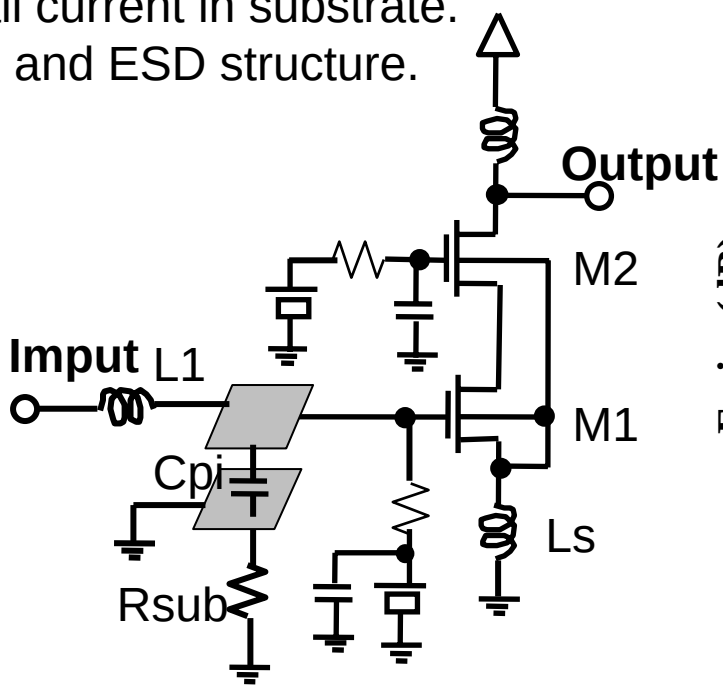
Minimum noise figure: Fmin

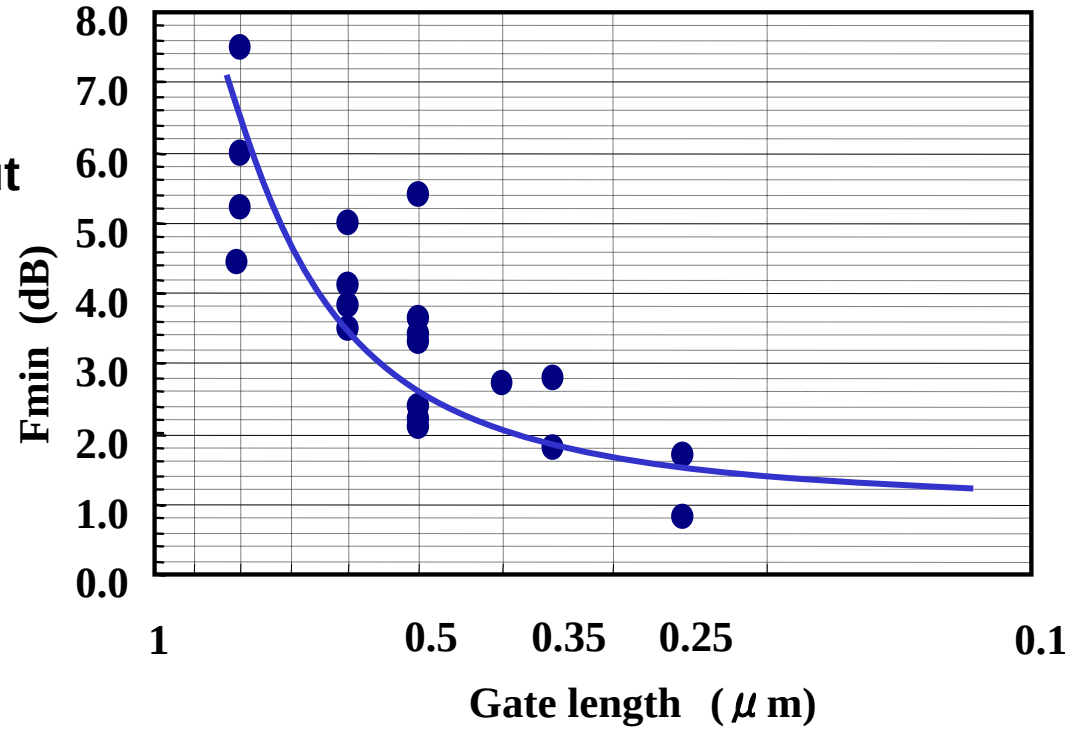
F_{min} has been improved , however saturated at 1dB.

Technical points

$$F_{min} \approx 1 + \frac{\gamma}{\alpha}\left(\frac{f_o}{f_T}\right)^2\left(\frac{2}{\kappa} + gm\ R_{eq}\right) + \frac{\alpha\delta}{\kappa gm\ R_{eq}}$$

High f_T and low gate resistance.
Small current in substrate.
PAD and ESD structure.



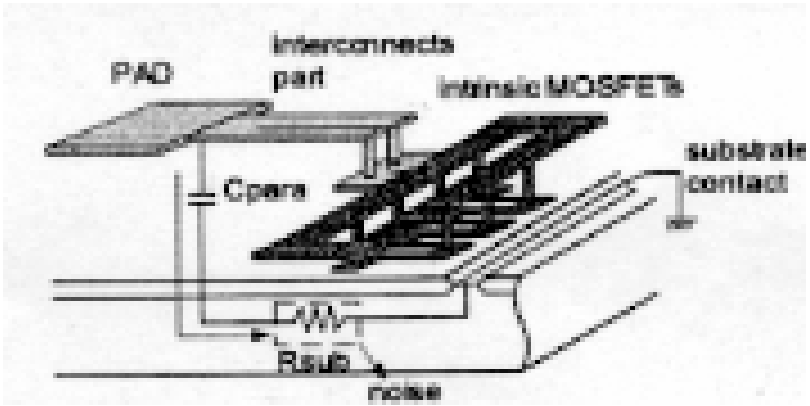


Substrate effect on NF in MOS

NF in MOS is very low at on a chip measurement,
But becomes very large when packaged!

NFmin@5GHz, 0.18um

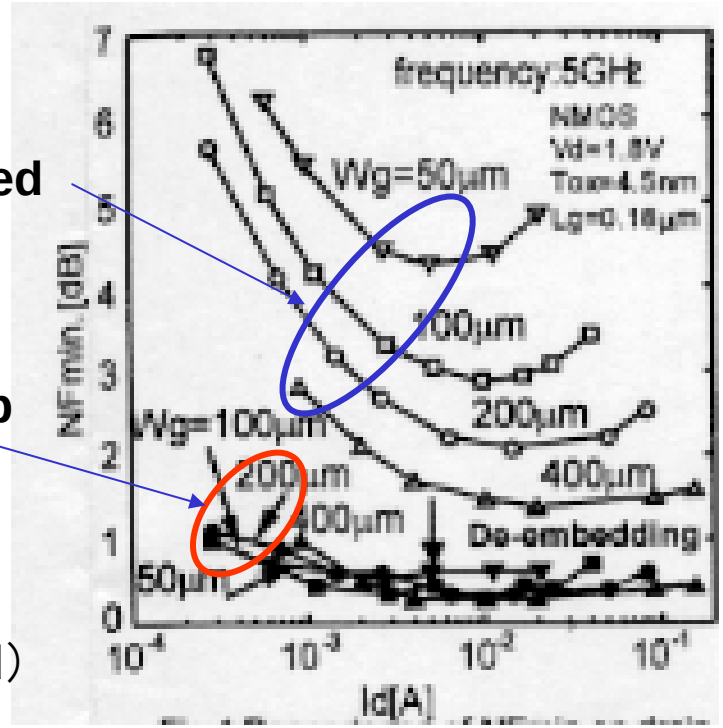
This is due to the substrate RF power loss



MOS

Packaged

On chip



（Substrate loss shall be added, when packaged）

- Packaged : NF_{min}=1.6dB
- On chip : NF_{min}=0.4dB

E.Morifuji, et al., SSDM98 pp.80-81

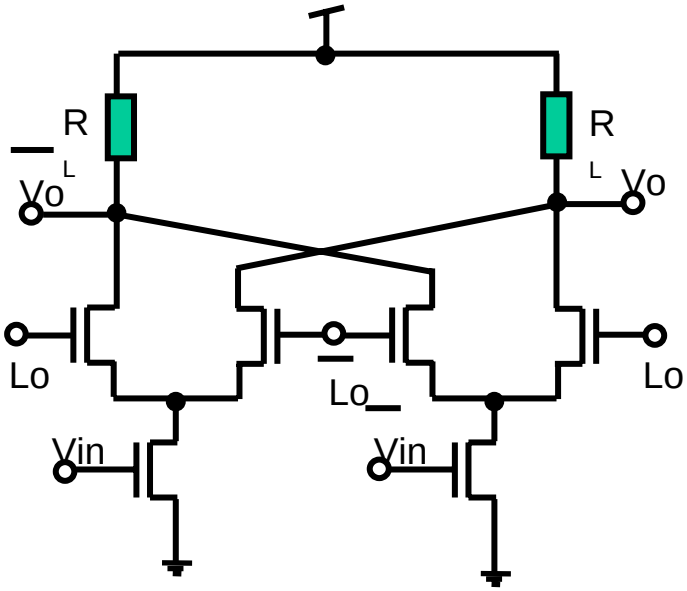
Mixer

The passive mixer can be realized by CMOS only.
High linearity, no 1/f noise effect, and low power are realized.

Active mixer (same as bipolar)

High conversion gain
High isolation

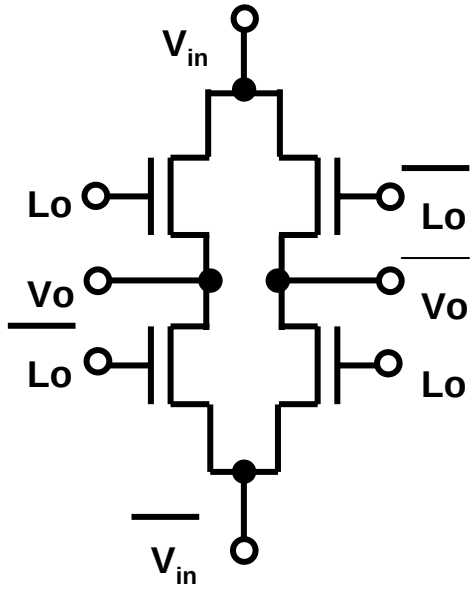
Larger power
Larger distortion
Larger 1/f noise



Passive mixer (MOS only)

Low power
High linearity
No 1/F noise

No conversion gain
No isolation, Bi-directional



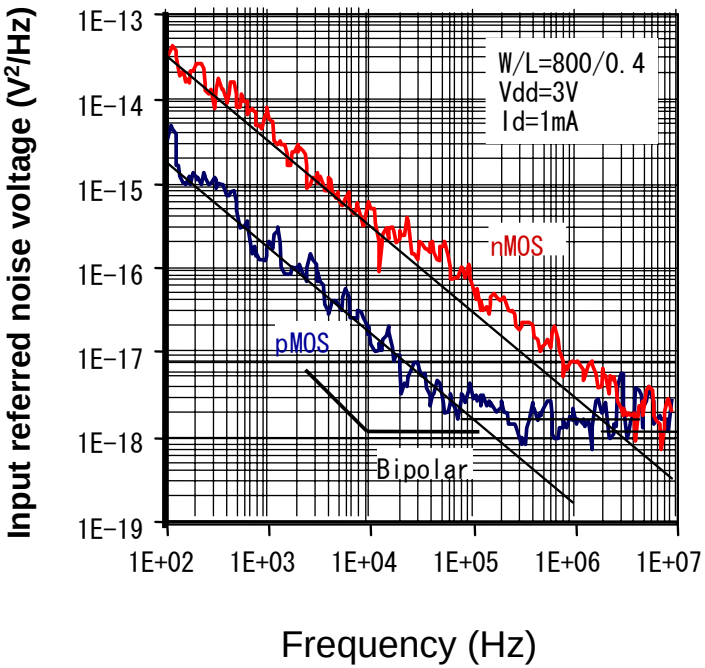
1/f noise

1/f noise of MOS is larger than that of bipolar.

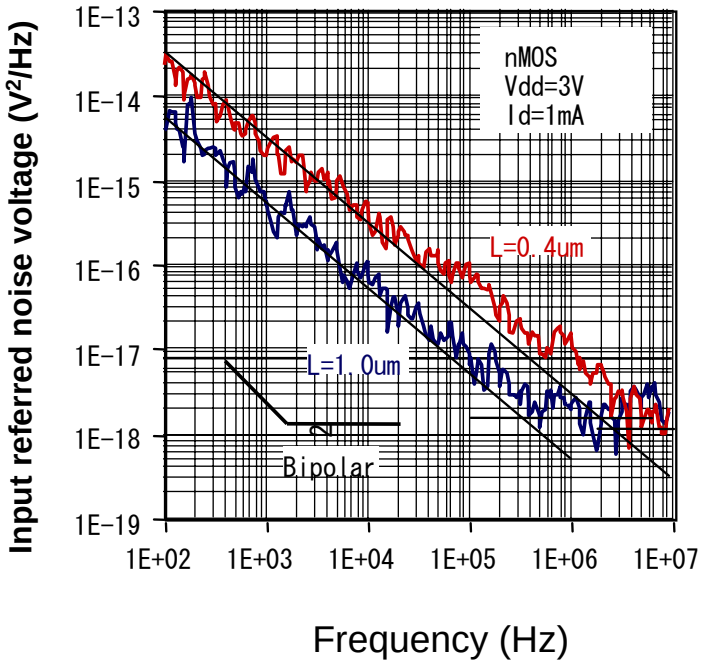
For the lower 1/f noise, the larger gate area is needed.

$$V_{nf}^2 = \frac{S_{vf}}{LW}\frac{\Delta f}{f}, \qquad S_{vf} \propto T_{ox}^2$$

Nch/Pch 0.4um



Nch 0.4um/1.0um



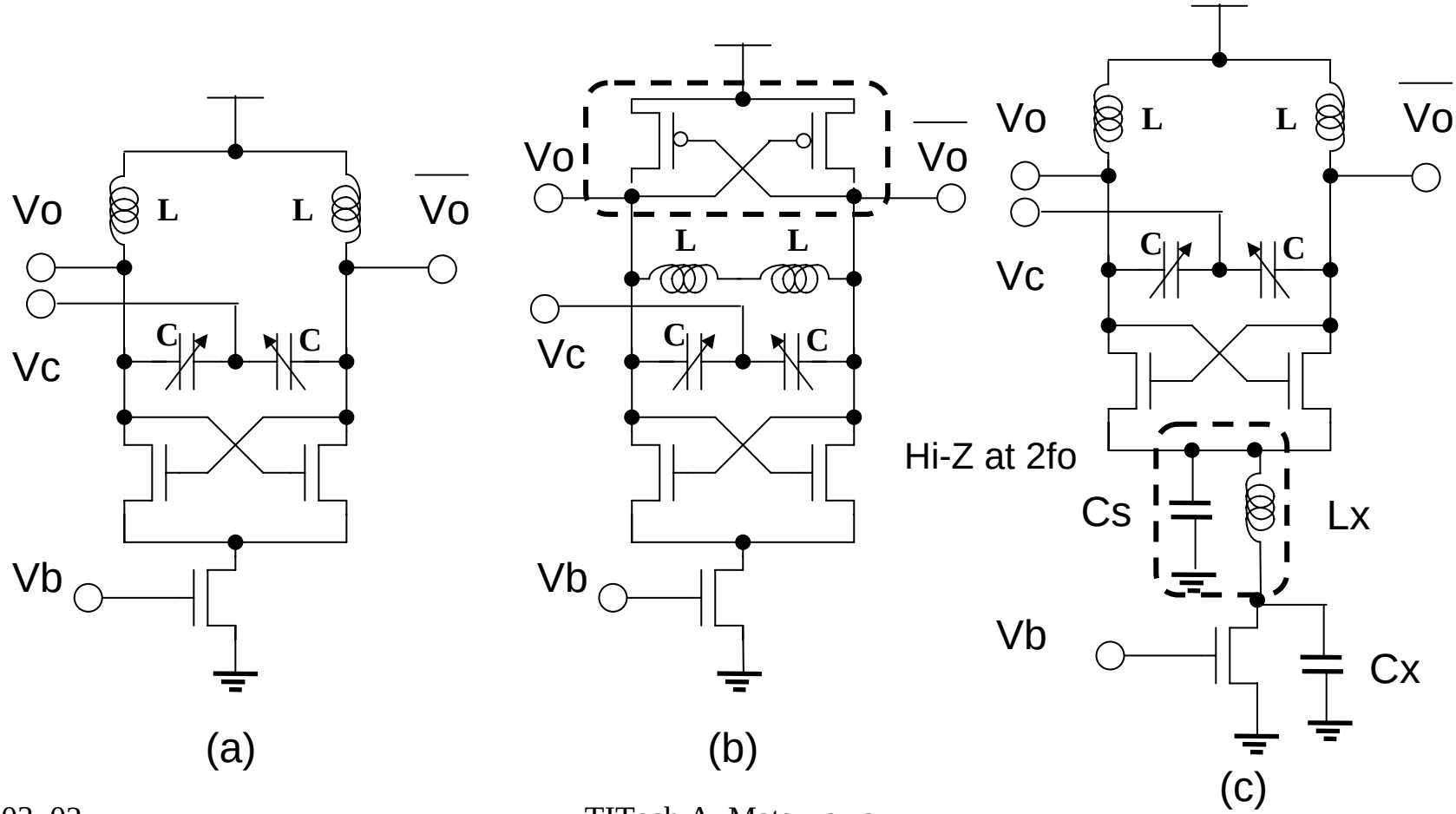
CMOS oscillator circuits

E. Hegazi, ISSCC 2001

Basic

Low power (gm is higher)

Low noise by filtering



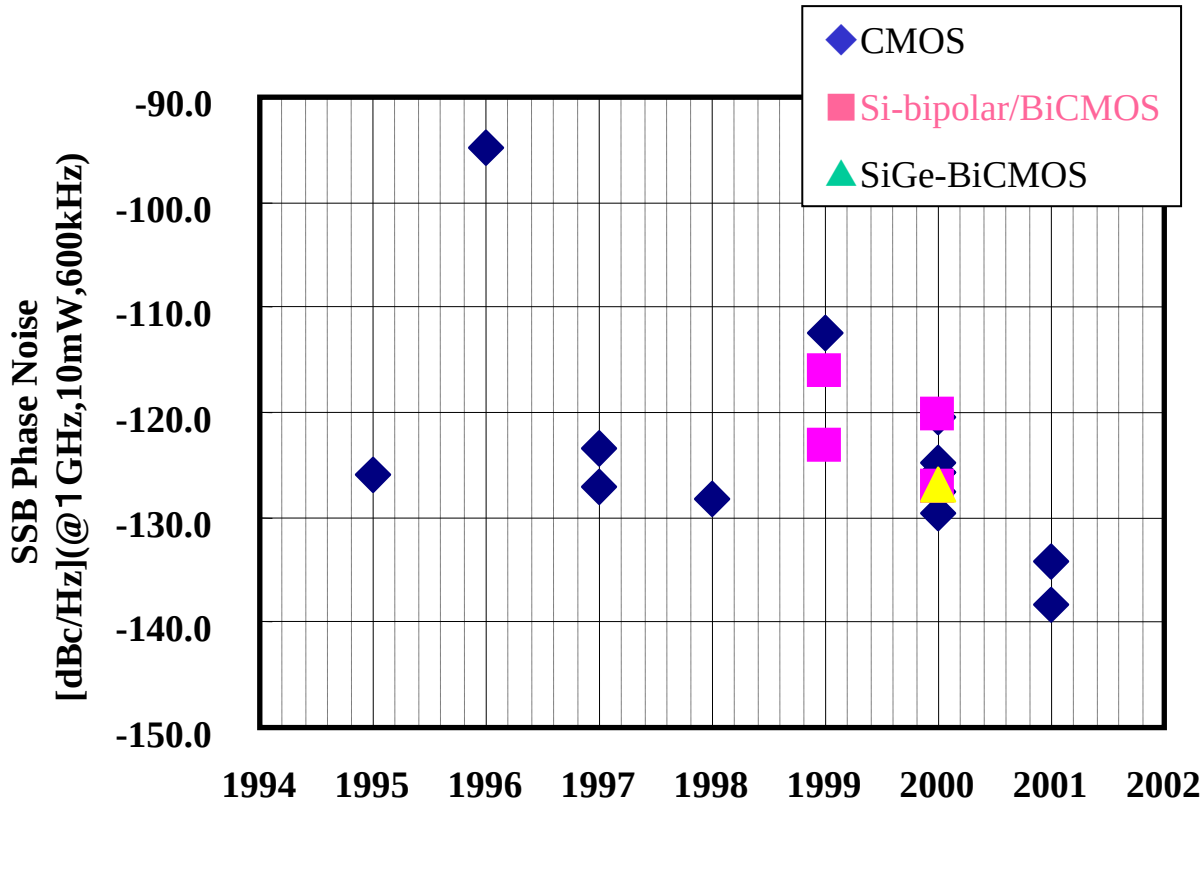
Oscillator phase noise progress

Phase noise in CMOS oscillator becomes lower than that of bipolar.

The larger voltage swing in MOS Oscillator realizes lower oscillation phase noise.

(High Q inductance is also very effective to reduce phase noise)

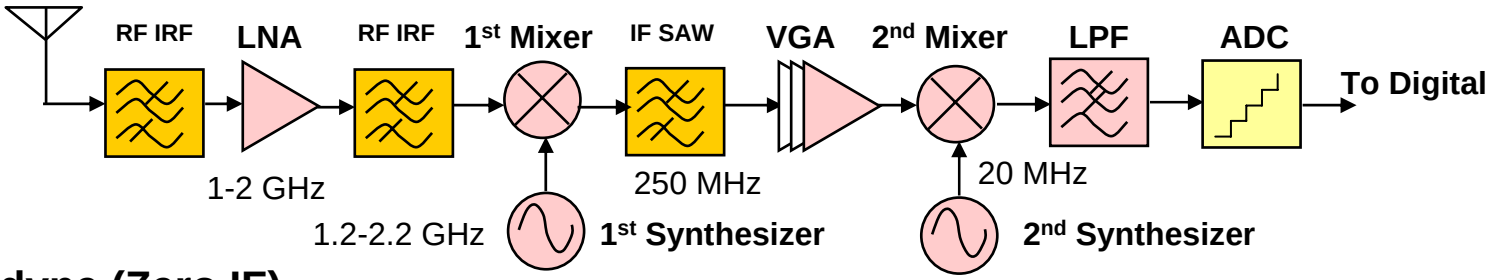
$$L(f_m) \propto \frac{1}{V_o^2} \cdot \frac{1}{Q^2} \cdot \left(\frac{f_o}{f_m} \right)$$



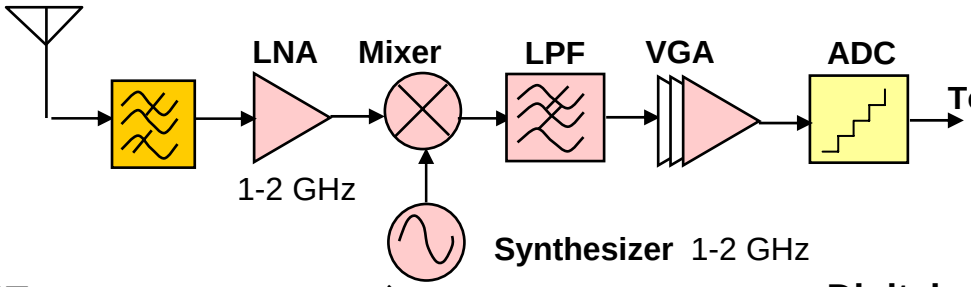
Architecture 1

Simpler architecture should be chosen to reduce power, area, and cost.

1) Super Heterodyne （Larger power, cost）



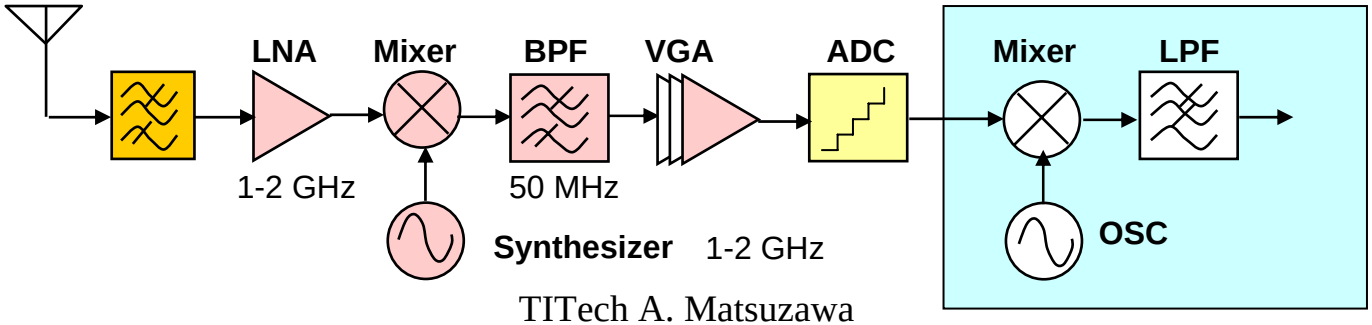
2) Homodyne (Zero IF) （Lower power and cost, however... , ）



DC offset
Lo leak
1/f noise

3) Low IF (Middle position）

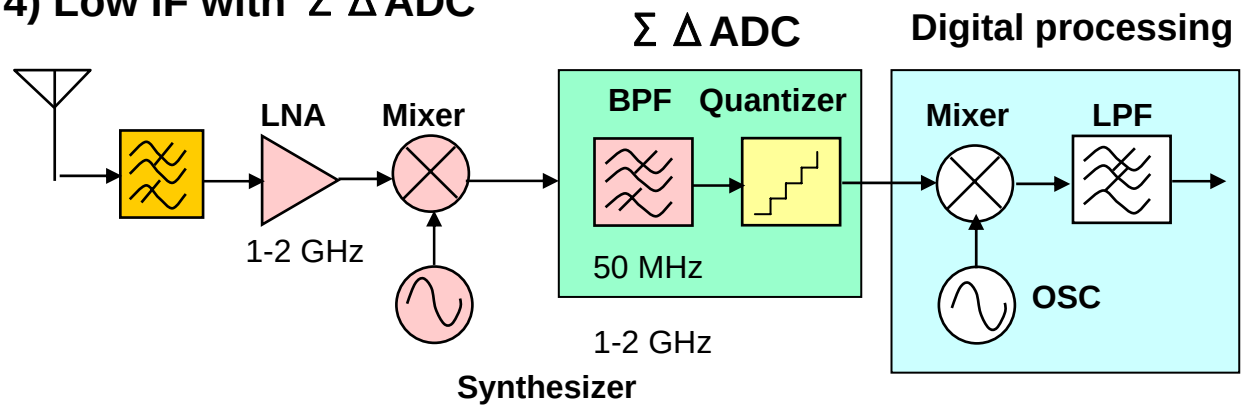
Digital processing



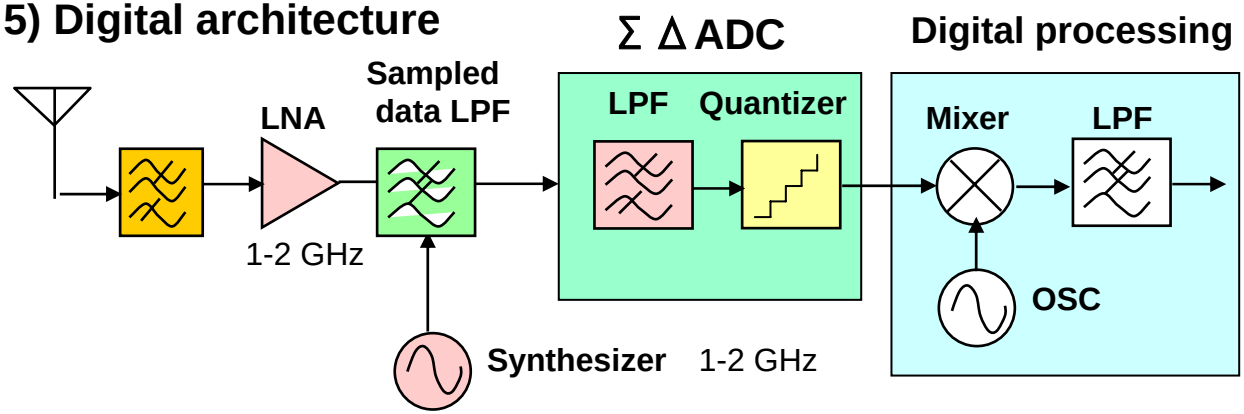
Architecture 2

Analog circuits have been replaced by digital circuits.
Small analog and big digital is a technology direction.

4) Low IF with Σ Δ ADC



5) Digital architecture



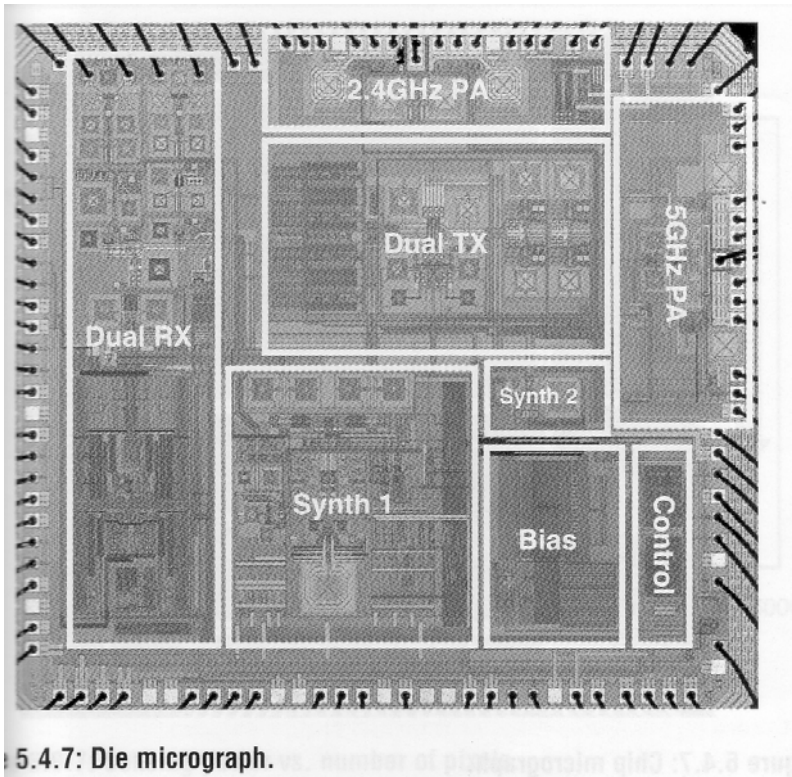
Bluetooth receiver
0.13um CMOS
1.5V

K. Muhammad (TI), et al., ISSCC2004, pp.268

Technology edge RF CMOS LSI

Many RF CMOS LSIs have been developed for many standards

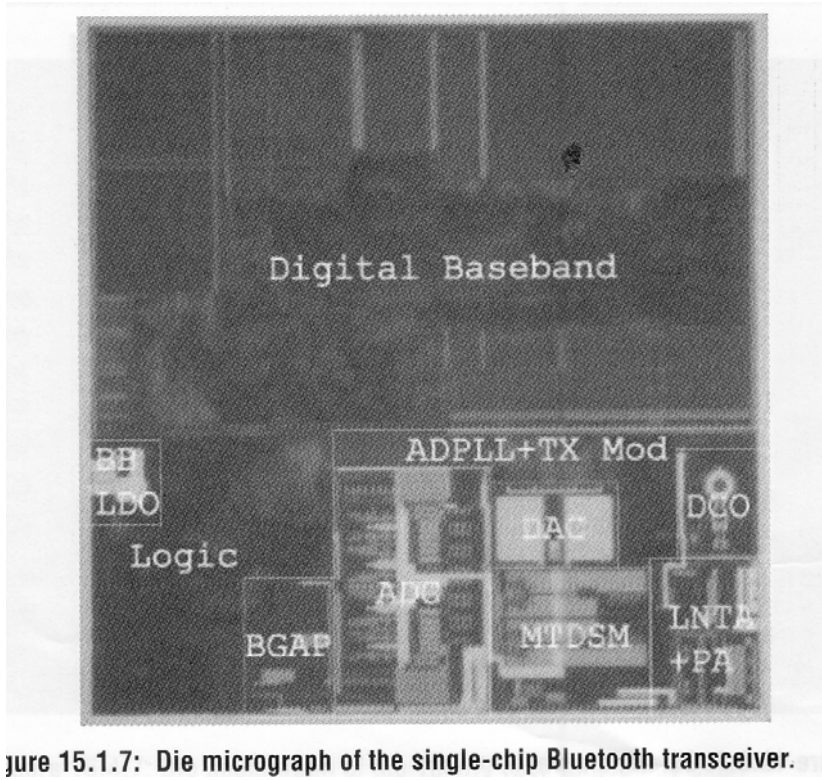
Wireless LAN, 802.11 a/b/g
0.25um, 2.5V, 23mm^2, 5GHz



5.4.7: Die micrograph.

M. Zargari (Atheros), et al., ISSCC 2004, pp.96

Discrete-time Bluetooth
0.13um, 1.5V, 2.4GHz



ure 15.1.7: Die micrograph of the single-chip Bluetooth transceiver.

K. Muhammad (TI), et al., ISSCC2004, pp.268

Advantage of SiGe Bi-CMOS

SiGe Bip has a great advantage in power consumption

		Alcatel[1)]	Oki	Broadcom	Conexant	Mitsubishi
Process		CMOS 0.25um	CMOS 0.35um	CMOS 0.35um	**SiGe**-BiCMOS 0.5um	Si-BiCMOS 0.5um
Chip size"		40.1mm2	18.0mm2			17.0mm2
Rx_Sens.		-80dBm	-77dBm	-80dBm	-78dBm	-80dBm
Tx_Power		+2dBm	+2.5dBm	+5dBm	+2dBm	0dBm
Id	Rx	50mA	47mA	46mA	**12mA**	34.4mA
	Tx	70mA	66mA	47mA	**16.4mA**	44.0mA
Vdd		2.5V	2.7-3.3V	3V(?)	1.8-3.6V	2.7-3.3V

Potential and limitation of RF CMOS

- **Potential**
  - RF CMOS are going to be a major in the wireless products.
  - SiGe Bi-CMOS technology will be used for only extremely low noise and low power RF products.
  - 60GHz or 100GHz CMOS circuits has already developed.

- **Limitation**
  - For low noise and low power characteristics in RF circuit, SiGe bipolar technology must be better than CMOS.
  - High power PA will not be integrated on scaled CMOS chip, due to low efficiency and needs low voltage operation.
  - Use of further advanced technology beyond 90nm would be limited. This is because low analog operating voltage of less than 0.9V and chip and development cost increase.

Expectation for new passive devices

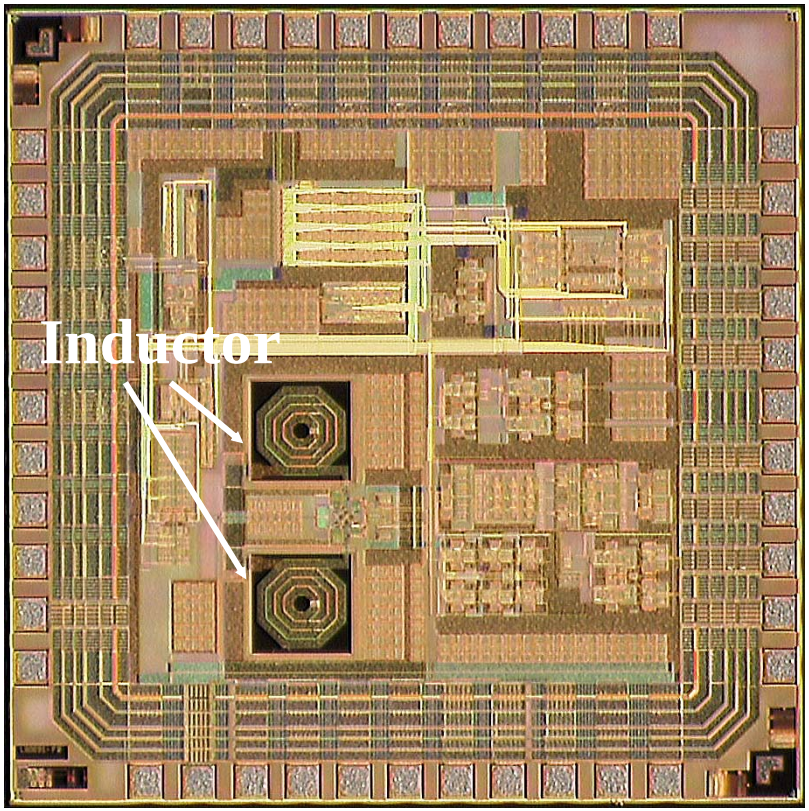
This would sound inconsistent with RF CMOS technology

RF CMOS technology is going to reducing analog and passive components.

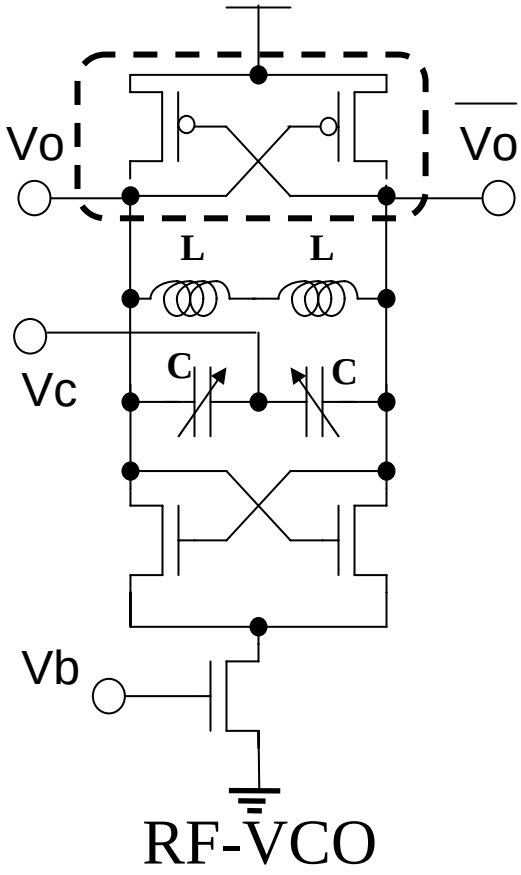
- **However, passives are still important**
  - **High Q inductance**
    - **VCO: reduce power and phase noise**
    - **LNA: reduce power and noise figure**
  - **Tunable inductor**
    - **Multi frequency, yet single inductance.**
    - **Reconfigurable RF circuits**
  - **RF band pass filter**
  - **RF switches**
    - **TX/RX**
    - **Select frequency bands to address multi-standards**
    - **Reconfigurable RF circuits**
  - **On chip solid reference Oscillator**

Inductor

Q of inductor determines almost all the performance of RF oscillator. Q is conventionally less than 10.



RF-CMOS LSI



RF-VCO

Noise:

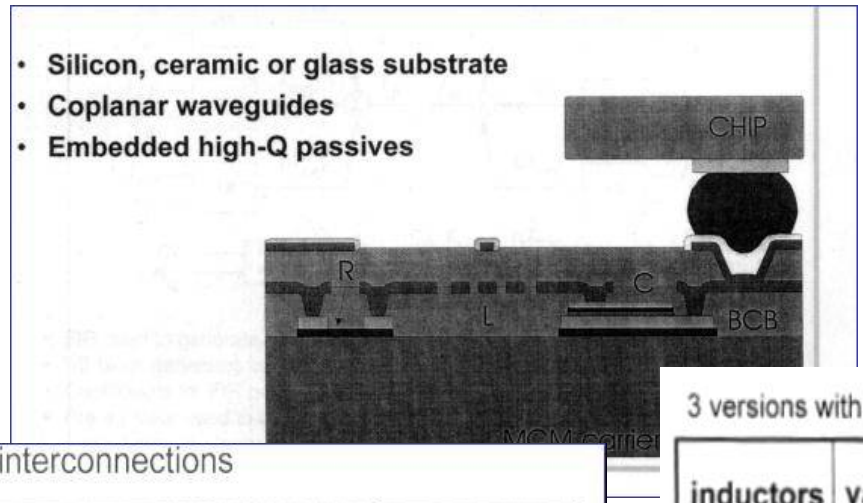
$$S_\phi \propto \frac{1}{Q^2}$$

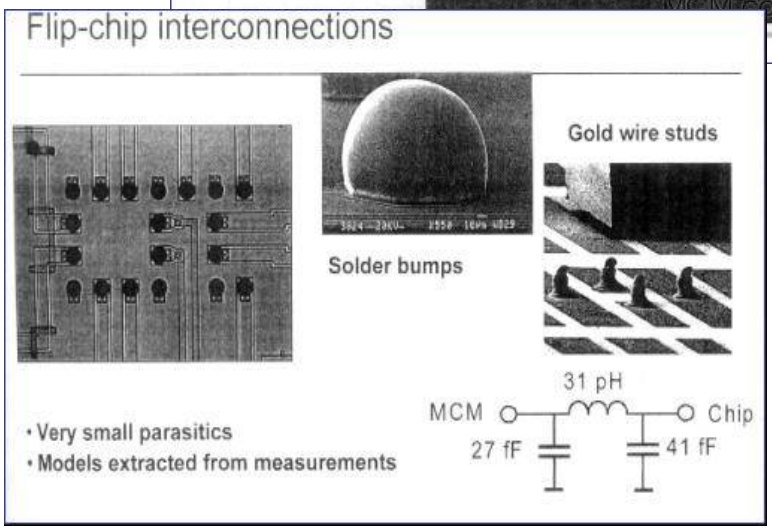
Current

$$I \propto \frac{1}{Q}$$

RF application of flip chip technology

High performance RF circuit has been realized by using the flip chip technology.





Qmax=63 @9.2GHz

3 versions with constant output power: -7 dBm (single-ended)

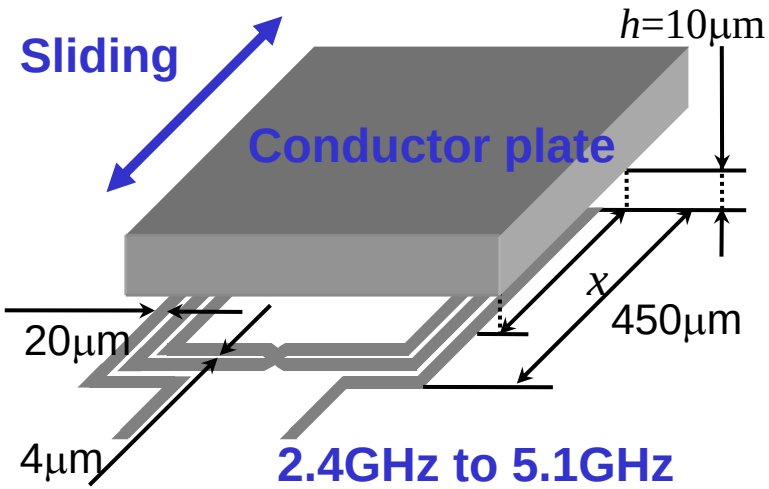
inductors	varactors	phase noise (dBc/Hz @ 100 kHz)	Power (mW)	FOM
on-chip Q=5.5	on-chip Q=17	-86	17.8	167
MCM Q=50	on-chip Q=17	-90	9.5	173.7
MCM Q=50	off-chip Q=40	-92	7.9	176.5

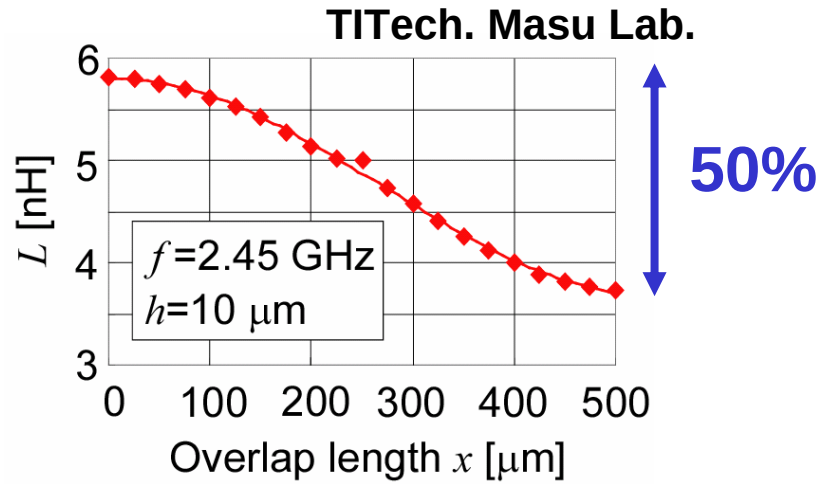
(simulated results)

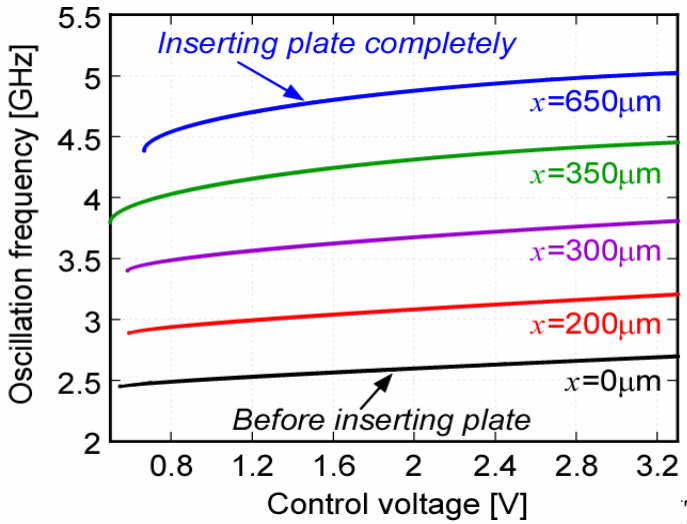
W.P.Donnay, et al., ISSCC 2000, WA 19.1

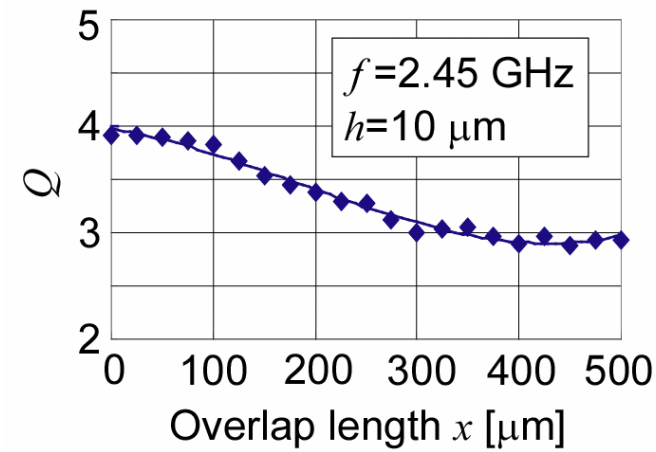
Variable Inductor

Sliding plate can vary inductance by 50%.
Wide tunable range VCO (2.4GHz to 5.1GHz) has been realized.





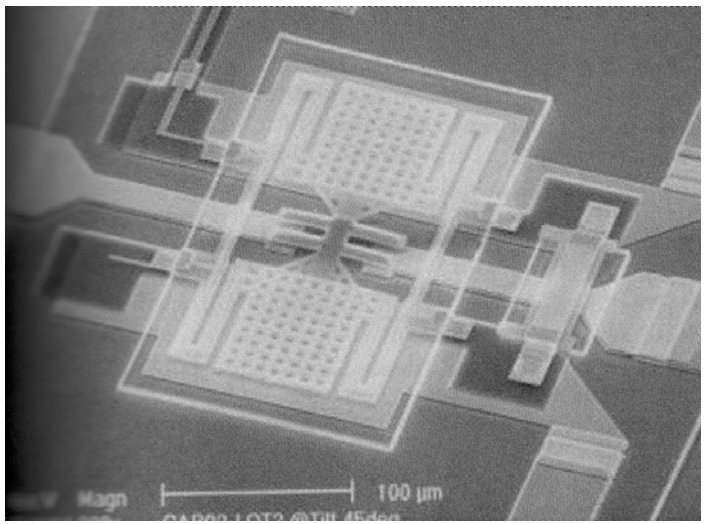


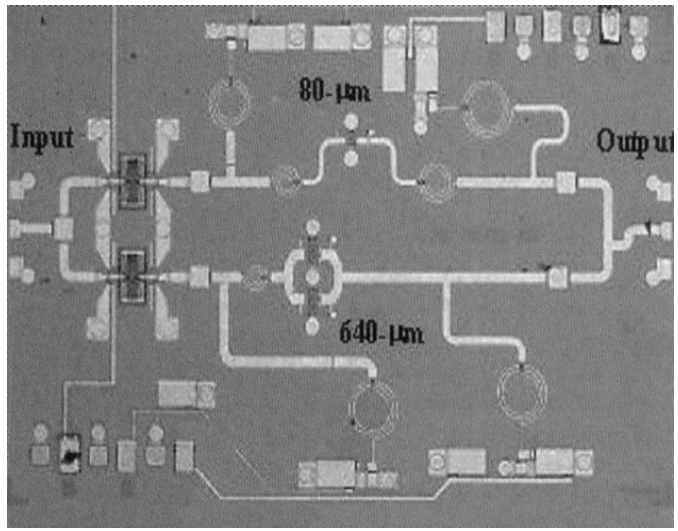


RF MEMS switch

Mechanical low-loss integrated switch enables;

Select or change inductance and capacitance
Select signals and circuits;
As a result, enables reconfigurable RF circuits

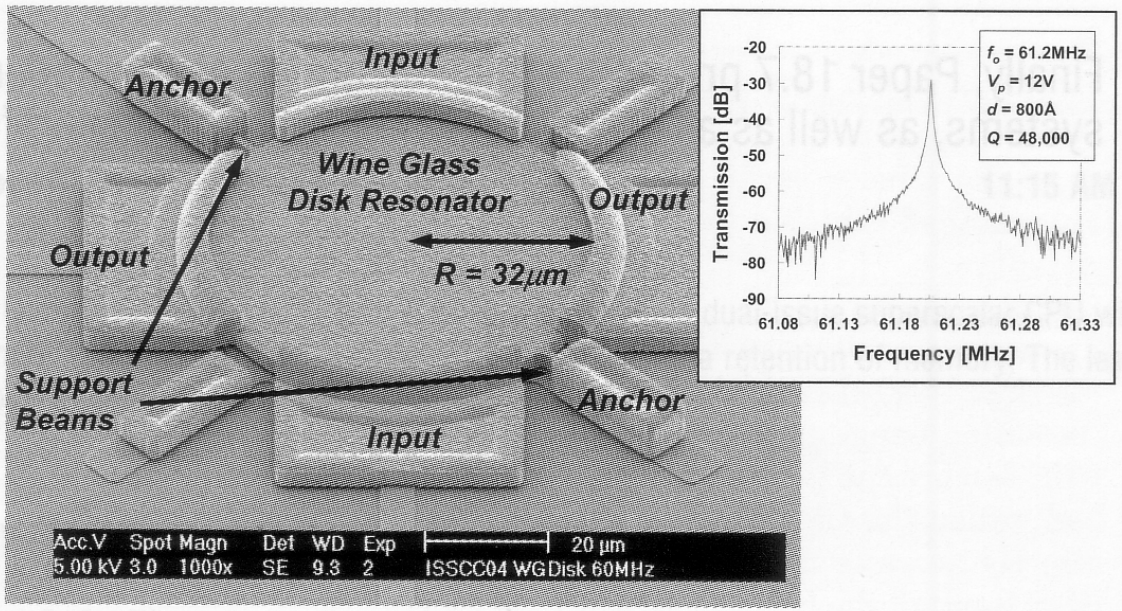




J. DeNatale, ISSCC 2004, pp. 310

Micromechanical-Disc Reference Oscillator

MEMS technology will realize an on-chip solid reference oscillator



Fo=61MHz
Q=48,000
-145dBc/Hz far-end
-115dBc/Hz @ 1KHz

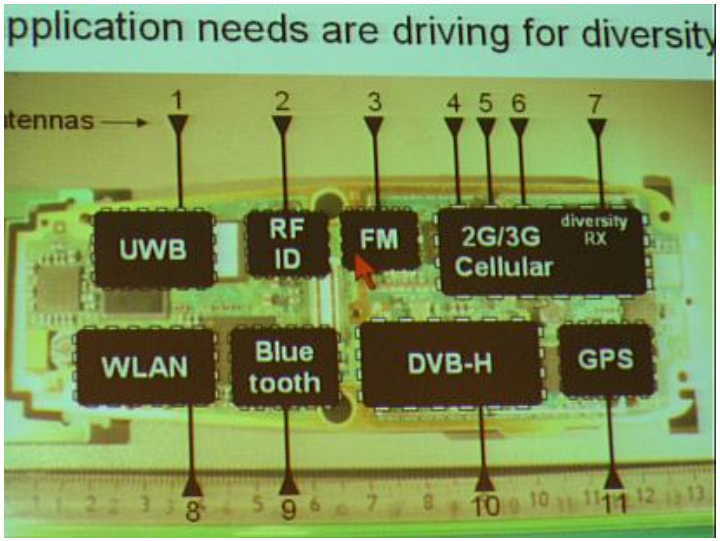
Yu-Wei Lin, et al., ISSCC 2004, pp. 322

Figure 17.7.6: Scanning electron micrograph (SEM) of a fabricated wine glass disk resonator with two supports, with its measured frequency characteristic.

Multi-standard issue

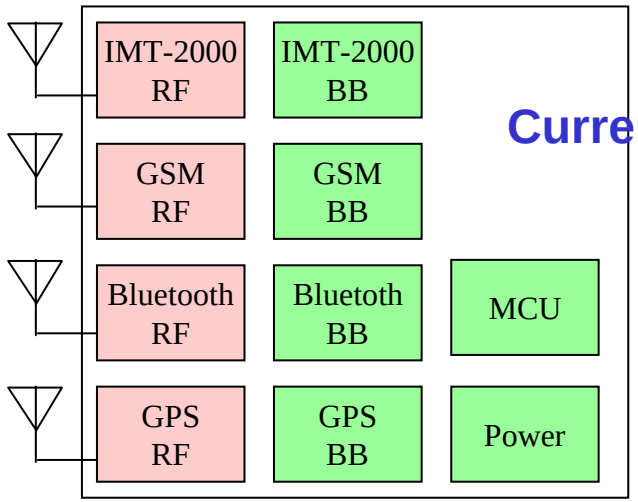
Reconfigurable RF circuit is strongly needed for solving multi-standard issue.

Future cellular phone needs 11 wireless standard!!



Yrjo Neuvo, ISSCC 2004, pp.32

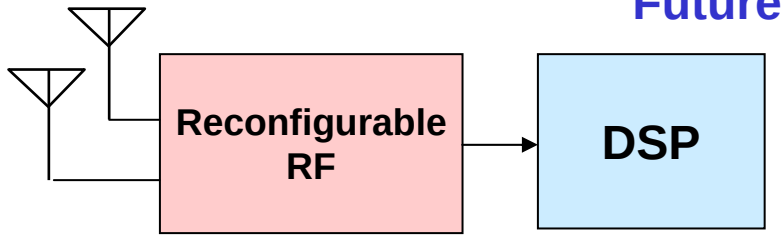
Multi-standards and multi chips



Current

Unification

Future



Unified wireless system

Summary

- **RF-CMOS technology**
  - **Becomes major**
    - **Performance increase and full system integration due to scaling**
    - **Development of suitable circuits and architecture**
    - **Small analog and large digital is a right way**
    - **Low cost and huge supply capacity**
  - **However, some issues**
    - **For low power and now noise, SiGe Bi-CMOS is better**
    - **Limited use of further scaled CMOS beyond 90nm**
- **Expectation of new passive device**
  - **Great demand for reconfigurable RF circuits:**
    - **Switches for the reconfigurability**
    - **On chip RF filter and Oscillator**
    - **High quality and tunable inductance**