Mixed signal SoC:
A new technology driver in LSI industry

Akira Matsuzawa

Matsushita Electric Industrial Co., Ltd

(Tokyo Institute of Technology, after this April)

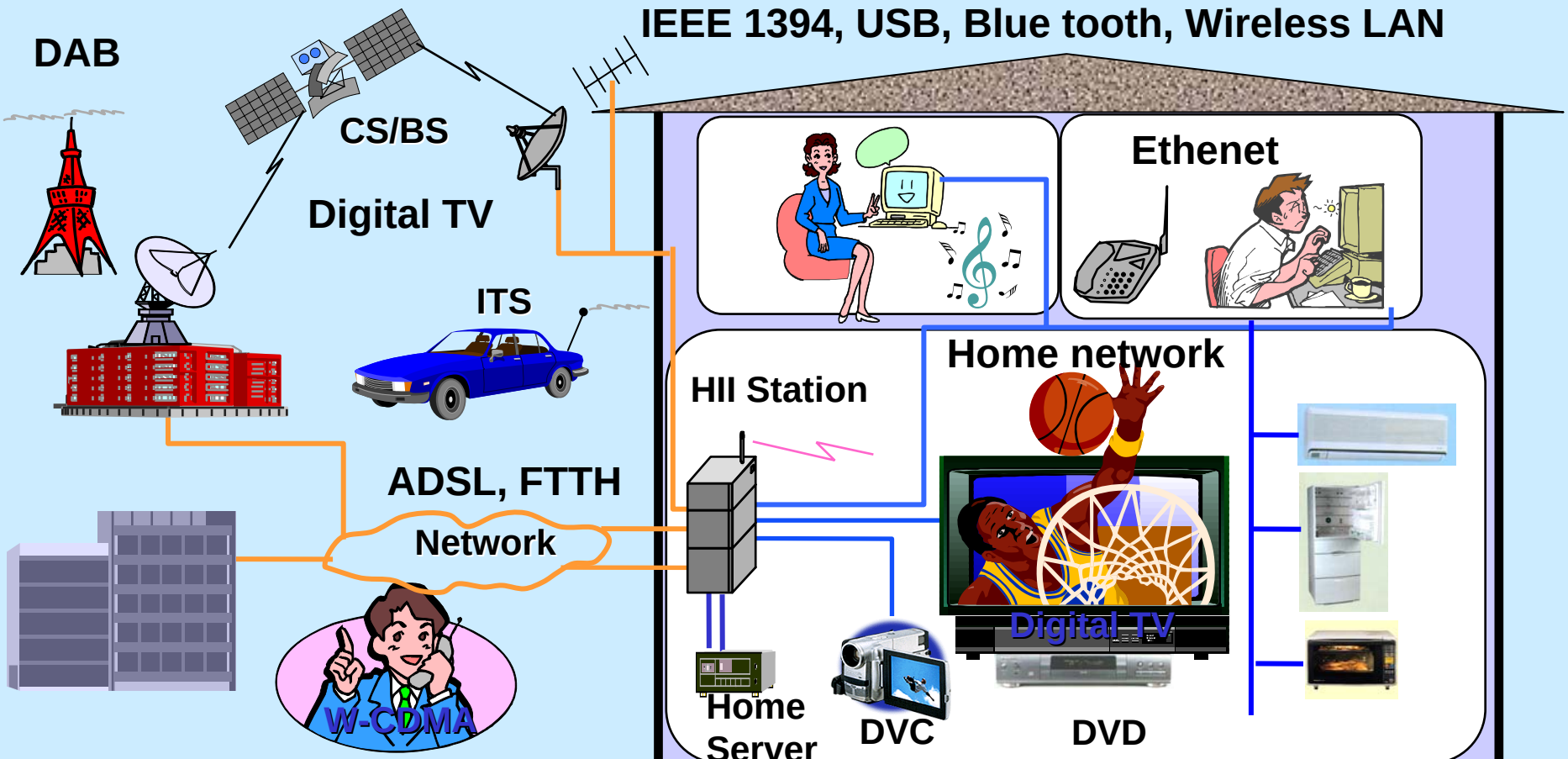
Contents

- Introduction
- Current electronics and mixed signal technology
- CMOS as an analog device
- Development strategy and design system for mixed signal SoC
- Issues of mixed signal SoC and solutions
- Summary

Current electronics and mixed signal technology

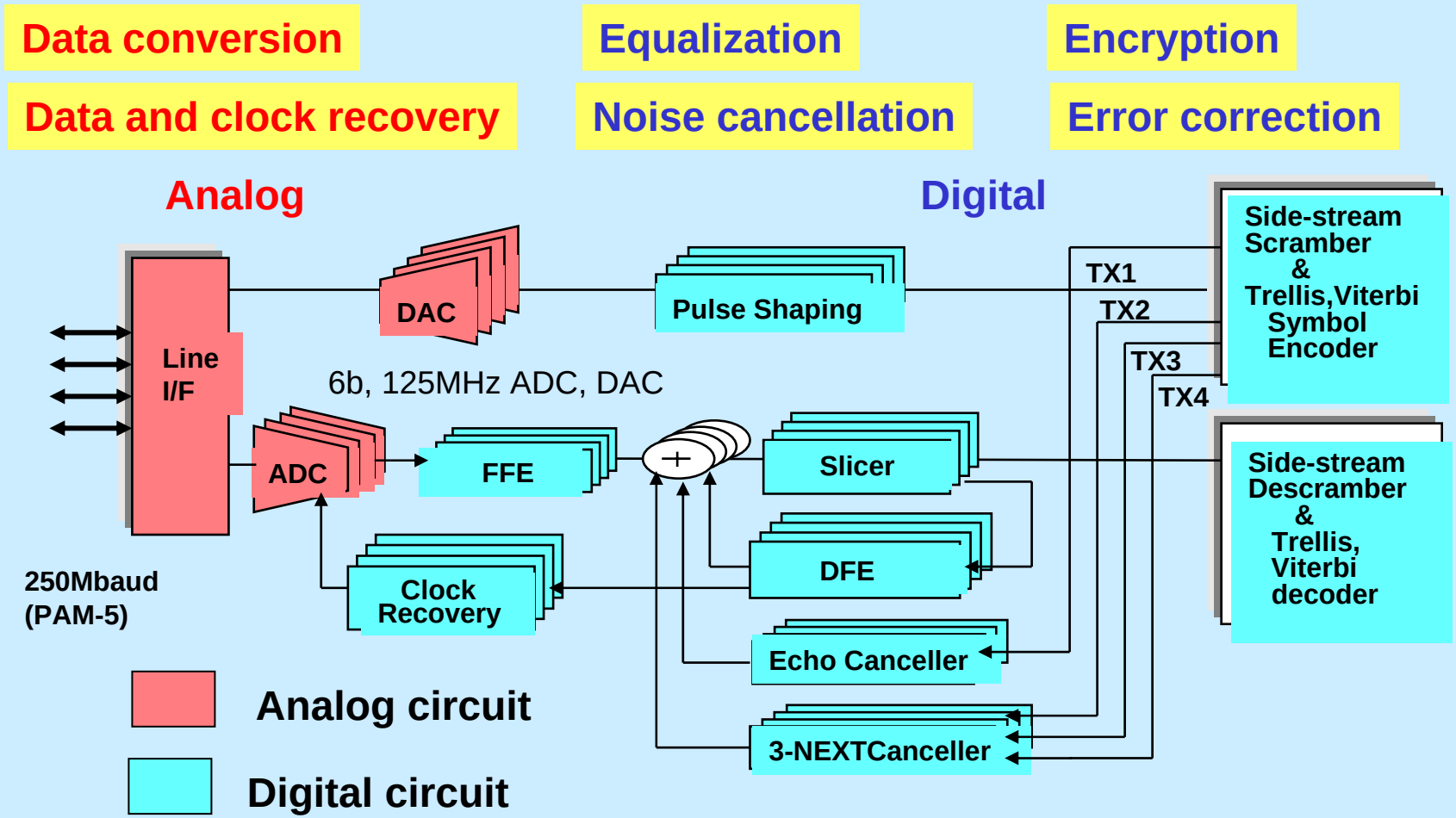
Image of current electronics

Digital consumer electronics and networking drive current electronics.



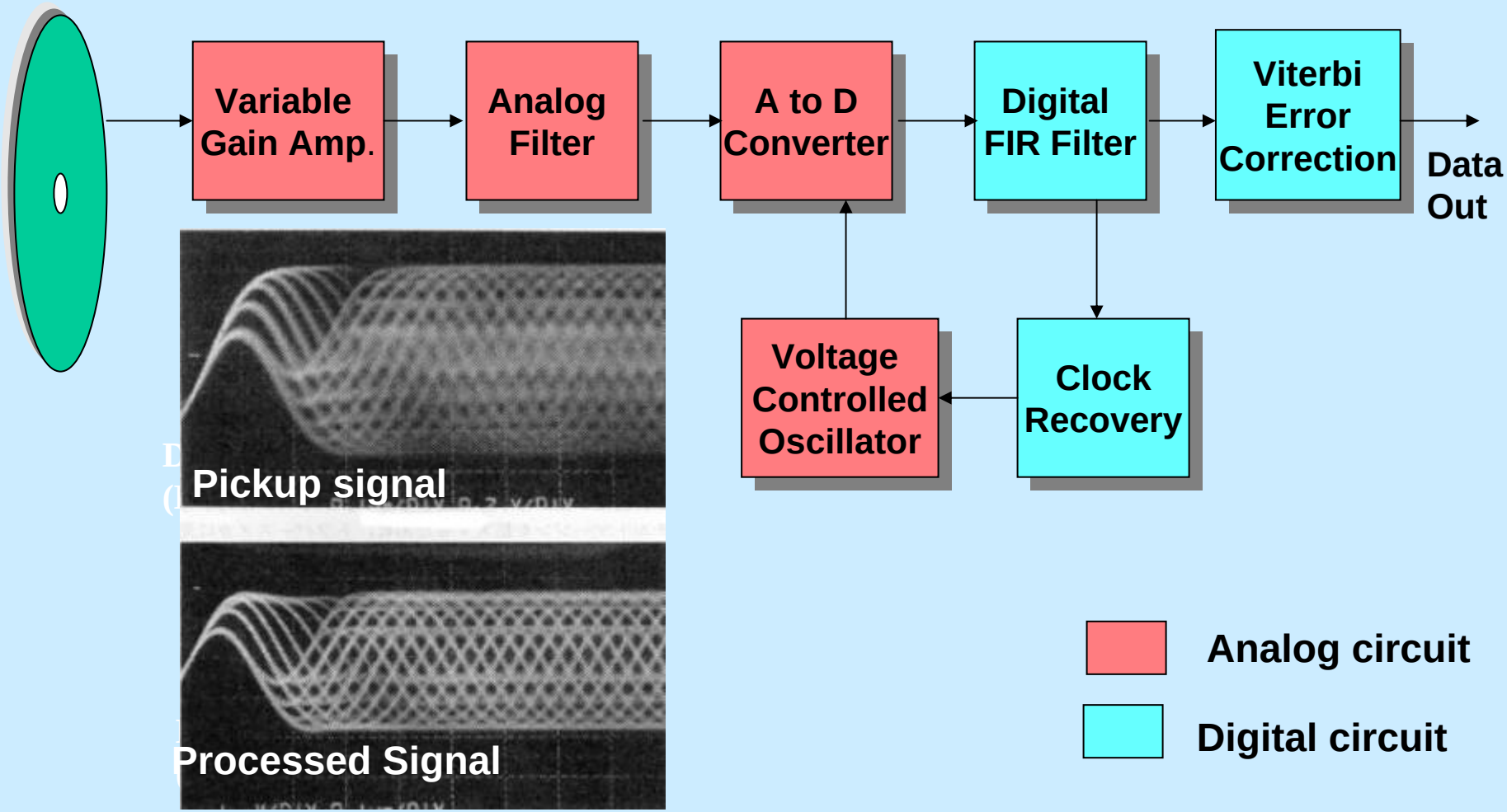
Mixed signal technology :Digital networkings

Mixed signal technology enables high speed digital networking.



Mixed signal tech. ;Digital read channel

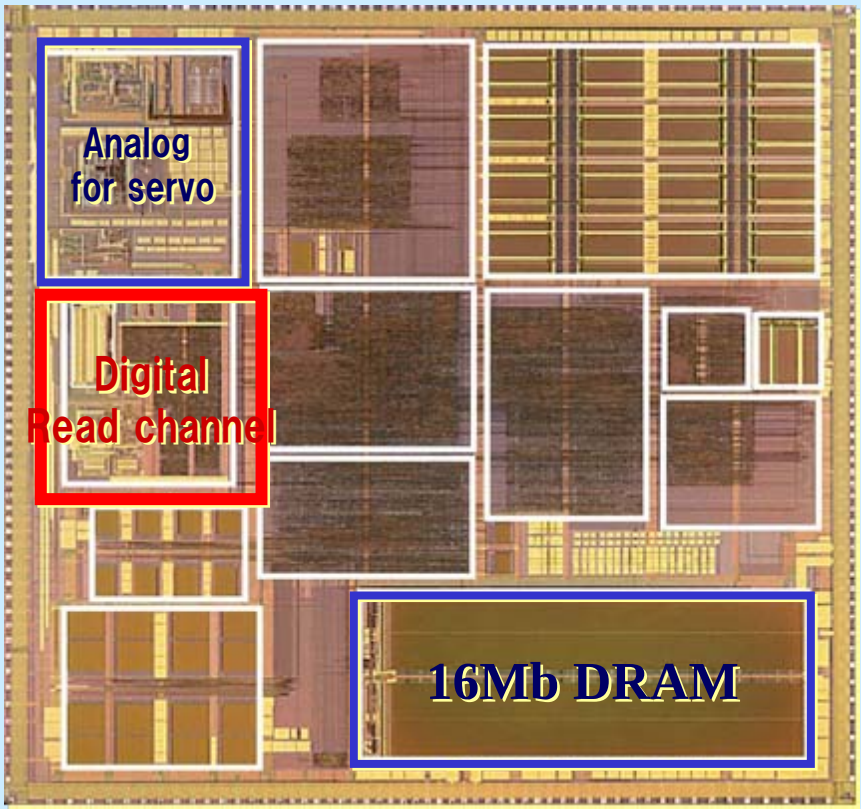
Digital storage also needs high speed mixed signal technologies.



Mixed signal SoC for DVD RAM system

This enables high readability for weak signal from DVD RAM pickup.

World fastest and highly integrated mixed signal CMOS SoC



0.18um- eDRAM

24M Tr
16Mb DRAM

500MHz
Mixed Signal

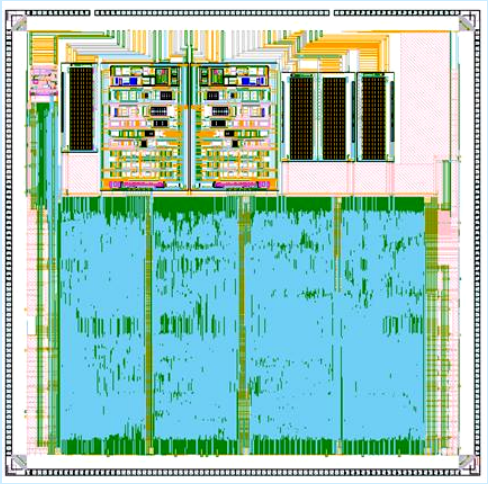
Goto, et al., ISSCC 2001

Recent developed mixed signal CMOS LSIs

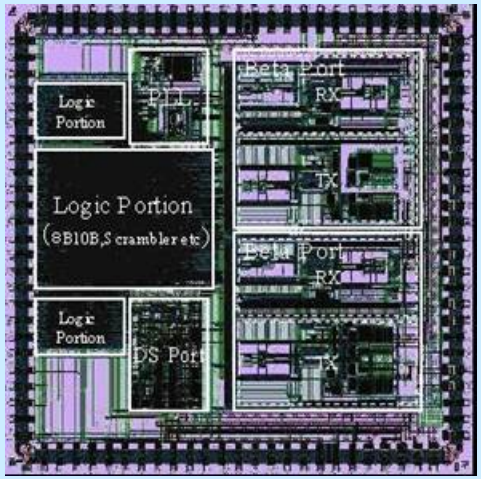
AFE (Analog Front End)

5G RF LAN

12b 50MHz ADC 2ch
12b 50MHz DAC 2ch

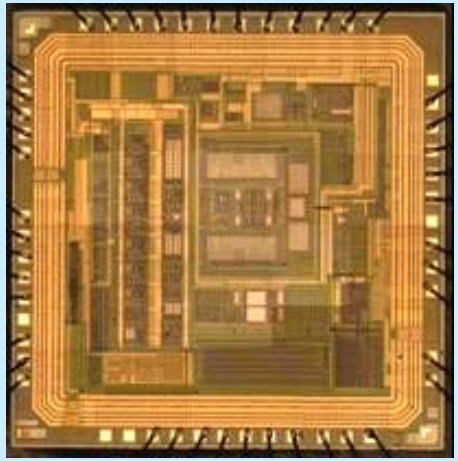


Digital network 1394b (1GHz)



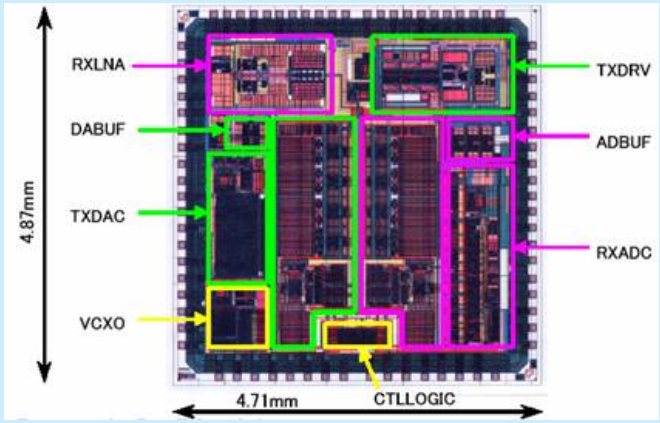
AFE for Digital Camera

12b 20MHz ADC+AGC

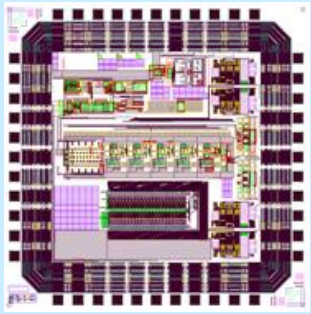


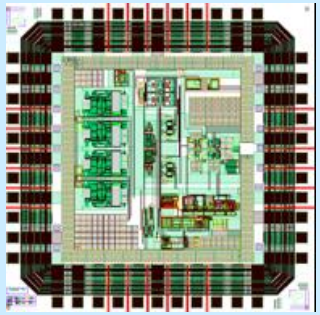
AFE for ADLS

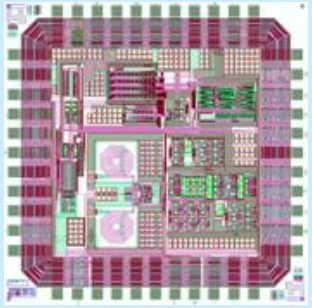
12b 20MHz ADC+DAC



2GHz RF CMOS







Application area in mixed signal CMOS tech.

Almost all the products need mixed signal CMOS LSI tech.

Network Communication

Wireless

- Cellular phone: PDC, W-CDMA
- RR-Net: Bluetooth, IEEE802.11
- Broad cast: STB, DTV, DAB

Wired

- Optical:FTTH, OC-xx
- Metal: ADSL, VDSL, Power line modem
  - Serial: IEEE1394, USB, Ethernet
  - Parallel: DVI, LVDS

Recording

- DVD, VDC, HDD

Output

- LCD, PDP, EL, Audio drive

Input

- Camera, Others

Power supply

- Switching supply, Every LSIs (On-chip)

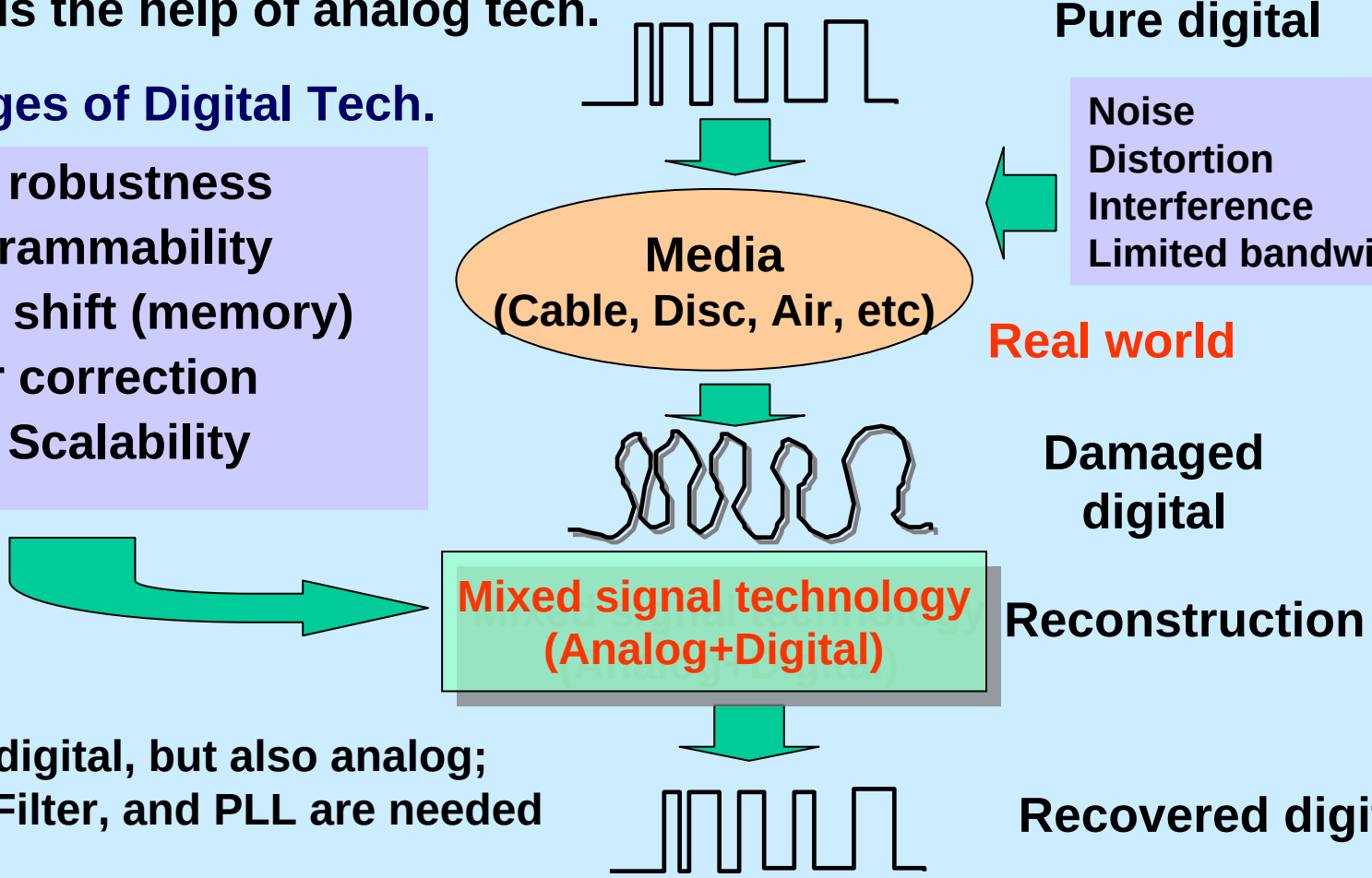
Digital technology in real world

Digital signal suffers heavy damage in real world.

But, digital can address this issue by own advantages, but needs the help of analog tech.

Advantages of Digital Tech.

- **High robustness**
- **Programmability**
- **Time shift (memory)**
- **Error correction**
- **High Scalability**

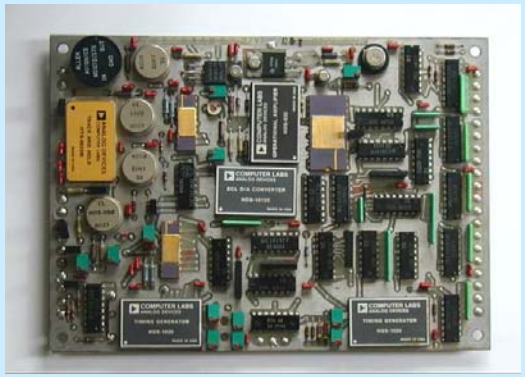


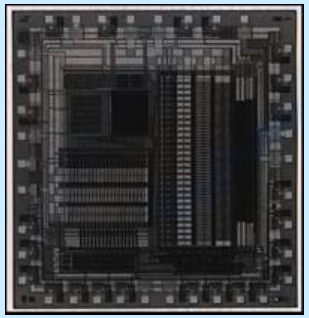
Not only digital, but also analog; ADC, DAC, Filter, and PLL are needed

Progress in A/D converter; video-rate 10b ADC

ADC is a key for mixed signal technology.
We have reduced the cost and power of ADC drastically;
1/ 2,000 for Power and 1/200,000 for the cost!
CMOS technology attained it. **dulling past 20 years**

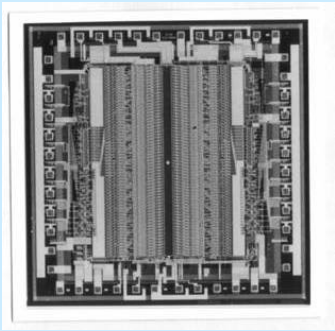
1980	1982	1993	Now
Conventional product	World 1st Monolithic	World lowest power	SoC Core
Board Level (Disc.+Bip)	Bipolar (3um)	CMOS (1.2um)	CMOS (0.15um)
20W	2W	30mW	10mW
$ 8,000	$ 800	$ 2.00	$0.04
Analog Devices Inc.	Our developed.	Our developed.	Our developed.





Progress in high-speed ADC

High speed ADC has reduced its power and area down to be embedded.

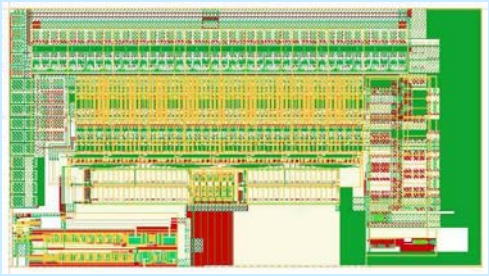


World fastest 6b ADC

6b, 1GHz ADC
2W,
1.5um Bipolar

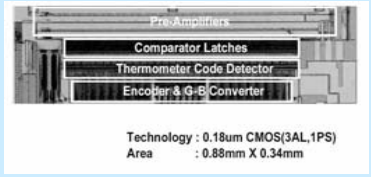
ISSCC 1991

ISSCC 2000 **World fastest CMOS ADC**



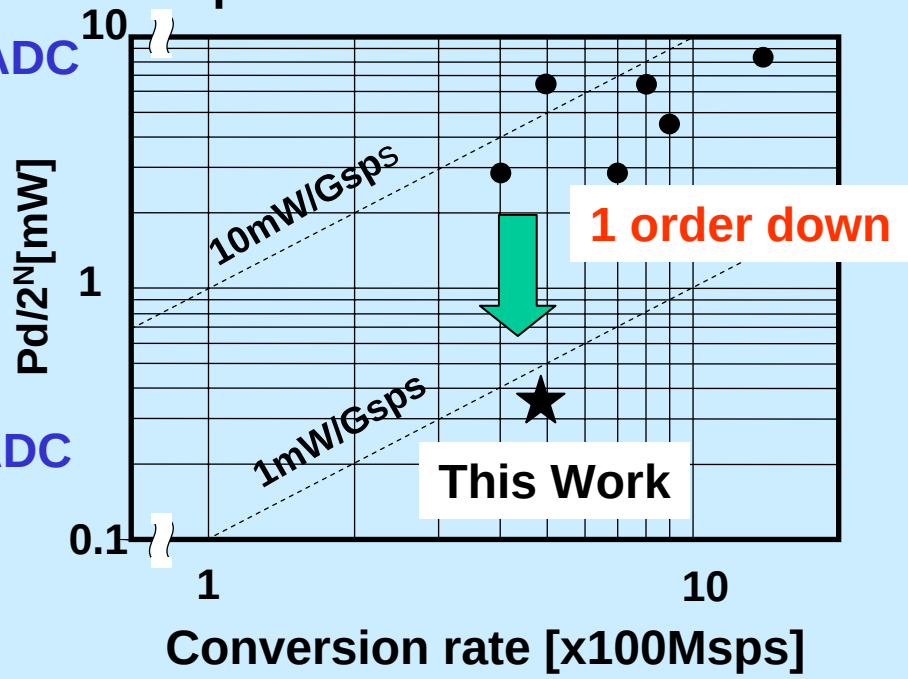
6b, 800MHz ADC
400mW, 2mm^2
0.25umCMOS

ISSCC 2002 **World lowest Pd HS ADC**



7b, 400MHz ADC
50mW, 0.3mm^2
0.18umCMOS

Reported Pd of CMOS ADCs

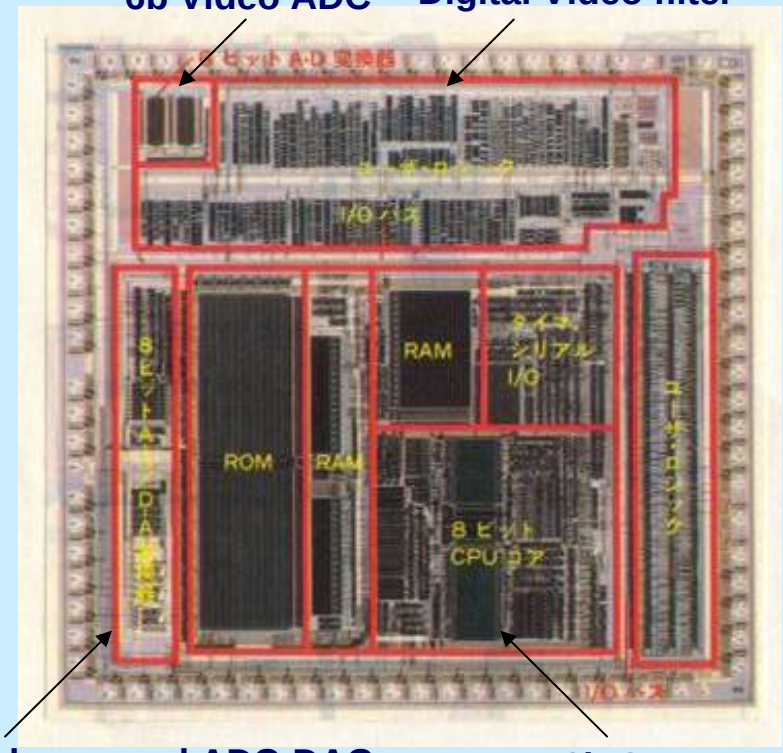


Early stage mixed signal CMOS LSI for CE

Success of CMOS ADC and DAC enabled low cost mixed signal CMOS LSI. This also enabled low cost and low power digital portable AV products.

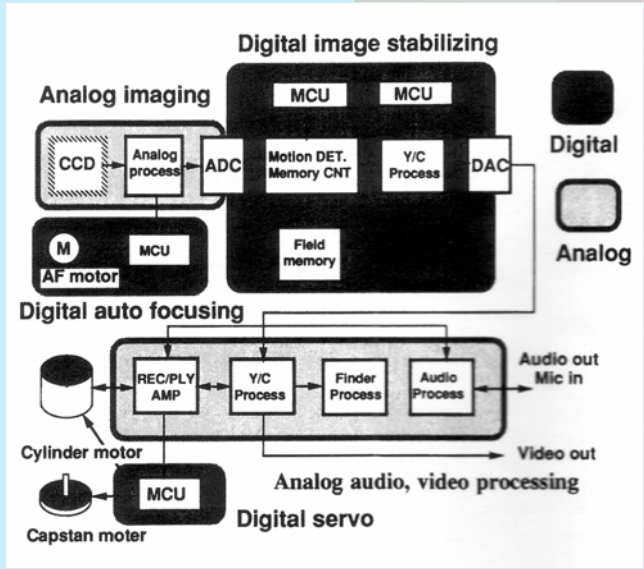
1993 Model: Portable VCR with digital image stabilizing

6b Video ADC **Digital Video filter**



8b low speed ADC;DAC **8b CPU**

System block diagram



CMOS as analog device

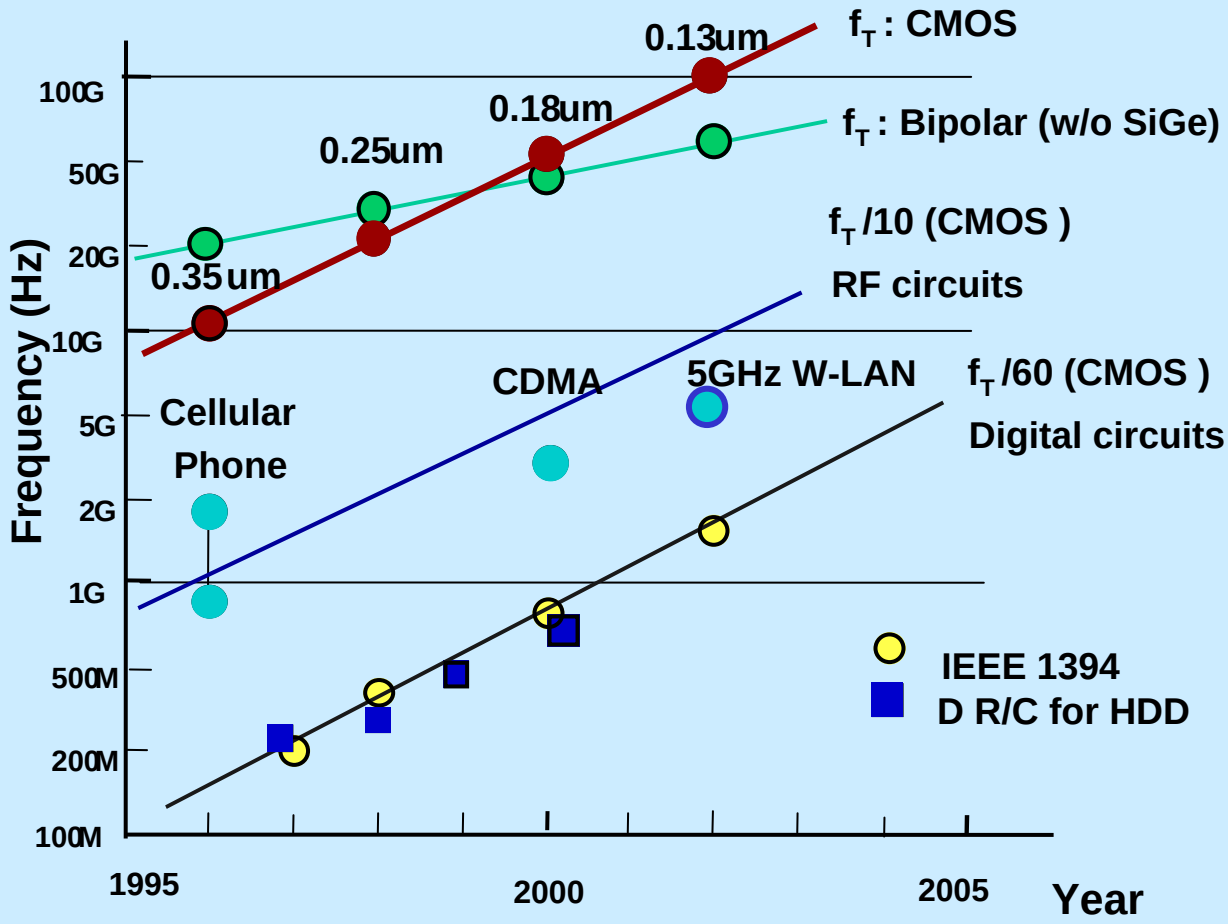
CMOS as analog device

**CMOS has many issues as analog device,
but also has a variety of circuit techniques**

	CMOS	Bipolar	Comment
Switch action	++	--	Only CMOS can realize switched capacitor circuits
Low Input current	++	--	
High gm	-	+	CMOS is ¼ of Bip.
Low Capacitance	+	-	This results in Cp issue
f_T	+	+	Almost same
Voltage mismatch	--	++	CMOS is 10x of Bip.
1/f noise	--	++	CMOS is 10x to 100x of Bip.
Low Sub. effect	-	+	
Offset cancel	++	--	CMOS has a variety of techniques to address the self issues
Analog calibration	++	--	
Digital calibration	++	--	
Embed in CMOS	++	--	

GHz operation by CMOS

Cutoff frequency of MOS becomes higher than that of Bipolar.
Over several GHz operations have attained in CMOS technology

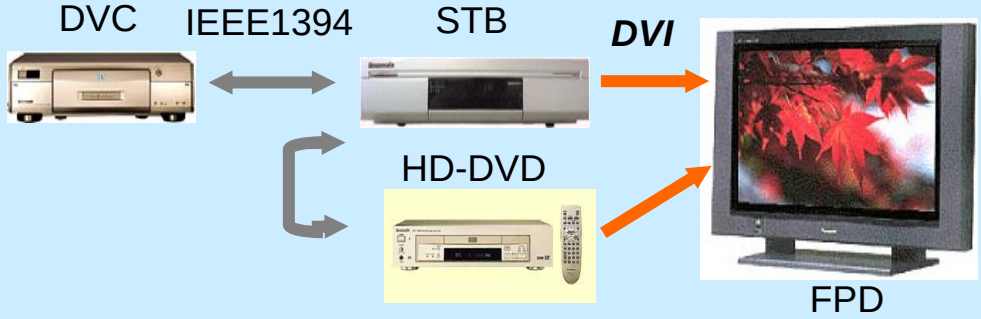


$$f_T \equiv \frac{gm}{2\pi C_{in}}$$

$$f_{Tpeak} \approx \frac{v_{sat}}{2\pi L_{eff}}$$

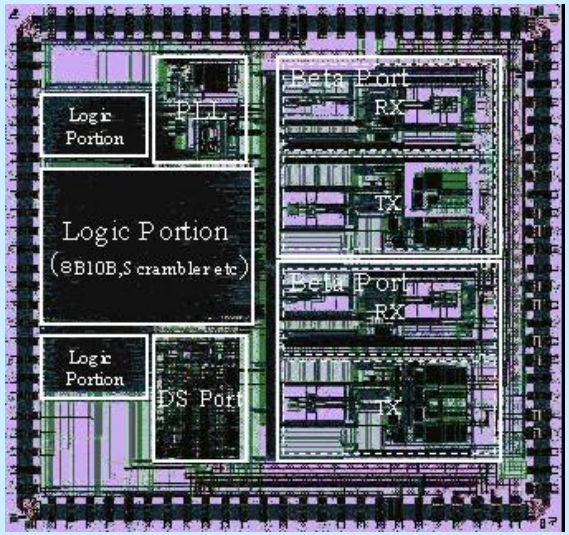
CMOS technology for over GHz networking

Digital consumer needs over GHz wire line networking.
CMOS has attained 5Gbps data transfer.



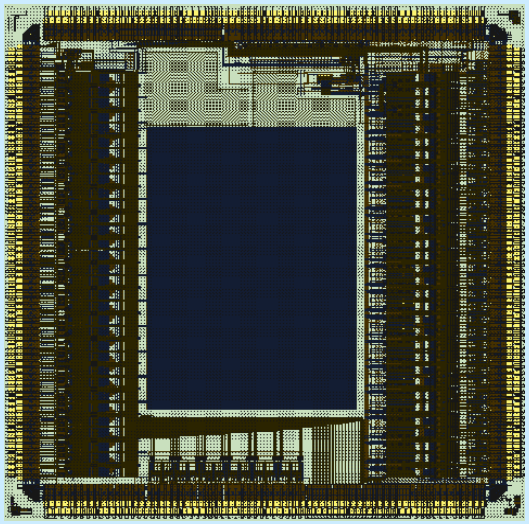
World first 1394b transceiver For 1Gbps networking

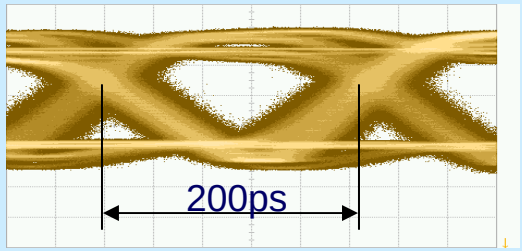
0.25um 3AL_CMOS



Test chip for 5Gbps wire line

0.18um 4AL_CMOS





5Gbps Eye pattern

f_T: MOS vs. Bipolar

Even if f_T of MOS is same as that of Bipolar,
f_T of MOS is easily lowered by parasitic capacitance.
Because, gm of MOS is ½ to ¼ of that of Bipolar at the same current.

MOS

$$gm \equiv \frac{Ids}{\left(\frac{V_{eff}}{2}\right)}$$

$$f_T \equiv \frac{gm}{2\pi Cin}$$

Bipolar

$$gm \equiv \frac{Ic}{U_T}$$

$$V_{eff\,\min} = 2nU_T \quad \text{n: 1.4}$$

$$U_T \equiv \frac{kT}{q} \approx 26mV$$

Veff/2: 50-100mV (actual ckt.)

$$gm_{CMOS} < \frac{1}{2}, \frac{1}{4} gm_{Bip}$$

（Same operating current）

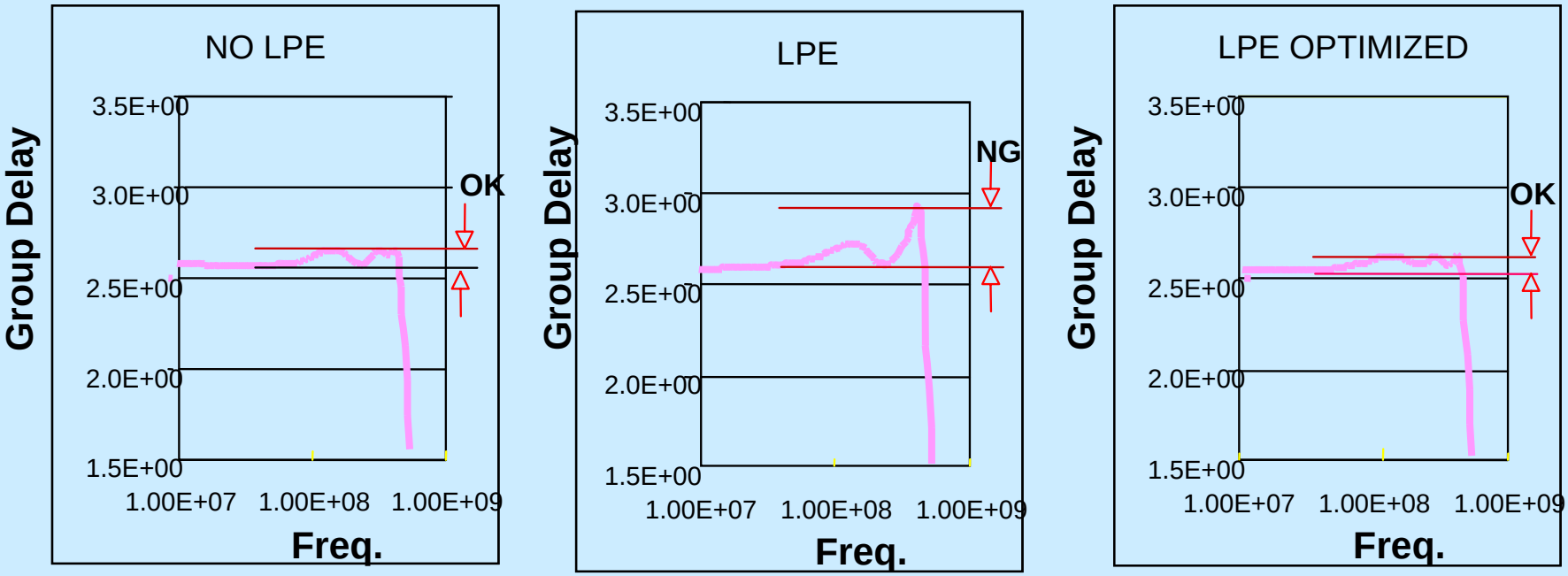
$$Cin_{CMOS} < \frac{1}{2}, \frac{1}{4} Cin_{Bip}$$

（Same f_T）

Parasitic effect: CMOS CT filter

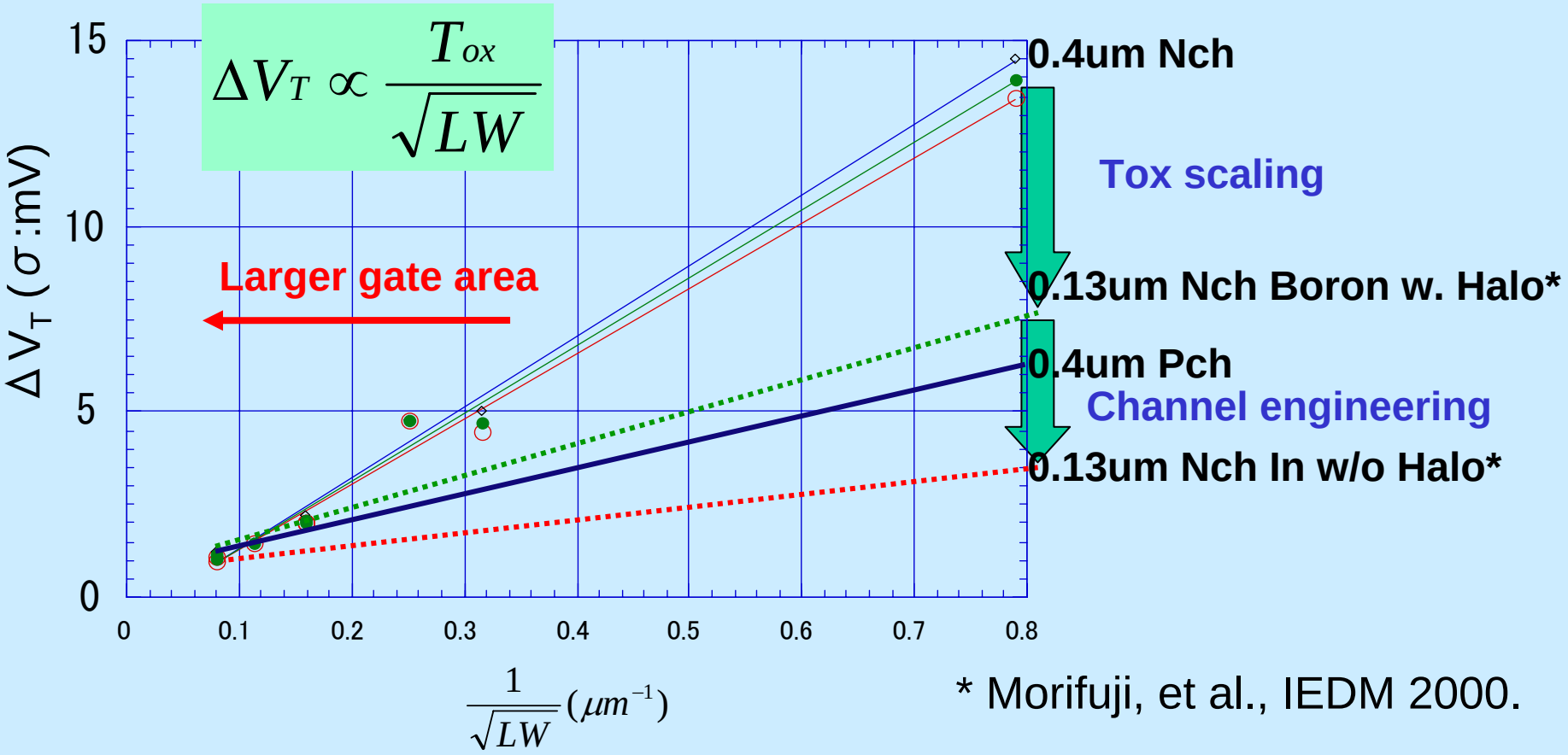
High frequency ckt. with scaled device is strongly affected from parasitic.
Circuit optimization with layout and parasitic effect is needed.

SIM w/o parasitic C → **SIM with parasitic C** → **Optimized with parasitic C**



Transistor issue: V_T mismatch

Larger gate area is needed for small V_T mismatch.
Scaling and proper channel structure can improve this.



* Morifuji, et al., IEDM 2000.

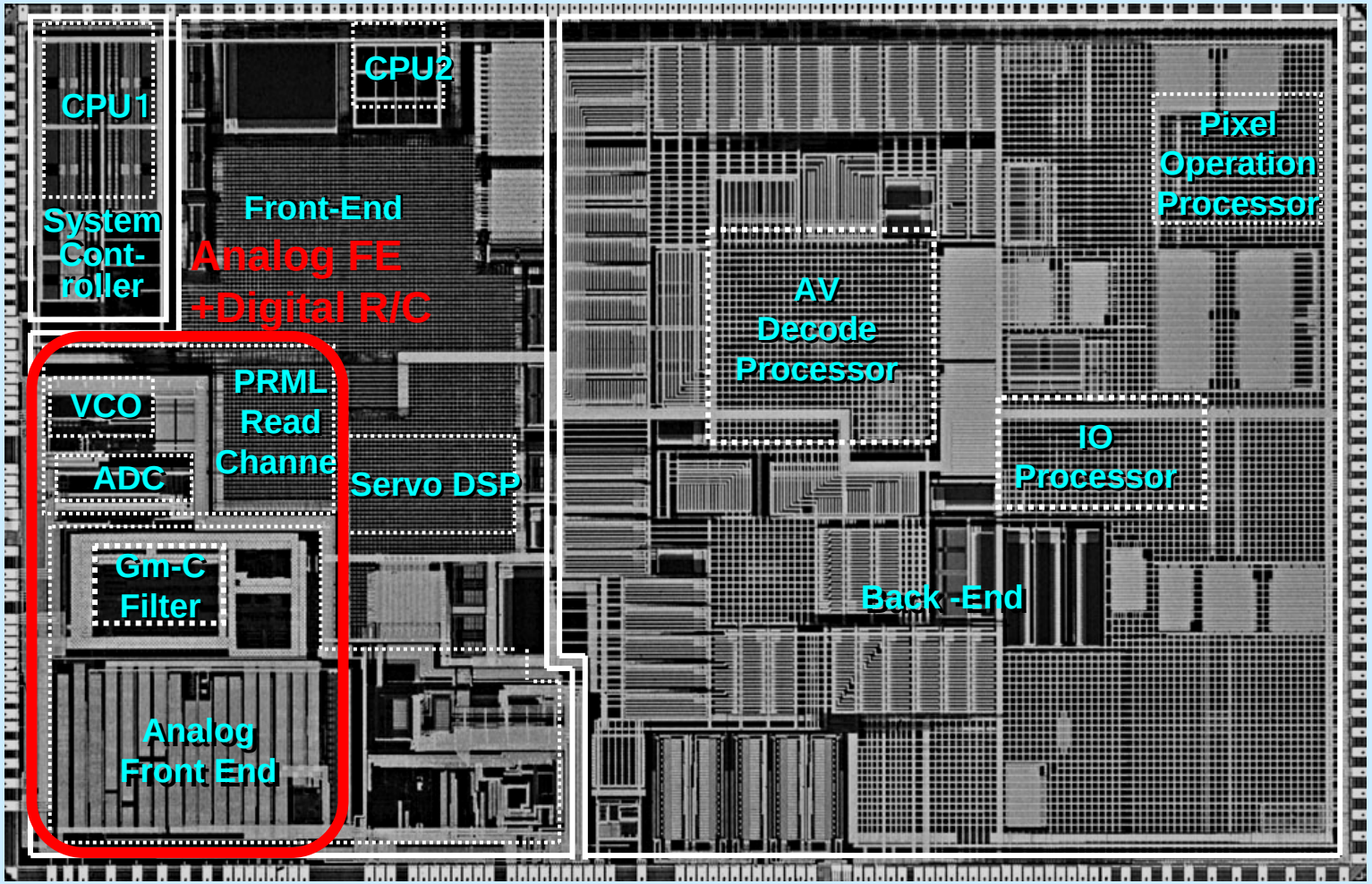
Development strategy and design system for mixed signal SoC

Full DVD system integration in 0.13um tech.

Advanced mixed signal SoC has been successfully developed.

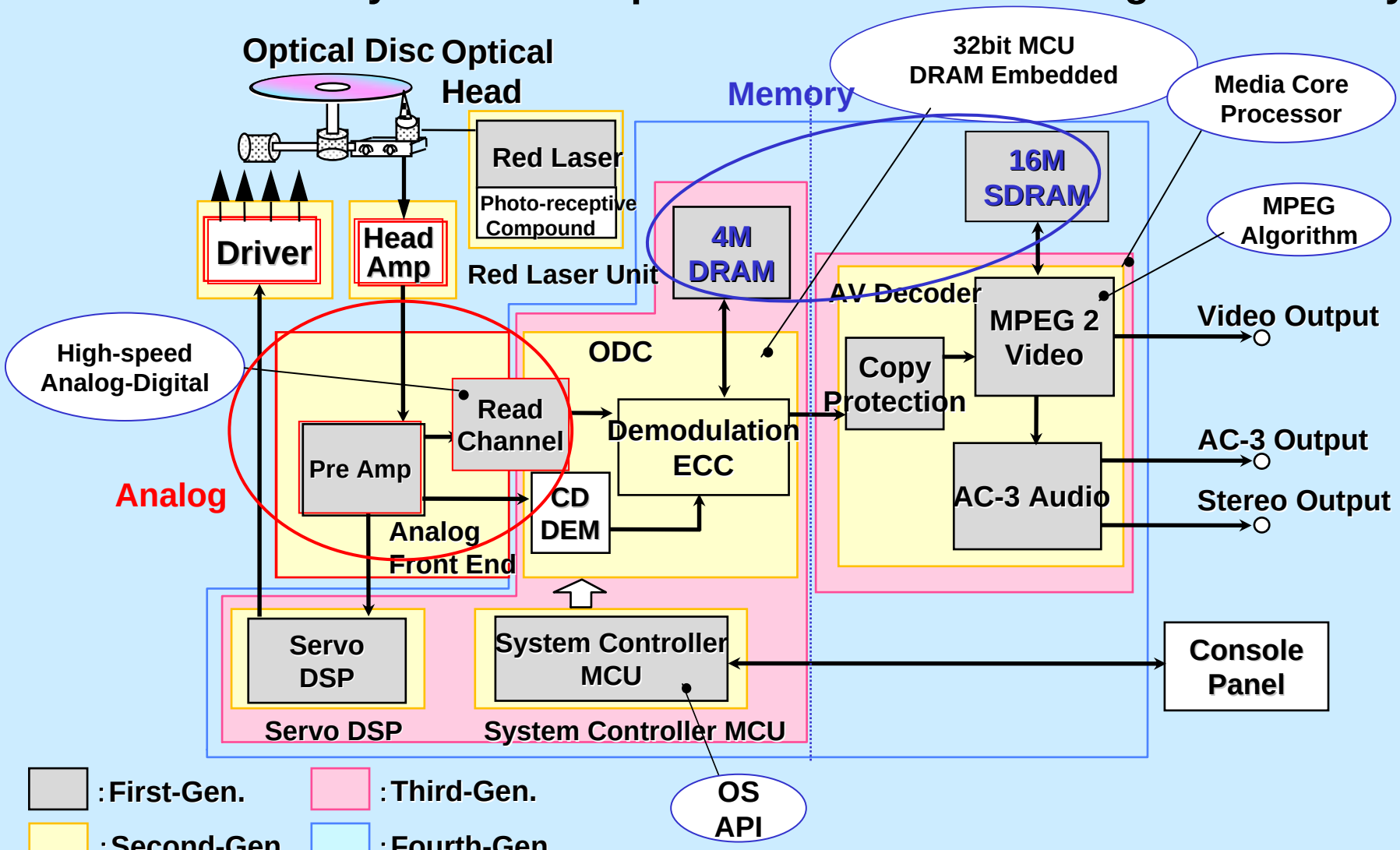
Okamoto, et al., ISSCC 2003

0.13um, Cu 6Layer, 24MTr



System: DVD player

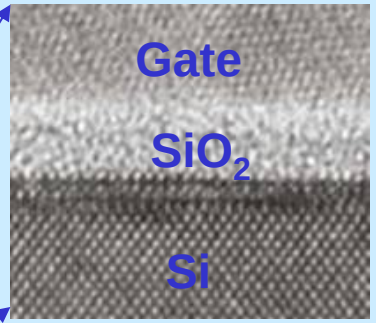
Current electrical system is complicated and needs analog and memory.



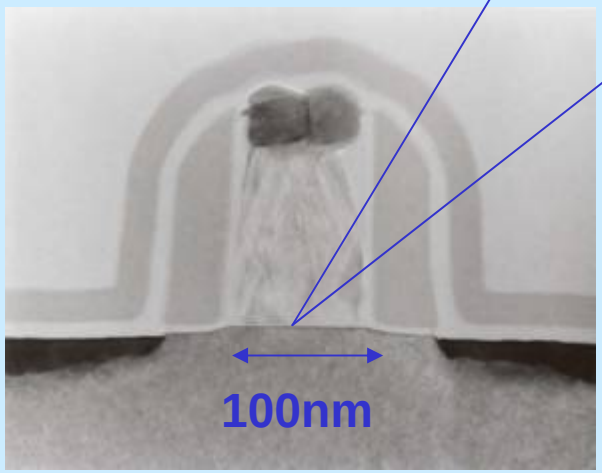
Scaled CMOS technology

Current Scaled CMOS technology is very artistic.

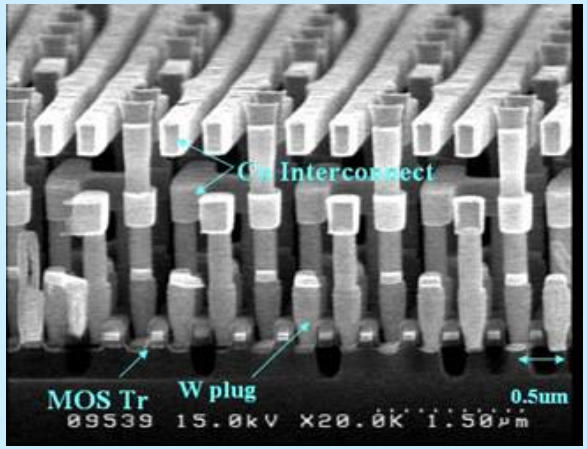
Matsushita's 0.13um CMOS technology



Seven lattices



Transistor



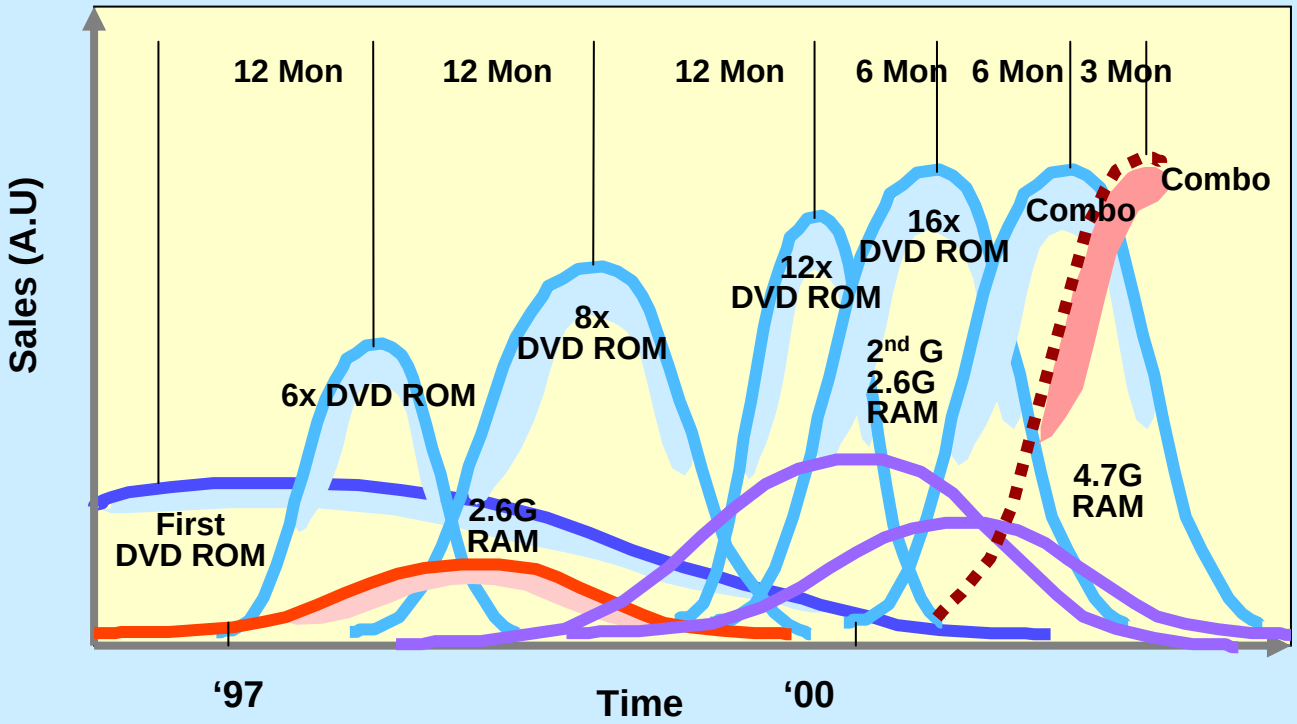
Cu Interconnection

Development strategy and system

Product time slot is narrow and development cost is huge.

Conventional analog LSI needs 2 or 3 re-designs.
This can not be accepted to mixed signal SoC

Advanced development strategy and design system must be established.

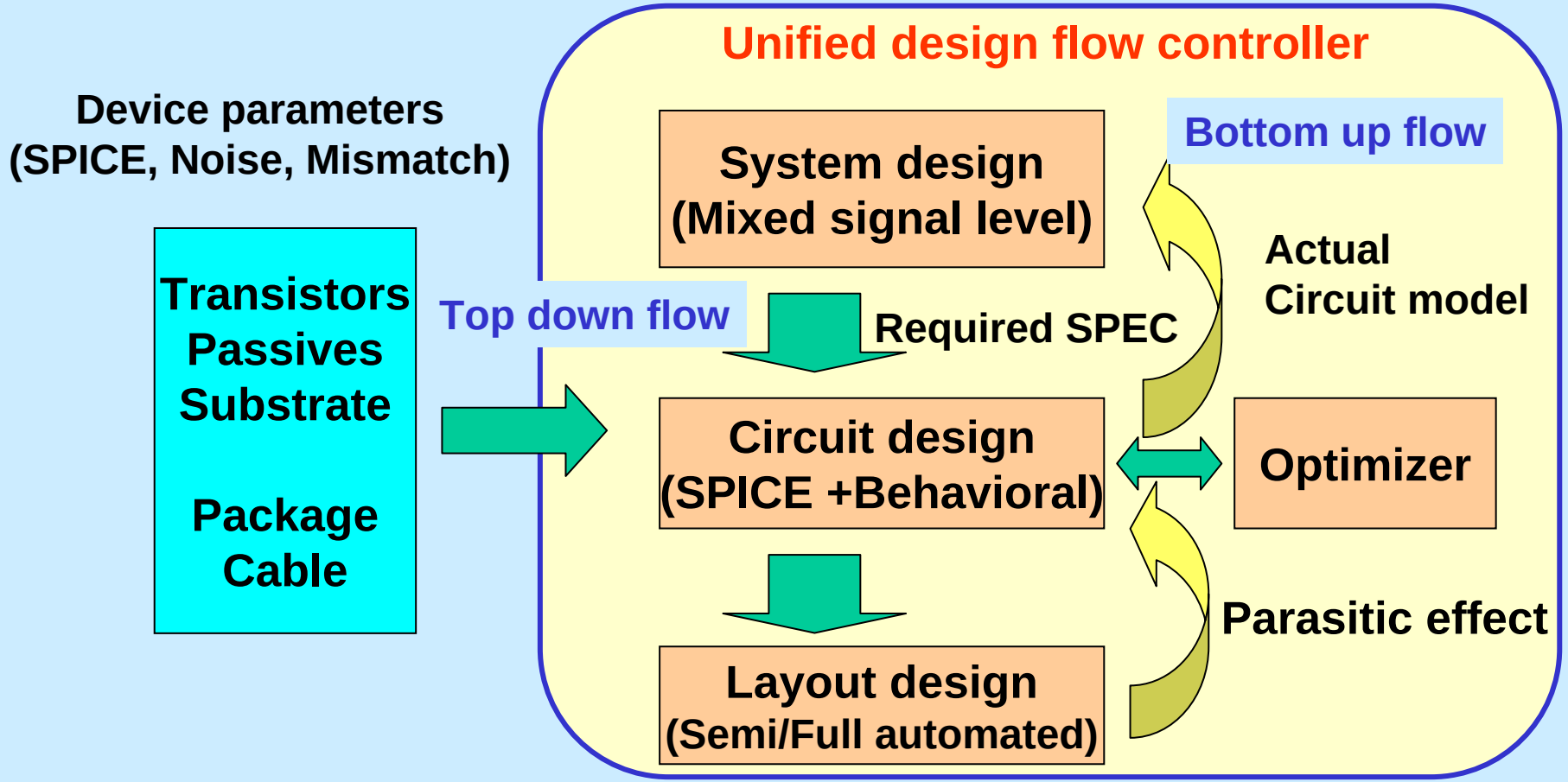


Strategy for the mixed signal SoC

- **System design**
  - **Digital calibration** for analog adjustment and unknown parameters.
  - **System optimization** to reduce analog area and increase robustness.
- **System verification**
  - Fast and accurate **mixed signal system simulator** with behavioral model to verify and optimize the mixed signal system.
  - Create the **target performance** for circuit blocks.
- **Circuit design**
  - **Ultra fast and accurate circuit simulation for P.V.T** and fluctuation analysis to verify the performance and robustness.
  - **Circuit optimizer** to find the sweet spot of the circuit.
  - **Automated creation of analog behavioral model** for system sim.
- **Process and device development**
  - Develop suitable **analog option device**
  - Early **analog parameter extraction** (mismatch, temp. and voltage chara.)
  - **Monitor and control** the analog parameters in Fab.

Design flow for mixed signal SoC

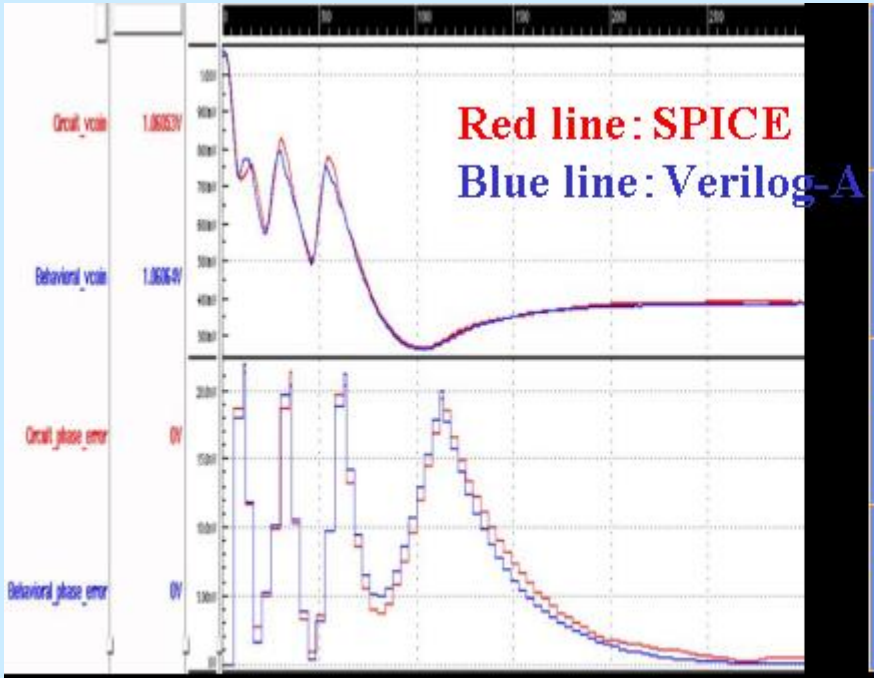
Design flow from System to layout with top down and bottom up process should be used for designing mixed signal SoC.
Accurate and a variety of device parameters is an another key.



Multi-language simulation

Multi-language simulation is 56x faster than SPICE with same accuracy. This will contribute to shorter design TAT and higher design quality.

SPICE+Verilog D+Verilog A

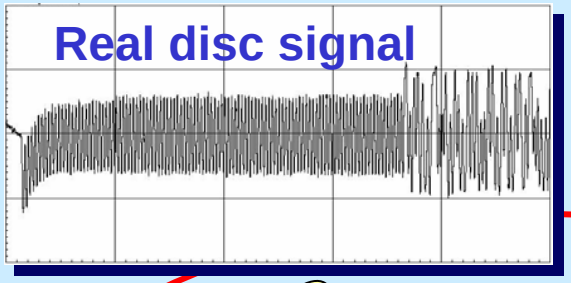


Description	Option	Time	CPU Time (s)	Speed Ratio
PLL Behavioral Lev (Verilog-A+SPICE)		9 min	545	56
PLL Circuit Level (Spice)	Model Opt.	2 hr 12 min	7939	3.8
PLL Circuit Level (Spice)		8 hr 27 min	30414	1

Mixed signal system design

Needs mixed signal Simulation for total signal processing.

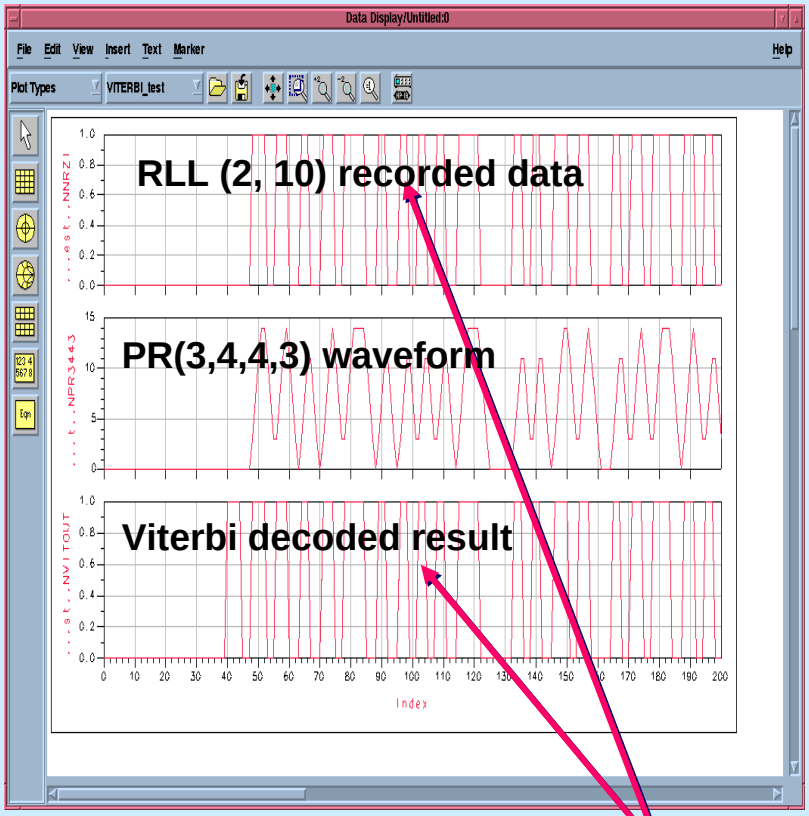
Many parameters and processing methods should be optimized.



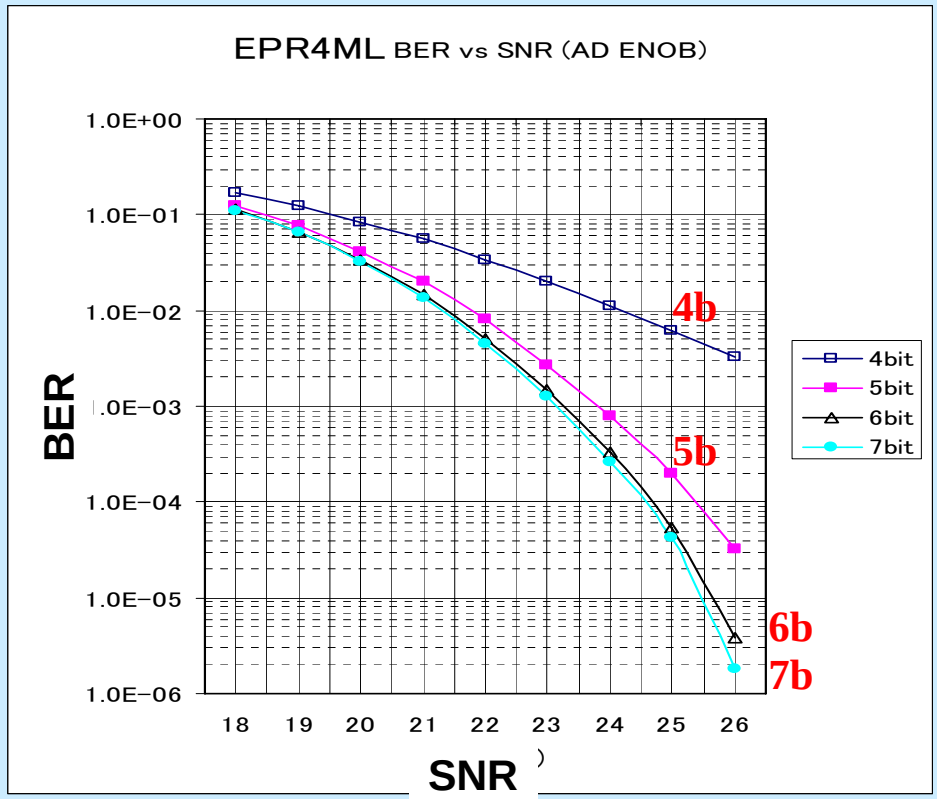
Finally, system is checked by real disc signals.

System simulation

Perfection of the mixed signal system should be verified and optimized by system simulation.



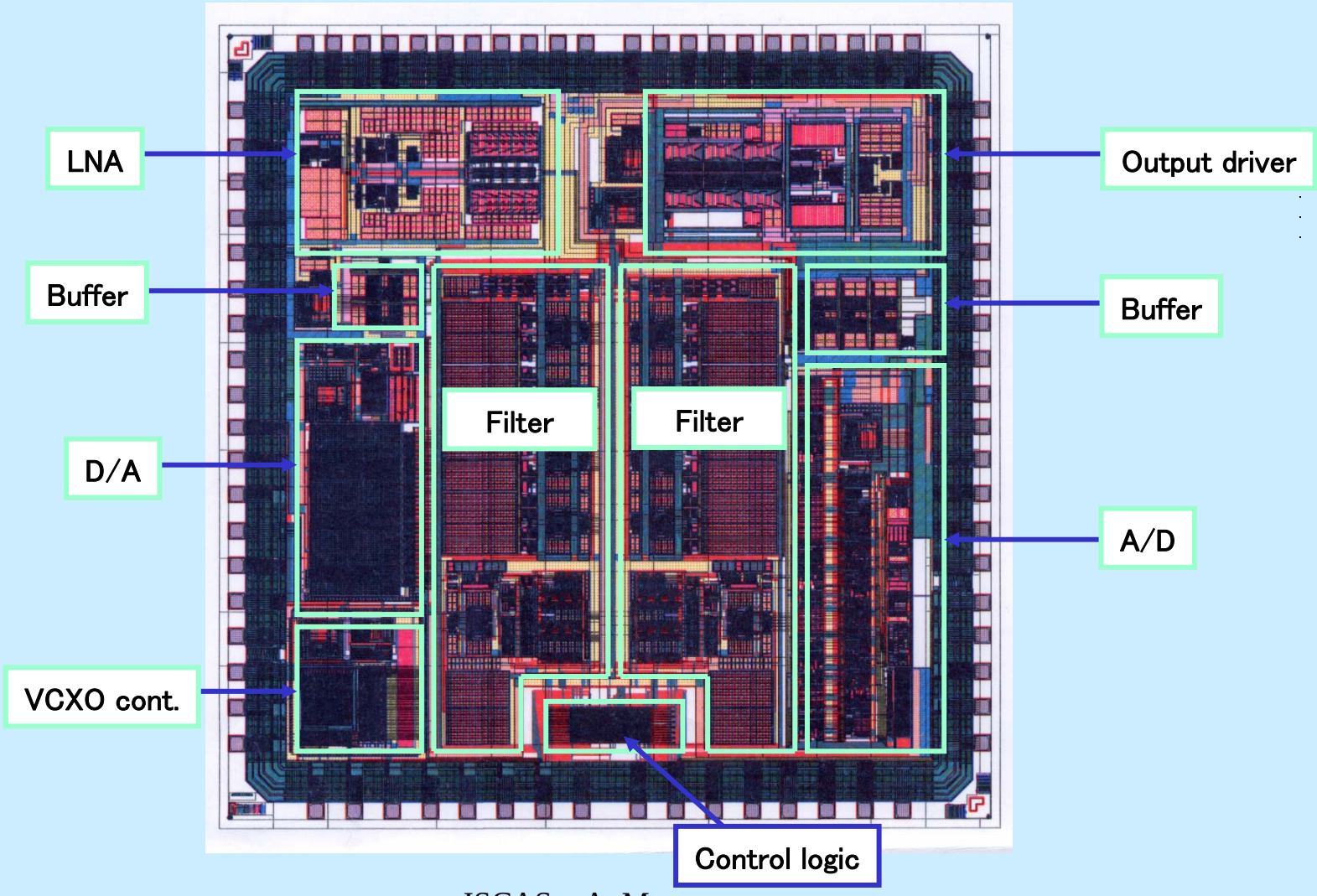
ADC resolution effect



System verification

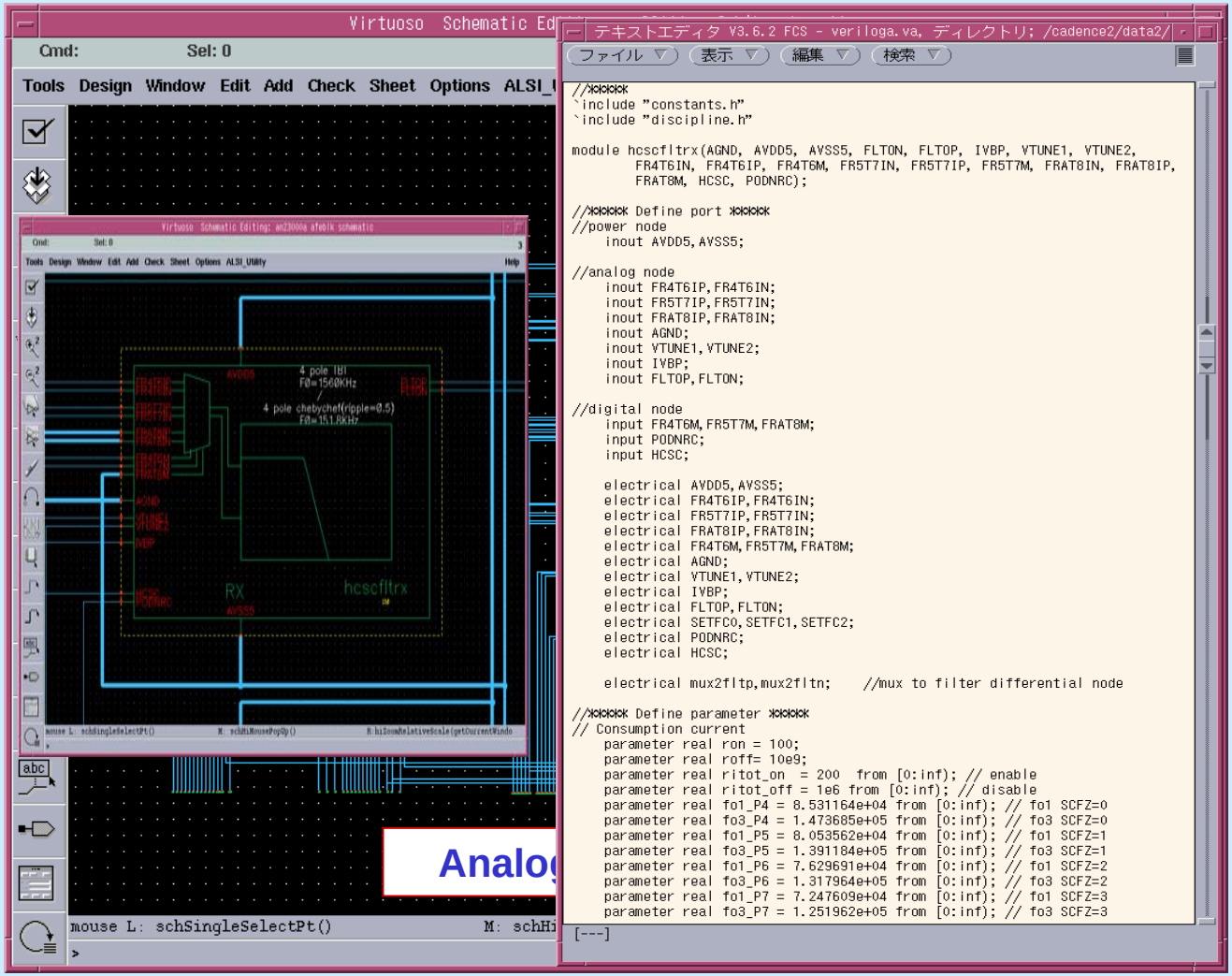
LSI design using behavioral language

Example: Analog Front End chip for ADSL system.



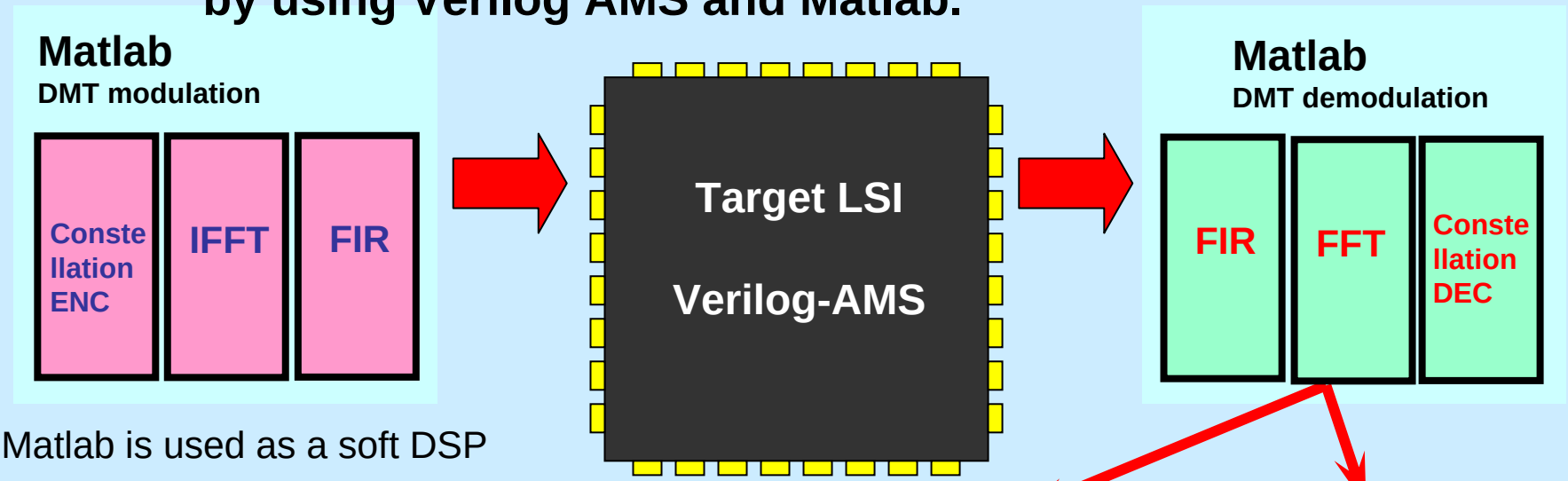
Hierarchical and behavioral system design

System should be described in behavioral language, hierarchically.

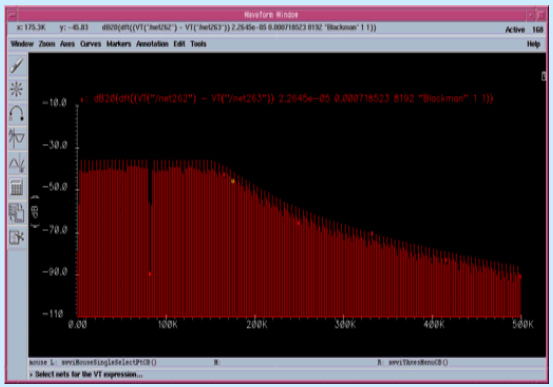


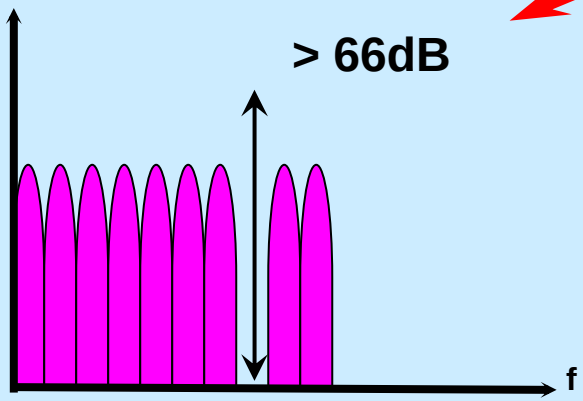
Virtual System test using Verilog AMS and Matlab

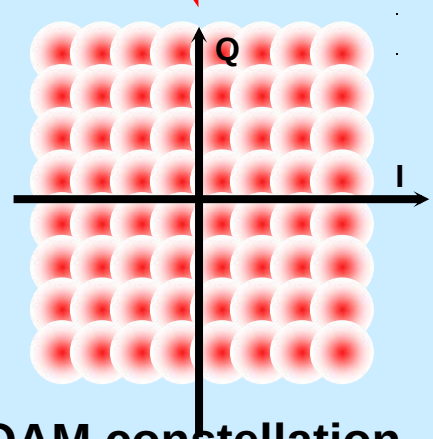
We can test the designed mixed signal system virtually, by using Verilog AMS and Matlab.



Matlab is used as a soft DSP





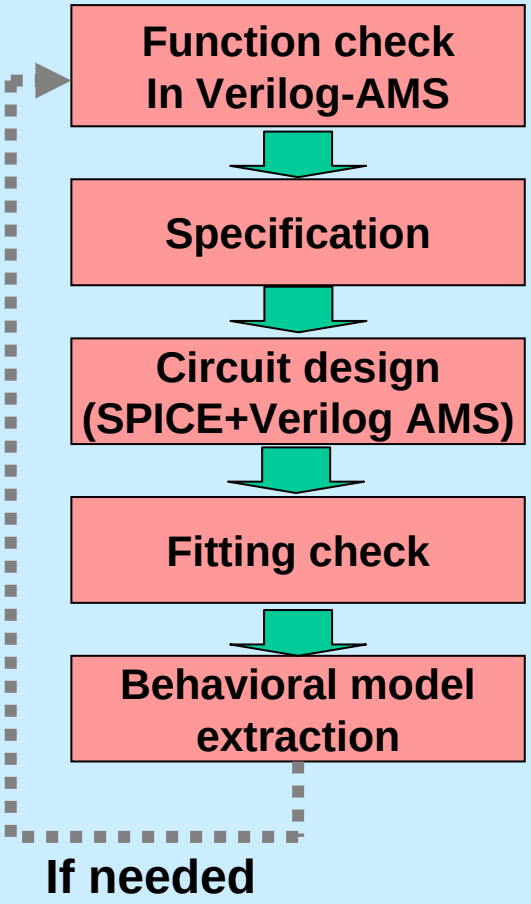


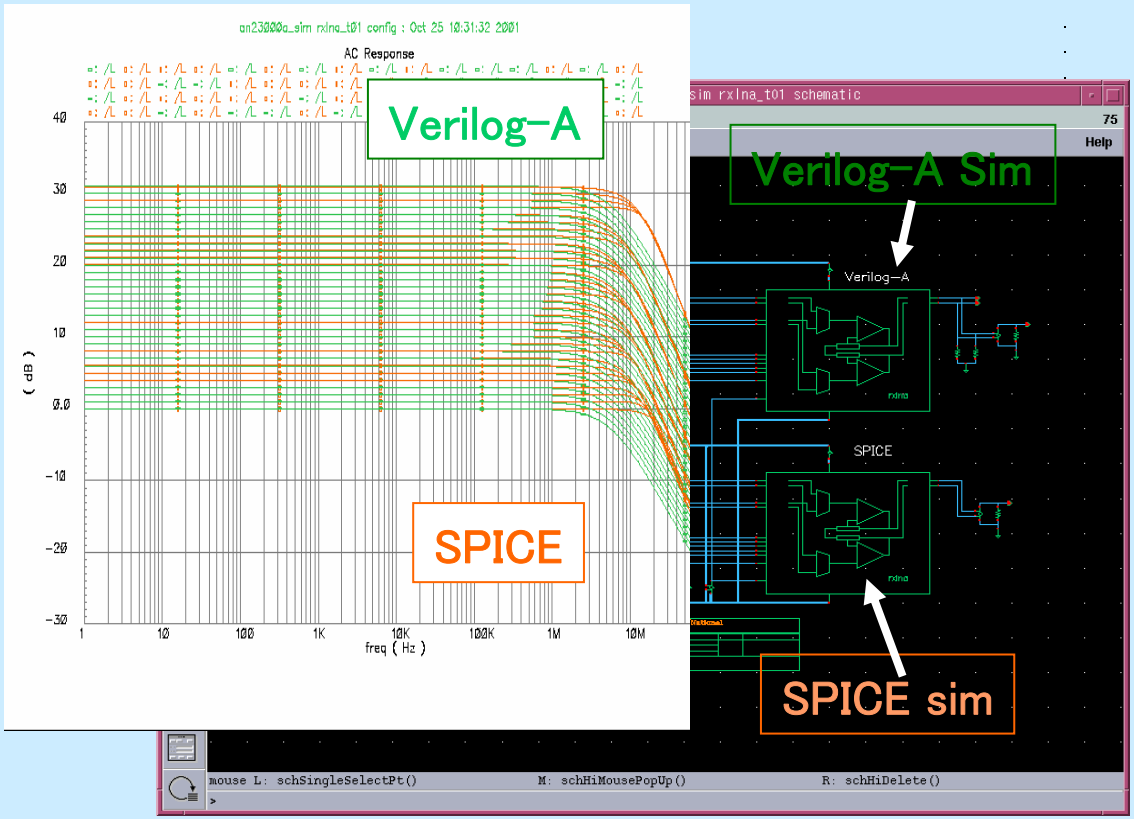
MTPR TEST (DMT Carrier hole)

QAM constellation

Fitting between behavioral and Spice

The combination of Verilog AMS and SPICE assures system perfection.



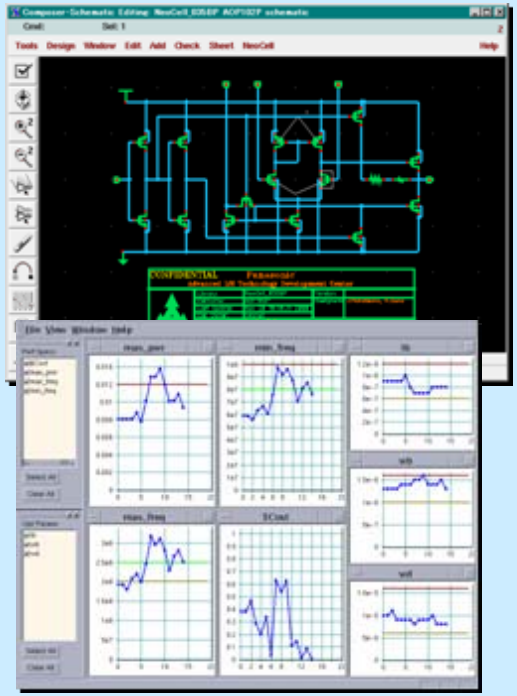


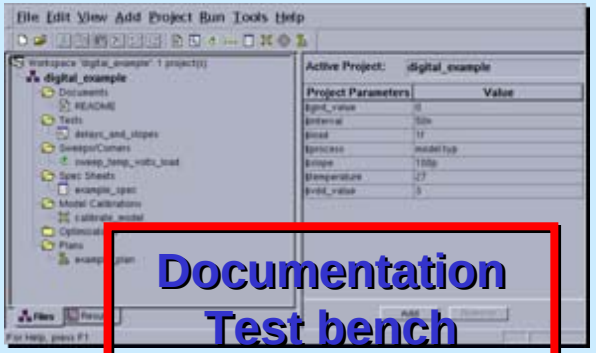
Unified mixed signal circuit simulator

New design system can increase design speed, 10x to 50x.

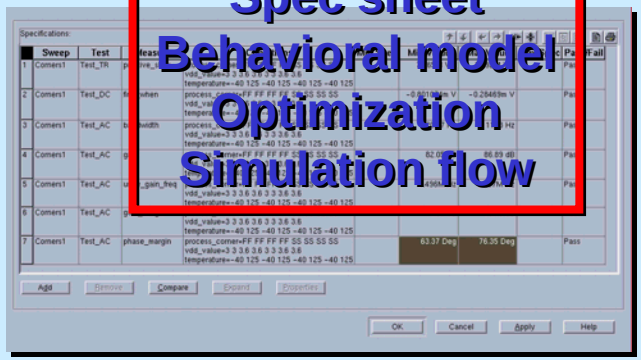
System level → *Specification* → **Optimization** → *Simulation Results* → **Design flow controller**

Verilog-AMS
+SPICE



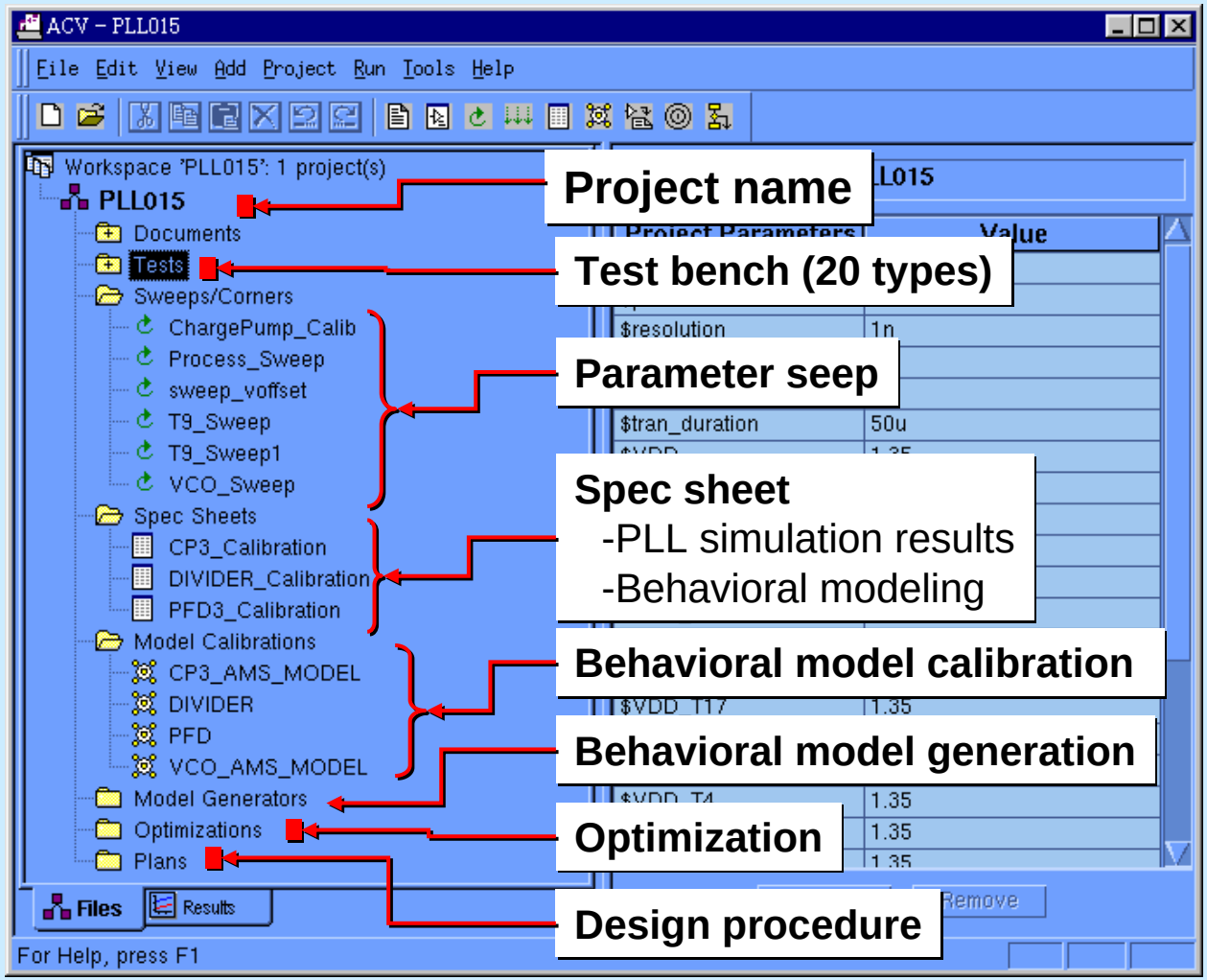


Documentation
Test bench
PVT analysis
Spec sheet
Behavioral model
Optimization
Simulation flow



Controller for automated simulation

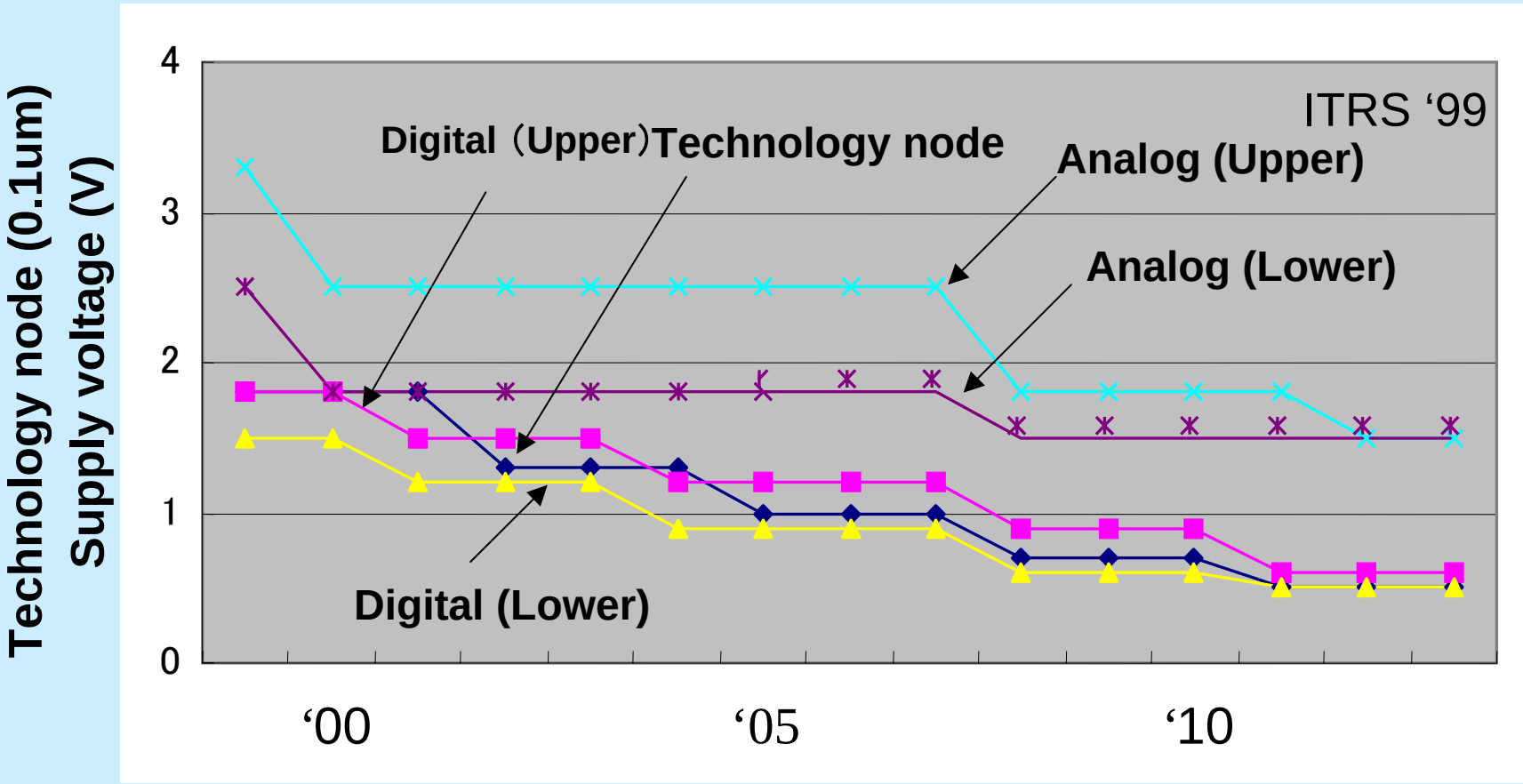
Simulation controller enables fast and automated simulation steps



Issues of mixed signal SoC

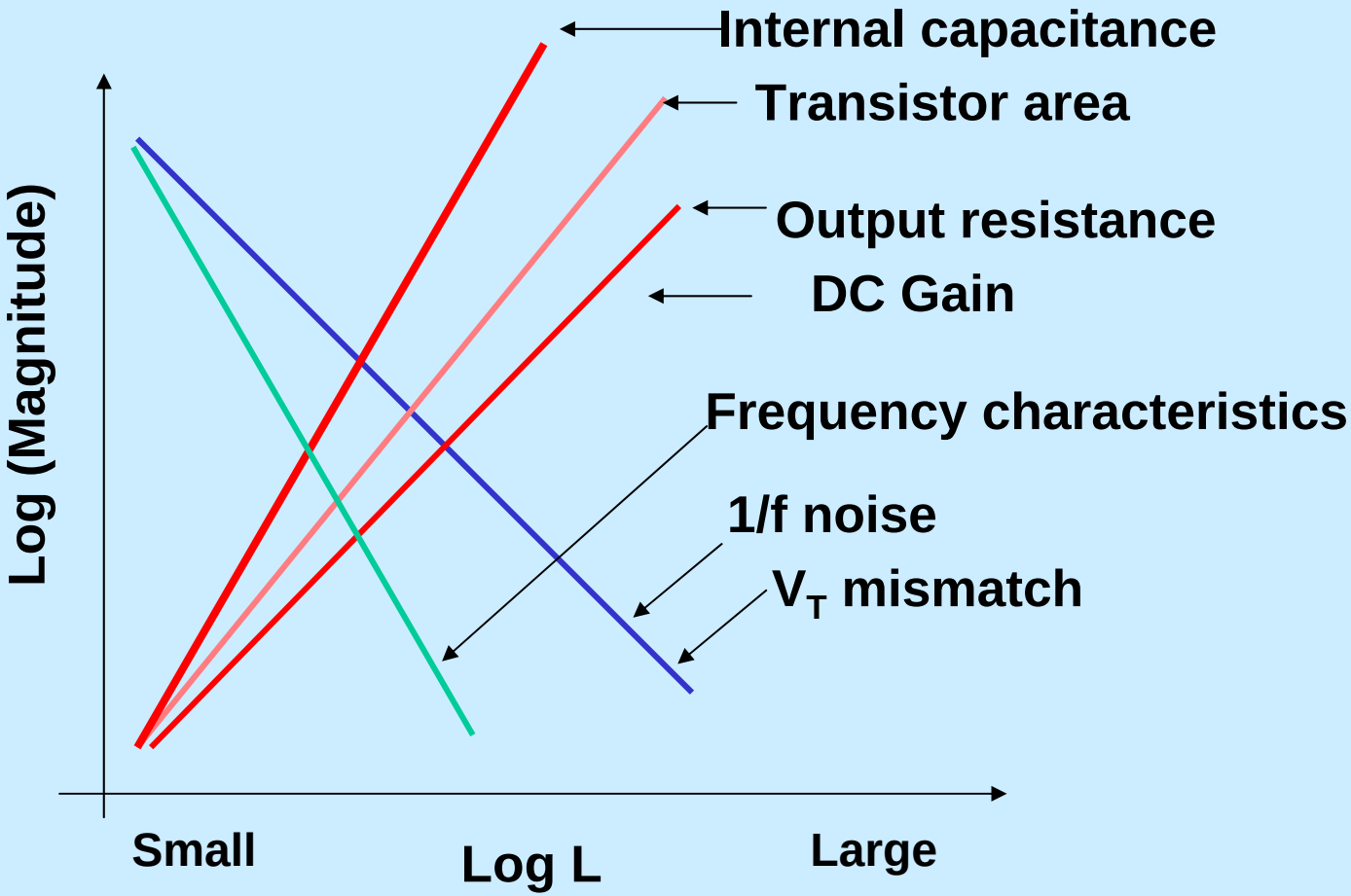
V_{dd} and CMOS scaling limits in analog

Lowest analog operating voltage must be 1.2V -1.8V.
Thus 0.18um – 0.13um must be a scaling limit for analog.
This results in salutation of f_T and area reduction.



Optimization in channel parameters

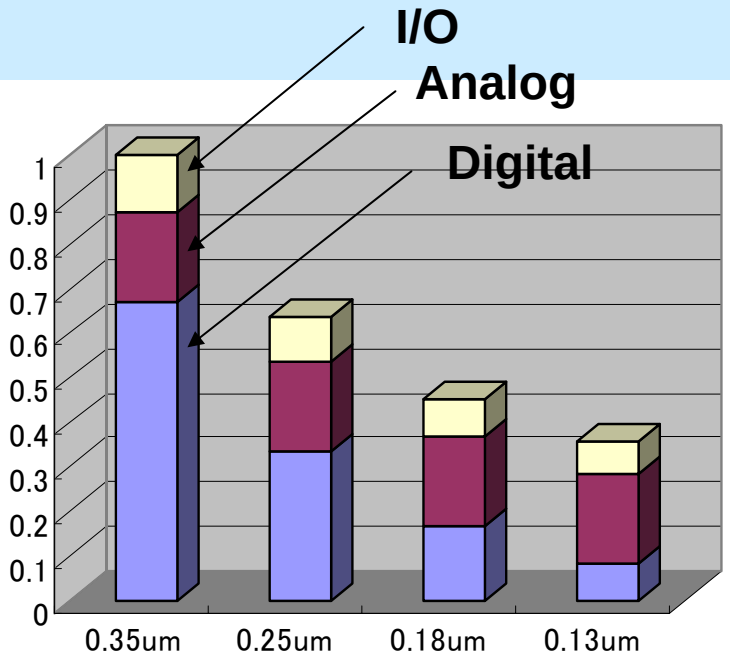
Larger gate length is needed for small mismatch and small noise circuit. However, this results in increase of cost and decrease of performance.



Cost up issue by analog & I/O

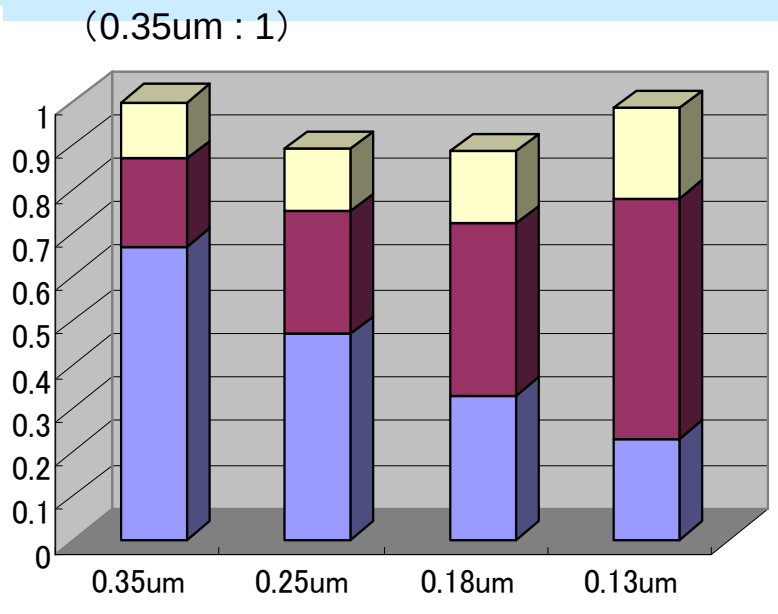
Cost of mixed A/D LSI will increase when using deep sub-micron device, due to the increase of cost of non-scalable analog and I/O parts.

Large analog on SoC must be unacceptable in near future.



Chip area

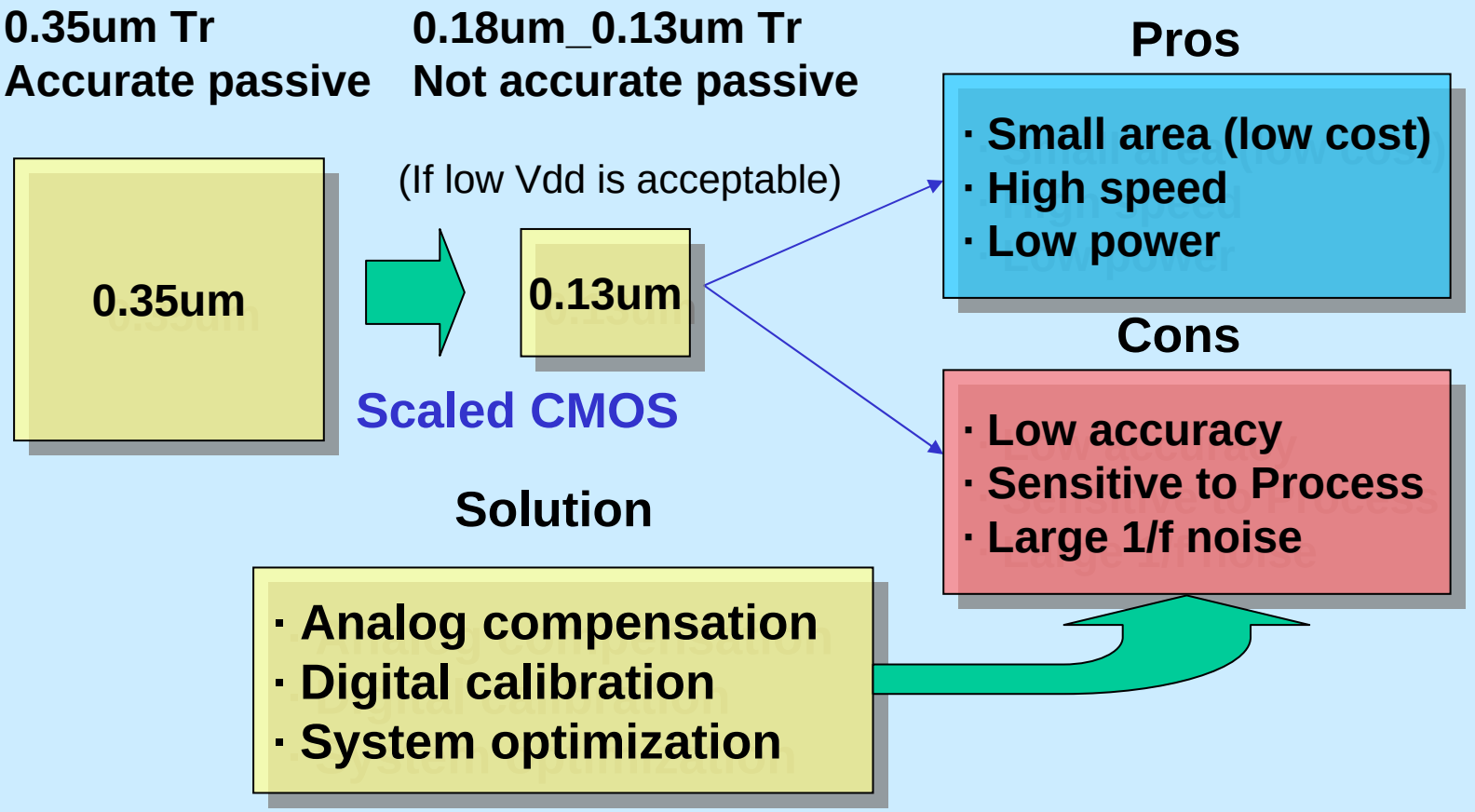
Wafer cost increases 1.3x for one generation



Chip cost

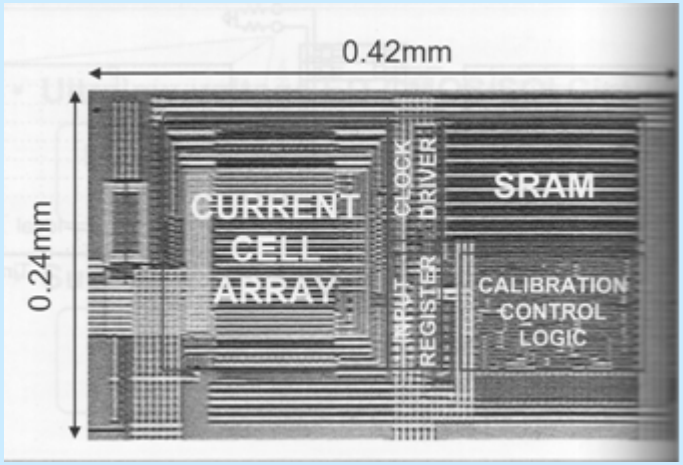
Solution 1: Scaled CMOS and use of digital

Use scaled CMOS and not accurate passives.
Address the issues by M/S compensation and system optimization.



Example: Analog+ digital calibration tech.

Area and power are reduced drastically, by scaled CMOS and digital tech.



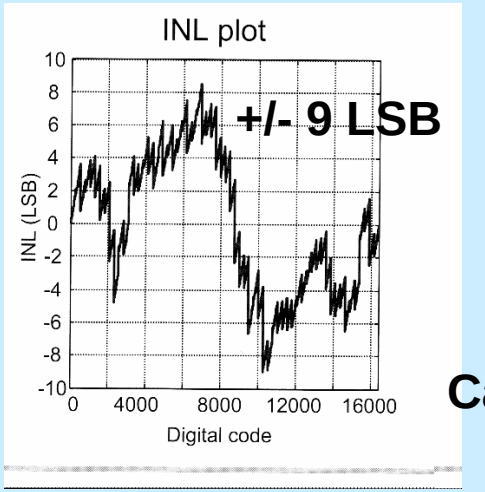
Y. Cong and R. L. Geiger, Iowa state university, ISSCC 2003

14b 100MS/s DAC

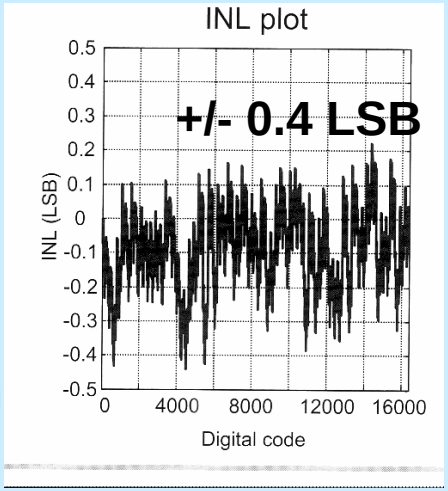
1.5V, 17mW, 0.1mm^2, 0.13um

0.5 LSB INL,

SFDR=82dB at 0.9MHz, 62dB at 42.5MHz



Calibration



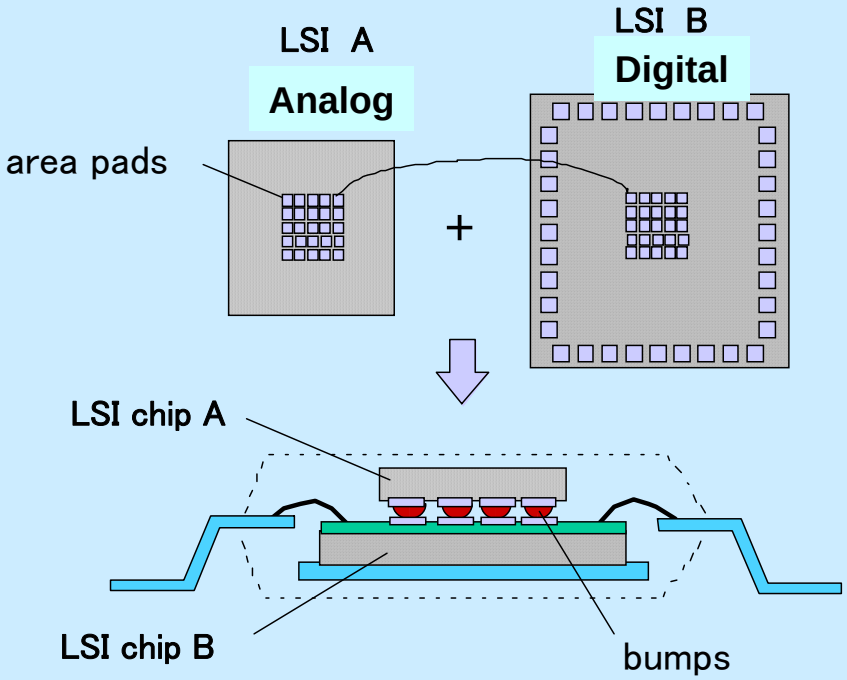
Area: 1/50

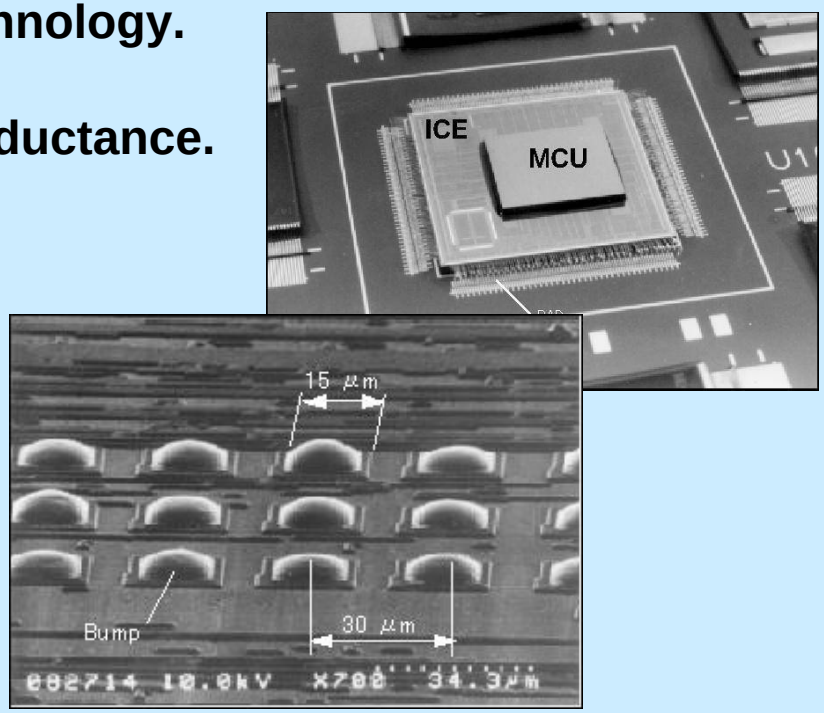
Pd: 1/20

Solution 2: Advanced packaging technology

Some advanced packaging technologies will give the solution.

Analog: using not so much scaled technology.
Digital: using scaled technology
Connect with low parasitic cap. and inductance.





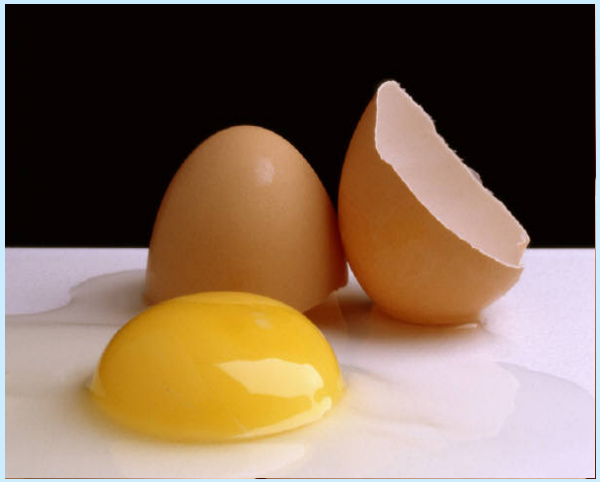
Chip On Chip technology

Same capacitance
as on-chip interconnection.
No interconnection inductance

Future step: Mixed signal egg.

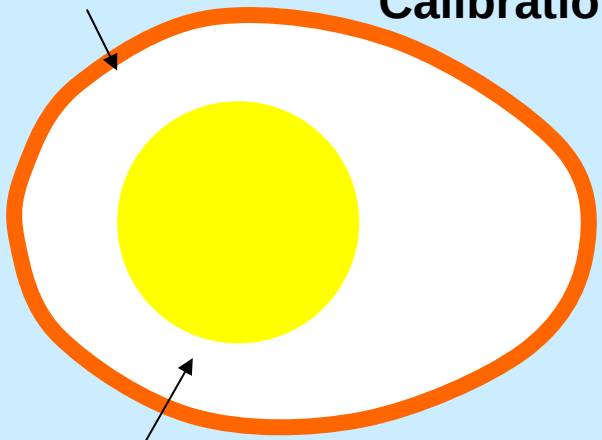
Analog helps digital (digital network and storage…).
Next step is digital must help analog.

Mixed signal egg (Analog yolk and white with digital shell)



Digital shell

Sustain the analog egg.
Calibration and adjustment.



Analog yolk and white

Ultra-low power signal processing **(Weak inversion)**
Ultra-high speed signal processing

But, very delicate and fancy

Summary

- The mixed signal (Analog+Digital) is essential for almost all the systems. Not analog only, not digital only.
- Effective modeling of analog parts and high speed concurrent simulation with digital is vital for design.
- CMOS is very powerful technology for analog, as well as digital, but scaling limitation is reaching.
- The collaboration between analog and digital, and advanced packaging technology will bring us effective solutions.