

# **Mixed signal SoC: A new technology driver in LSI industry**

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(Tokyo Institute of Technology, after this April)

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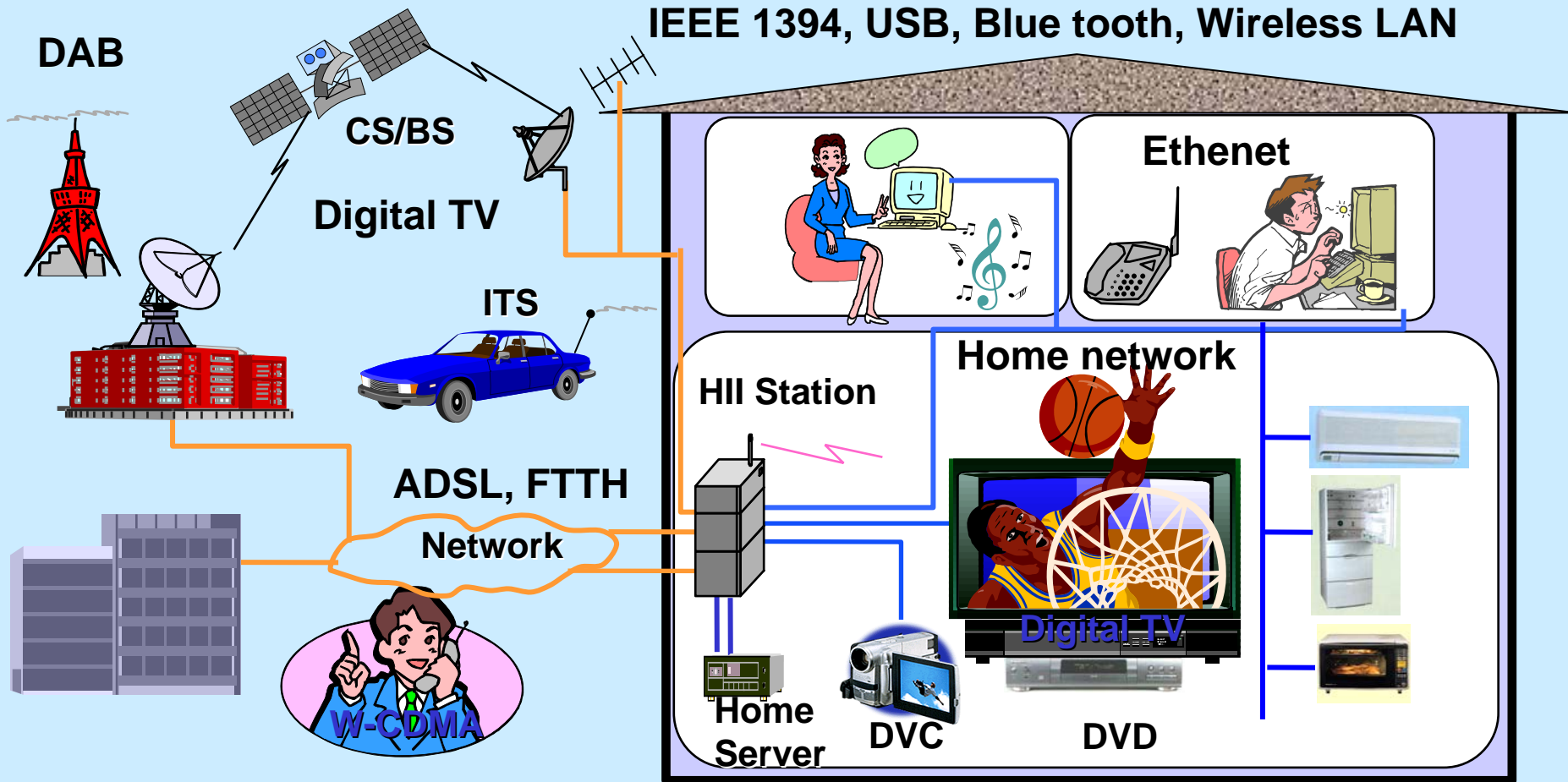
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- **Introduction**
- **Current electronics and mixed signal technology**
- **CMOS as an analog device**
- **Development strategy and design system for mixed signal SoC**
- **Issues of mixed signal SoC and solutions**
- **Summary**

# **Current electronics and mixed signal technology**

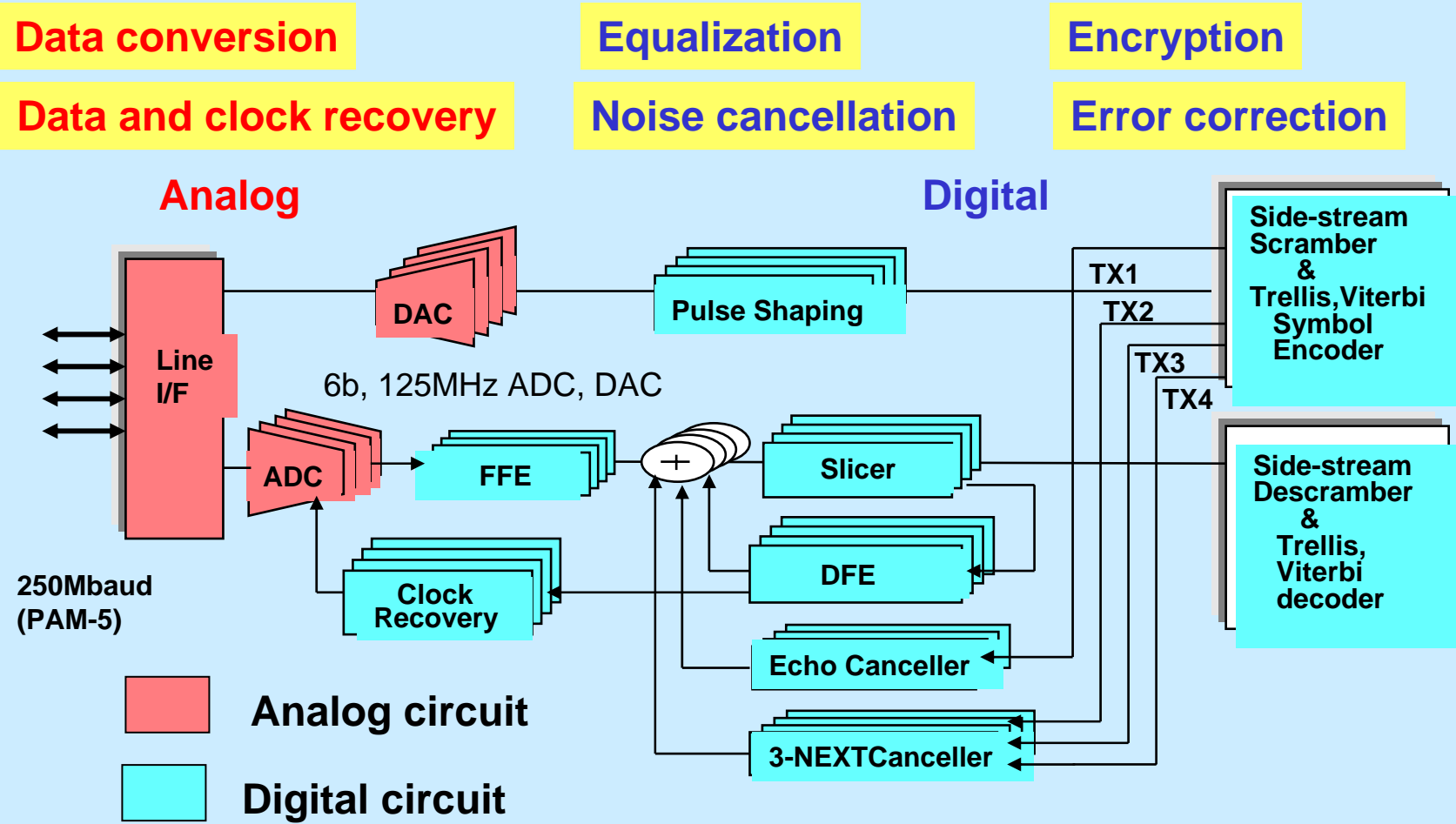
# Image of current electronics

Digital consumer electronics and networking drive current electronics.



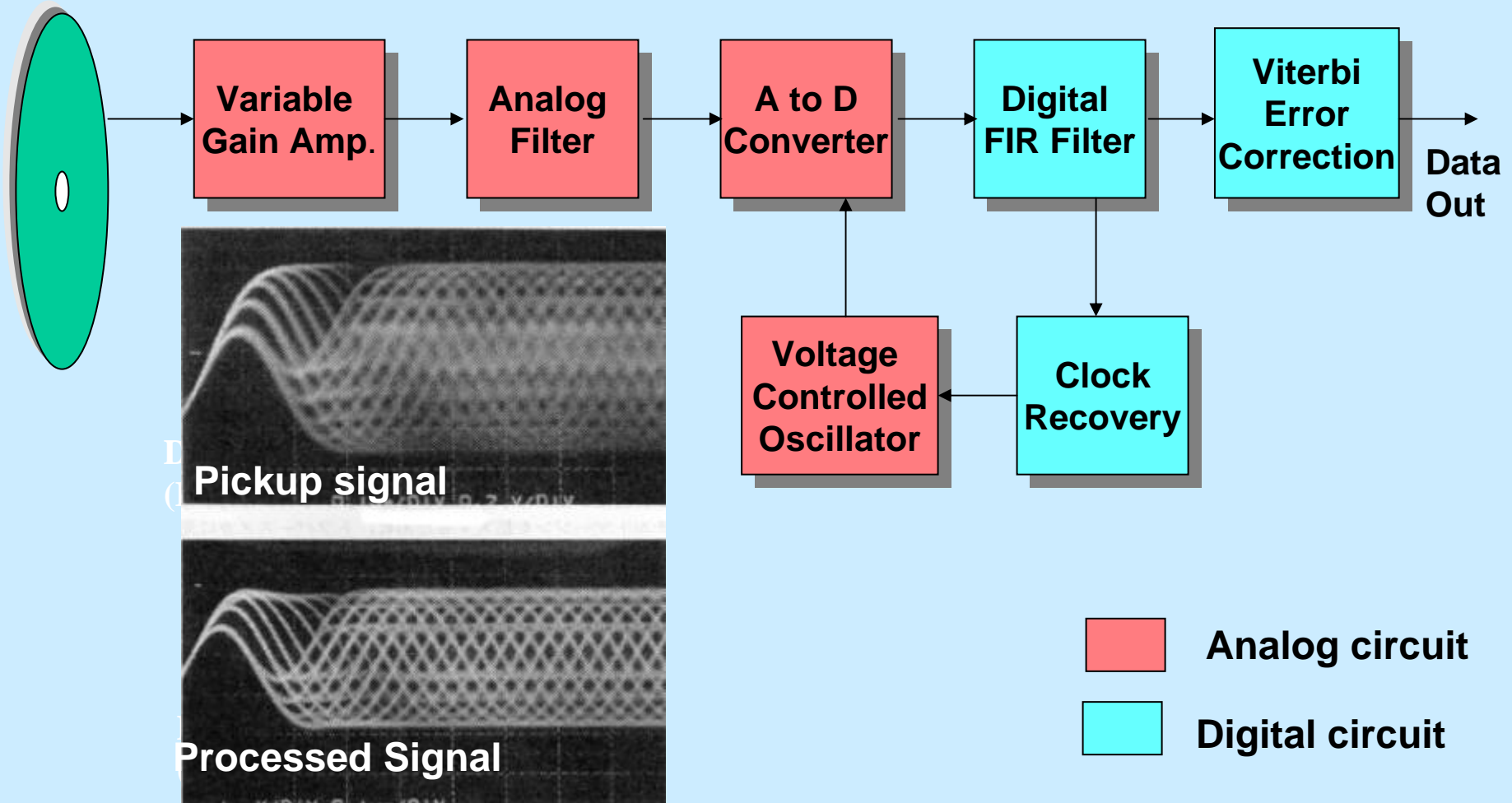
# Mixed signal technology :Digital networkings

Mixed signal technology enables high speed digital networking.



# Mixed signal tech. ; Digital read channel

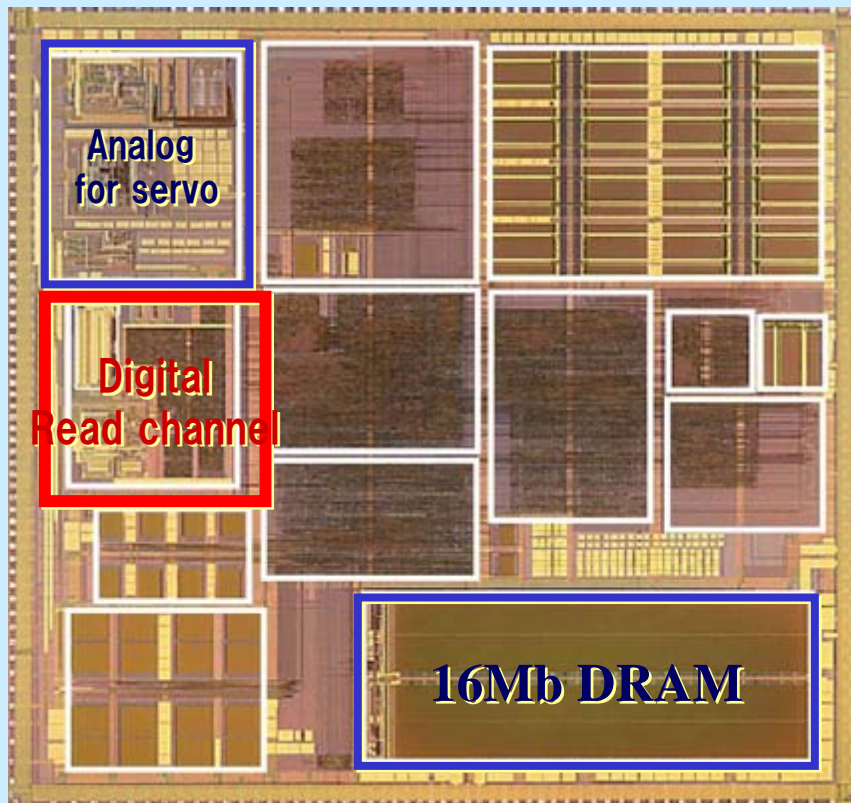
Digital storage also needs high speed mixed signal technologies.



# Mixed signal SoC for DVD RAM system

This enables high readability for weak signal from DVD RAM pickup.

World fastest and highly integrated mixed signal CMOS SoC



0.18um- eDRAM

24M Tr

16Mb DRAM

500MHz

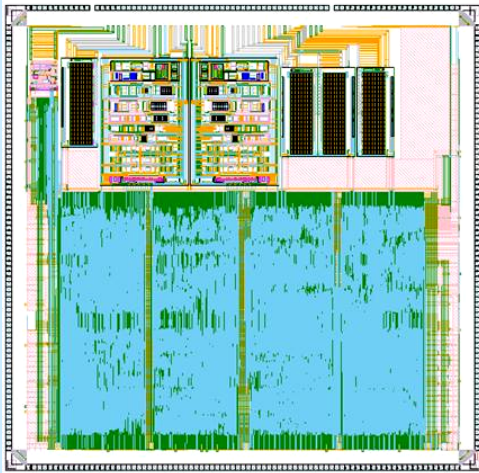
Mixed Signal

Goto, et al., ISSCC 2001

# Recent developed mixed signal CMOS LSIs

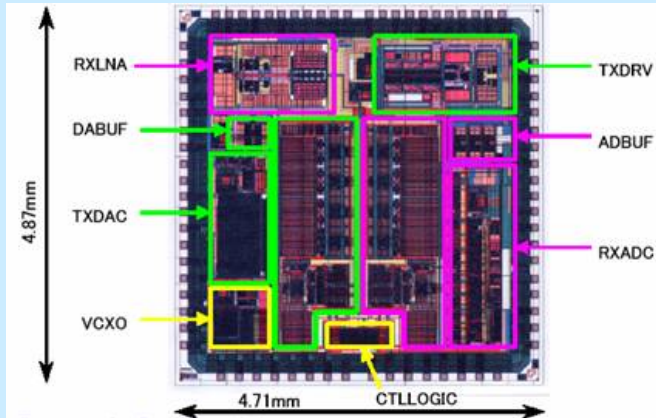
**5G RF LAN**

12b 50MHz ADC 2ch  
12b 50MHz DAC 2ch

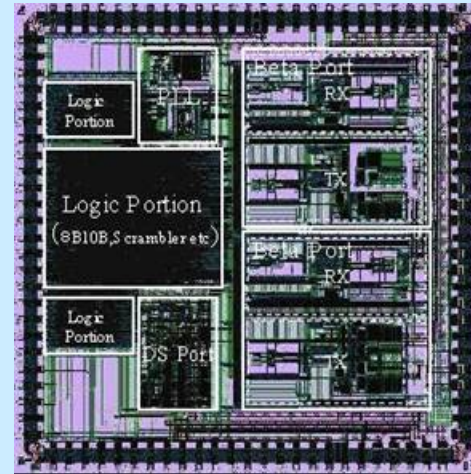


**AFE for ADLS**

12b 20MHz  
ADC+DAC



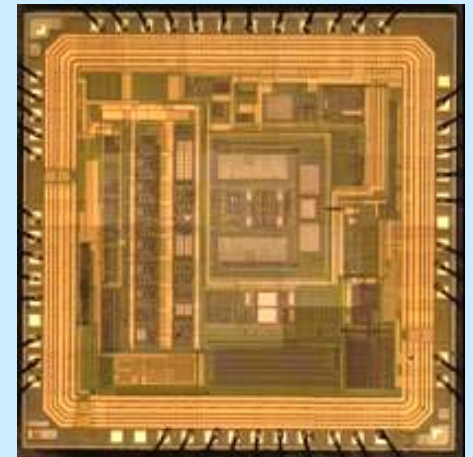
**Digital network  
1394b (1GHz)**



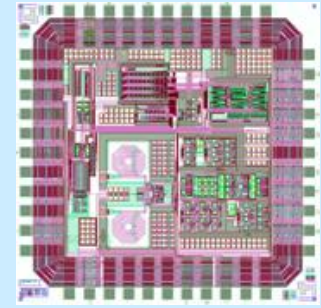
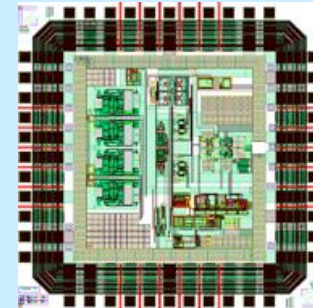
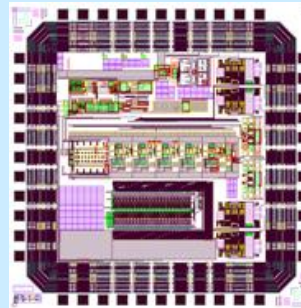
**AFE (Analog Front End)**

**AFE for Digital Camera**

12b 20MHz ADC+AGC



**2GHz RF CMOS**





# Application area in mixed signal CMOS tech.

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Almost all the products need mixed signal CMOS LSI tech.

## Wireless

Network  
Communication

- Cellular phone: PDC, W-CDMA
- RR-Net: Bluetooth, IEEE802.11
- Broad cast: STB, DTV, DAB

## Wired

Recording

- DVD, VDC, HDD

Output

- LCD, PDP, EL, Audio drive

Input

- Camera, Others

Power supply

- Switching supply, Every LSIs (On-chip)

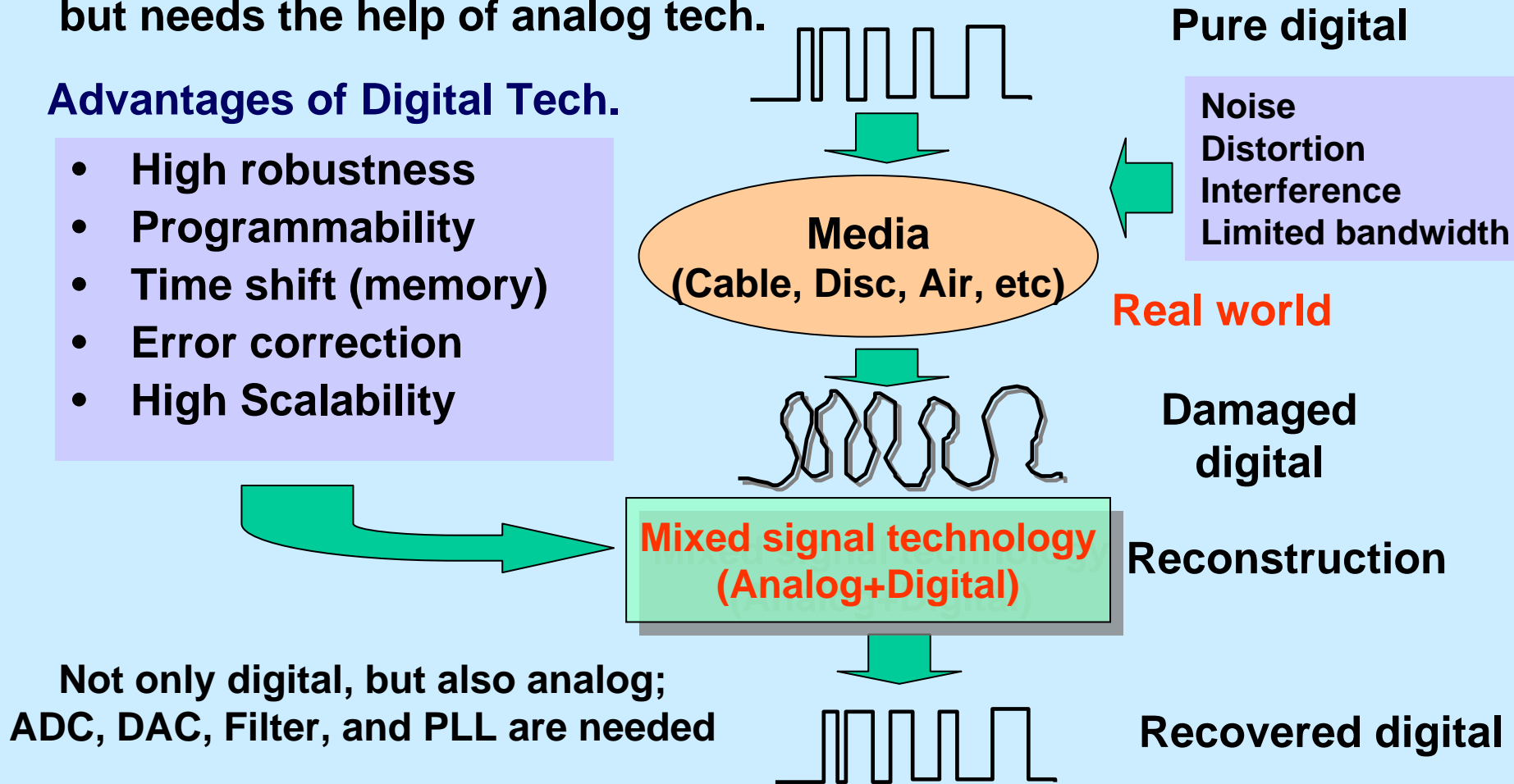
# Digital technology in real world

Digital signal suffers heavy damage in real world.

But, digital can address this issue by own advantages, but needs the help of analog tech.

## Advantages of Digital Tech.

- High robustness
- Programmability
- Time shift (memory)
- Error correction
- High Scalability



# Progress in A/D converter; video-rate 10b ADC

ADC is a key for mixed signal technology.

We have reduced the cost and power of ADC drastically;

**1/ 2,000 for Power and 1/200,000 for the cost!**

**CMOS technology attained it.**

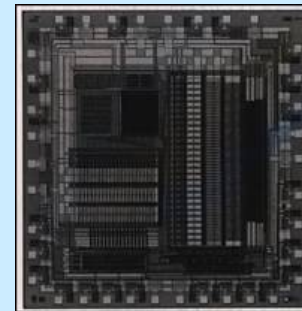
dulling past 20 years

1980	1982	1993	Now
Conventional product	World 1 <sup>st</sup> Monolithic	World lowest power	SoC Core
Board Level (Disc.+Bip)	Bipolar (3um)	CMOS (1.2um)	CMOS (0.15um)
20W	2W	30mW	10mW
\$ 8,000	\$ 800	\$ 2.00	\$0.04

Analog Devices Inc.



Our developed.

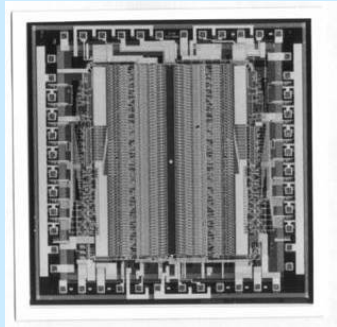


Our developed.



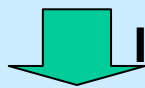
# Progress in high-speed ADC

High speed ADC has reduced its power and area down to be embedded.

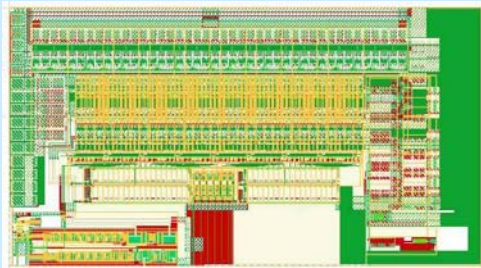


## World fastest 6b ADC

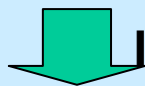
6b, 1GHz ADC    ISSCC 1991  
2W,  
1.5um Bipolar



## ISSCC 2000 World fastest CMOS ADC



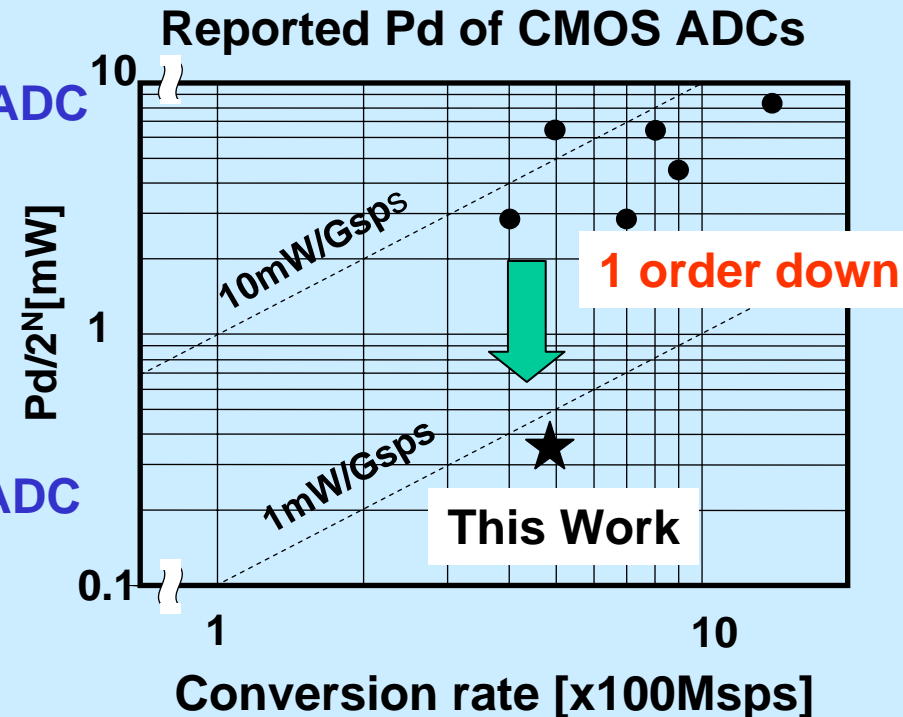
6b, 800MHz ADC  
400mW, 2mm<sup>2</sup>  
0.25umCMOS



## ISSCC 2002 World lowest Pd HS ADC



7b, 400MHz ADC  
**50mW, 0.3mm<sup>2</sup>**  
0.18umCMOS



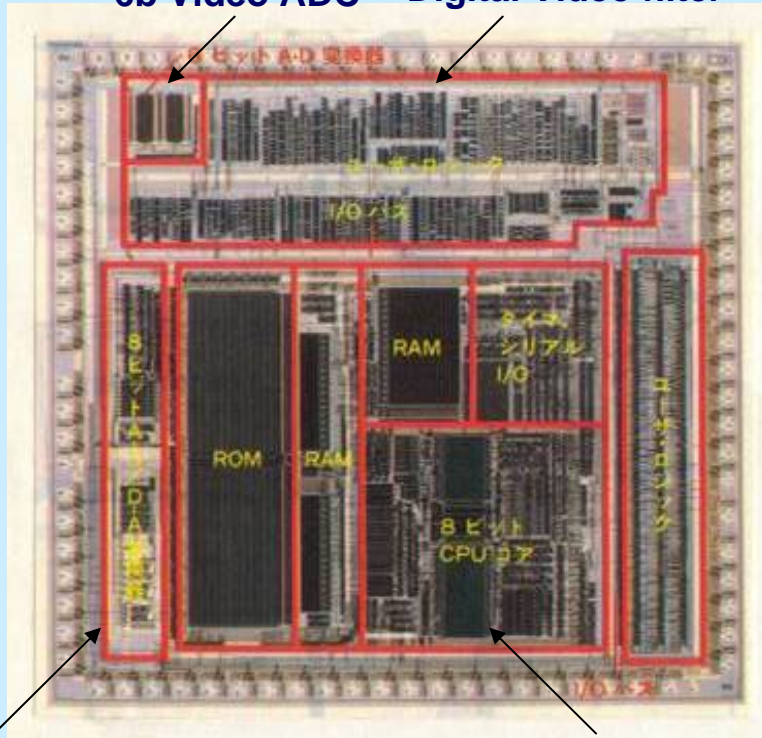
# Early stage mixed signal CMOS LSI for CE

Success of CMOS ADC and DAC enabled low cost mixed signal CMOS LSI. This also enabled low cost and low power digital portable AV products.

1993 Model: Portable VCR with digital image stabilizing



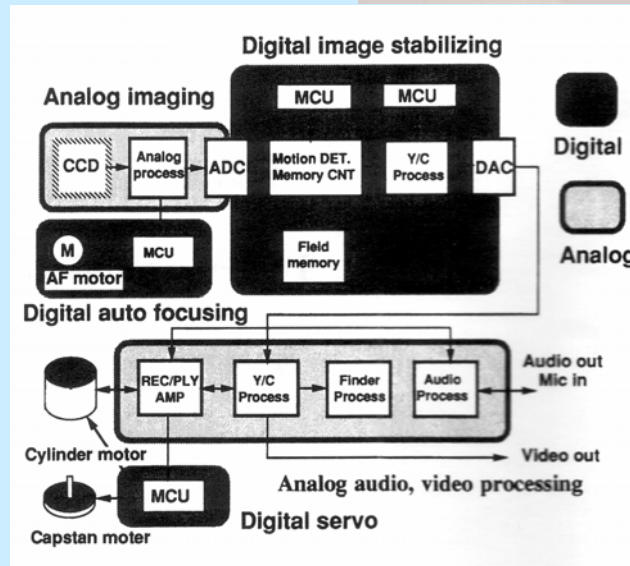
6b Video ADC    Digital Video filter



8b low speed ADC;DAC

8b CPU

System block diagram



# CMOS as analog device

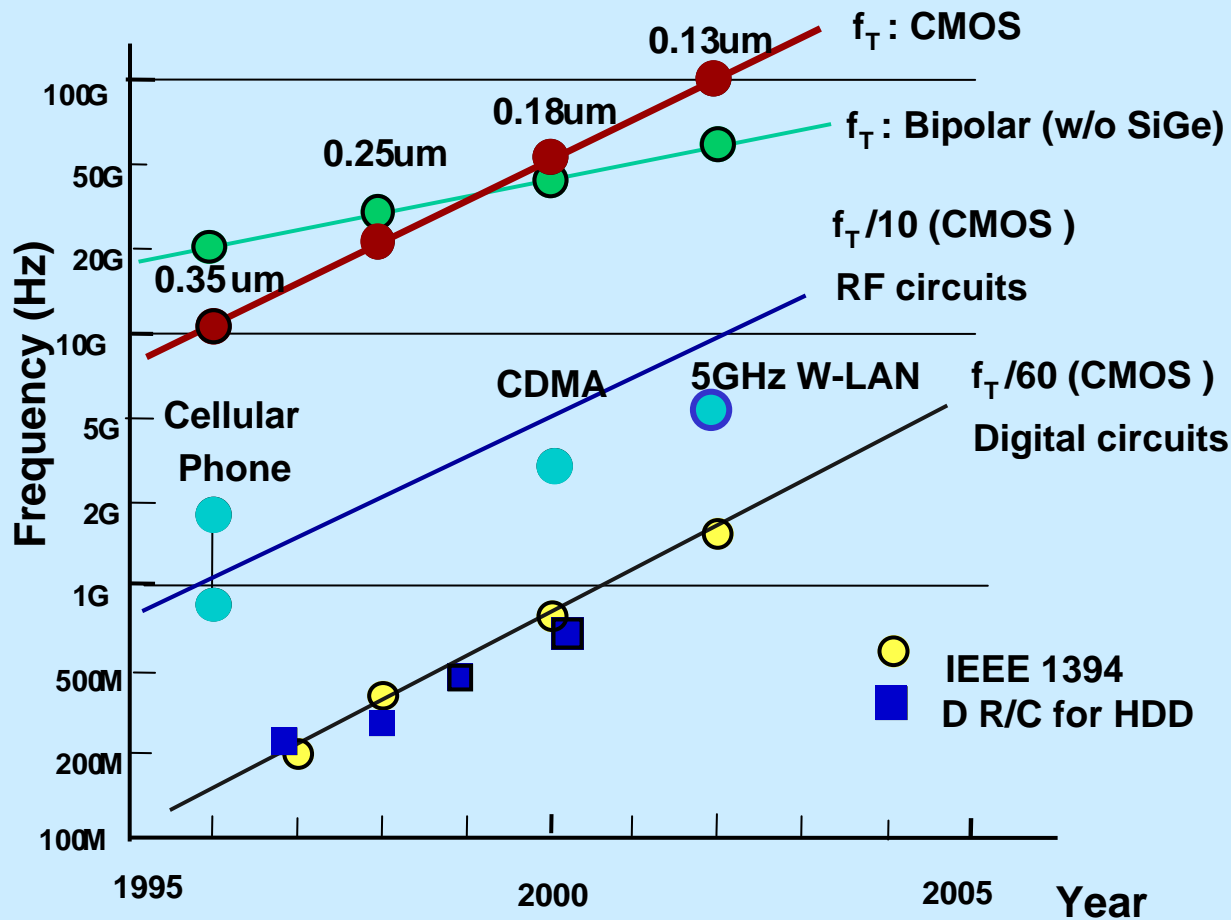
# CMOS as analog device

CMOS has many issues as analog device,  
but also has a variety of circuit techniques

	CMOS	Bipolar	Comment
Switch action	++	--	Only CMOS can realize switched capacitor circuits
Low Input current	++	--	
High gm	-	+	CMOS is ¼ of Bip.
Low Capacitance	+	-	This results in Cp issue
$f_T$	+	+	Almost same
Voltage mismatch	--	++	CMOS is 10x of Bip.
1/f noise	--	++	CMOS is 10x to 100x of Bip.
Low Sub. effect	-	+	
Offset cancel	++	--	CMOS has a variety of techniques to address the self issues
Analog calibration	++	--	
Digital calibration	++	--	
Embed in CMOS	++	--	

# GHz operation by CMOS

Cutoff frequency of MOS becomes higher than that of Bipolar.  
Over several GHz operations have attained in CMOS technology



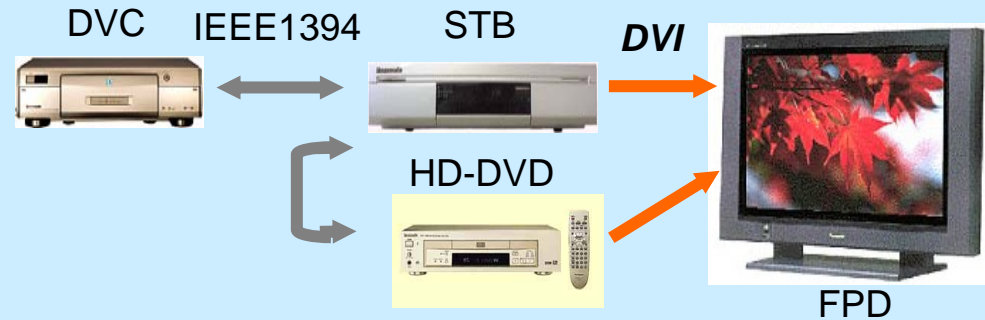
$$f_T \equiv \frac{gm}{2\pi C_{in}}$$

$$f_{Tpeak} \approx \frac{V_{sat}}{2\pi L_{eff}}$$



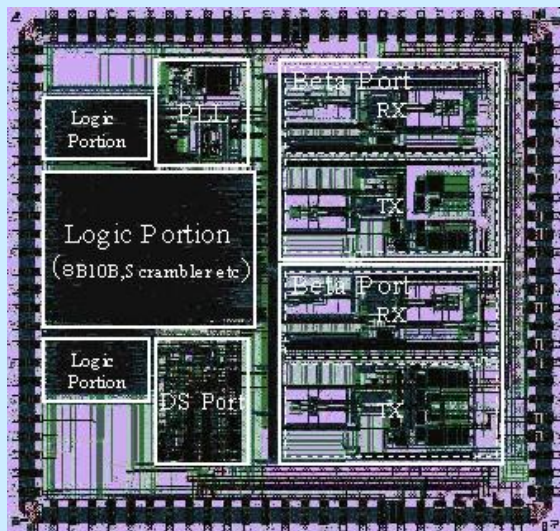
# CMOS technology for over GHz networking

Digital consumer needs over GHz wire line networking.  
CMOS has attained 5Gbps data transfer.



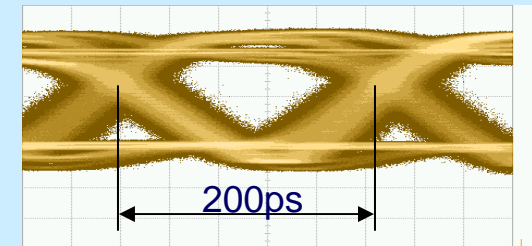
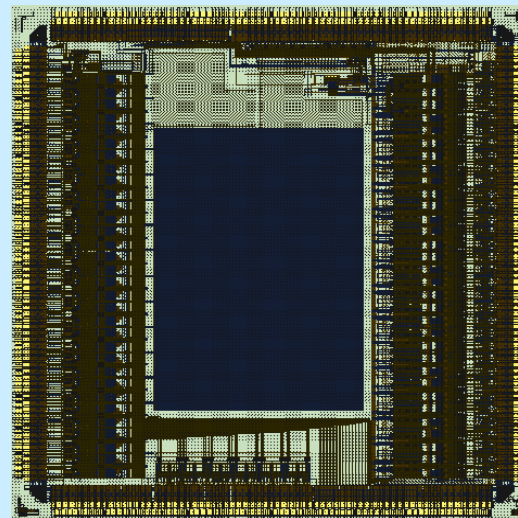
World first 1394b transceiver  
For 1Gbps networking

0.25um 3AL\_CMOS



Test chip for 5Gbps wire line

0.18um 4AL\_CMOS



5Gbps Eye pattern

# $f_T$ : MOS vs. Bipolar

Even if  $f_T$  of MOS is same as that of Bipolar,  
 $f_T$  of MOS is easily lowered by parasitic capacitance.  
 Because,  $g_m$  of MOS is  $\frac{1}{2}$  to  $\frac{1}{4}$  of that of Bipolar at the same current.

MOS

$$g_m \equiv \frac{I_{ds}}{\left(\frac{V_{eff}}{2}\right)}$$

$$V_{eff\ min} = 2nU_T \quad n: 1.4$$

$V_{eff}/2$ : 50-100mV  
 (actual ckt.)

$$f_T \equiv \frac{g_m}{2\pi C_{in}}$$

Bipolar

$$g_m \equiv \frac{I_c}{U_T}$$

$$U_T \equiv \frac{kT}{q} \approx 26mV$$

(Same operating current)

$$g_{m_{CMOS}} < \frac{1}{2}, \frac{1}{4} g_{m_{Bip}}$$

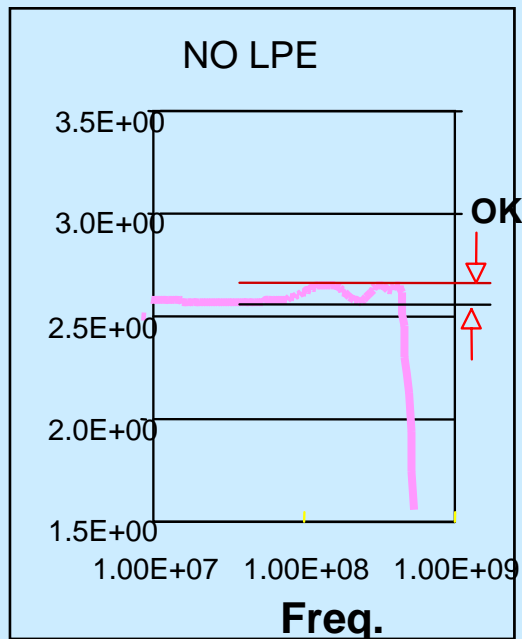
$$C_{in_{CMOS}} < \frac{1}{2}, \frac{1}{4} C_{in_{Bip}}$$

(Same  $f_T$ )

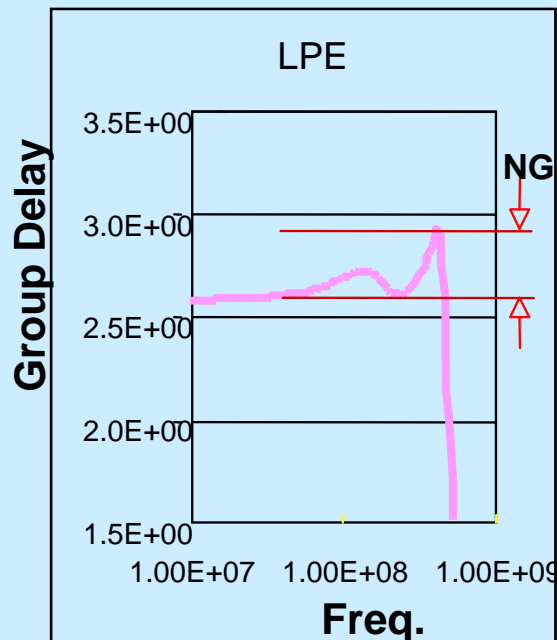
# Parasitic effect: CMOS CT filter

High frequency ckt. with scaled device is strongly affected from parasitic. Circuit optimization with layout and parasitic effect is needed.

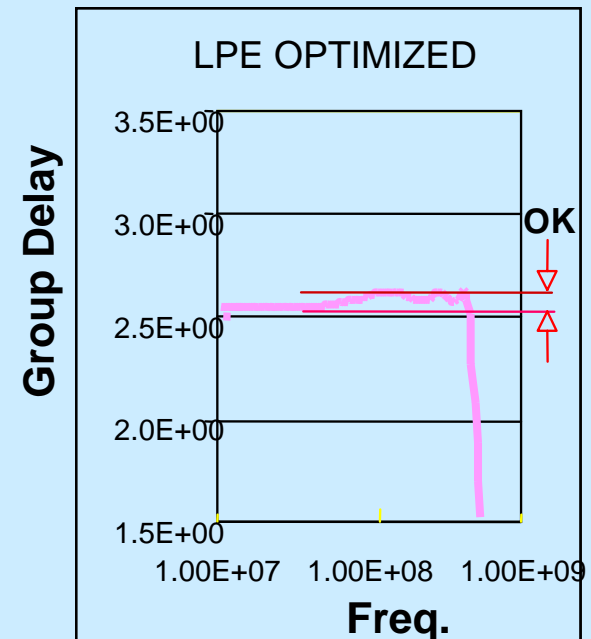
SIM w/o parasitic C



SIM with parasitic C

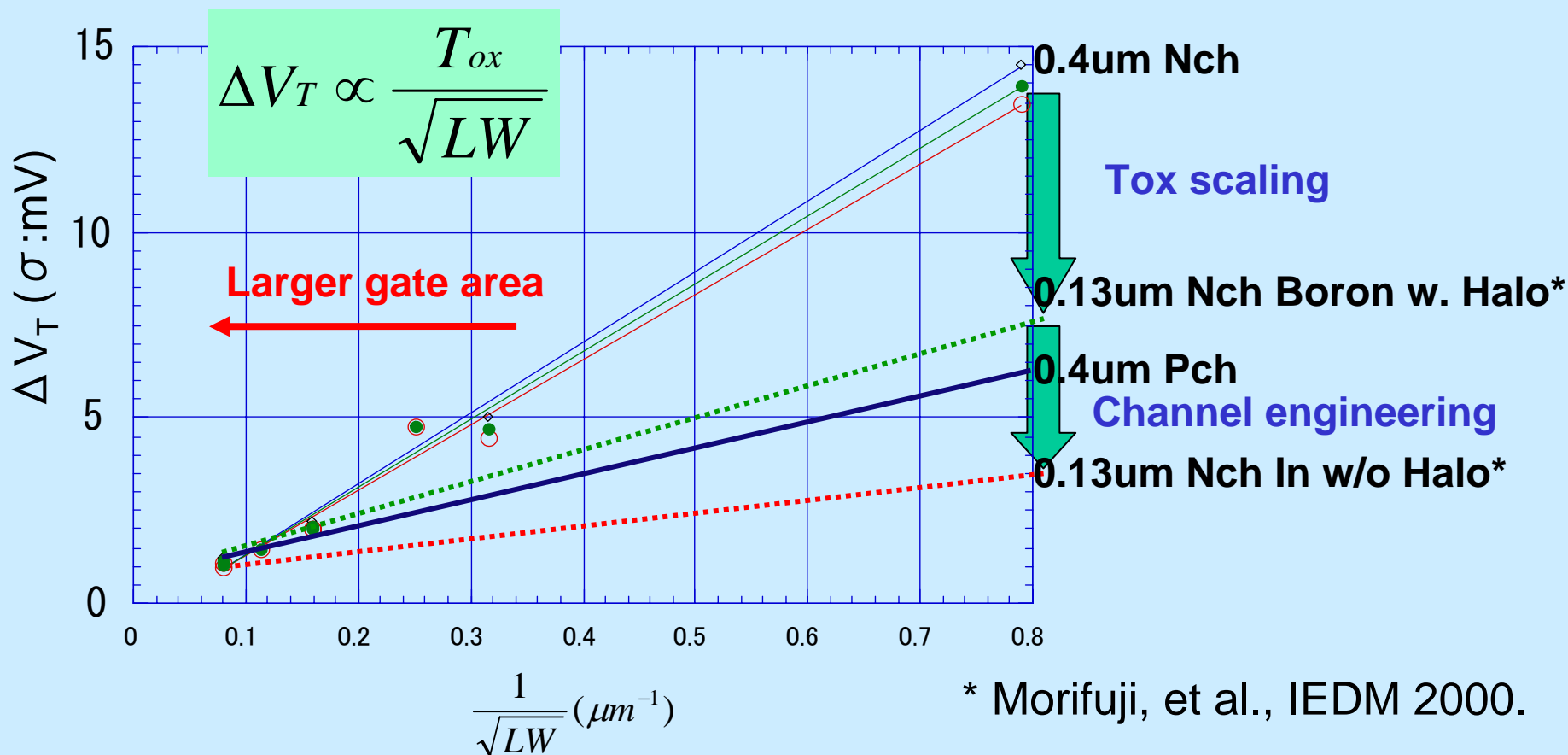


Optimized with parasitic C



# Transistor issue: $V_T$ mismatch

Larger gate area is needed for small  $V_T$  mismatch.  
Scaling and proper channel structure can improve this.



\* Morifuji, et al., IEDM 2000.

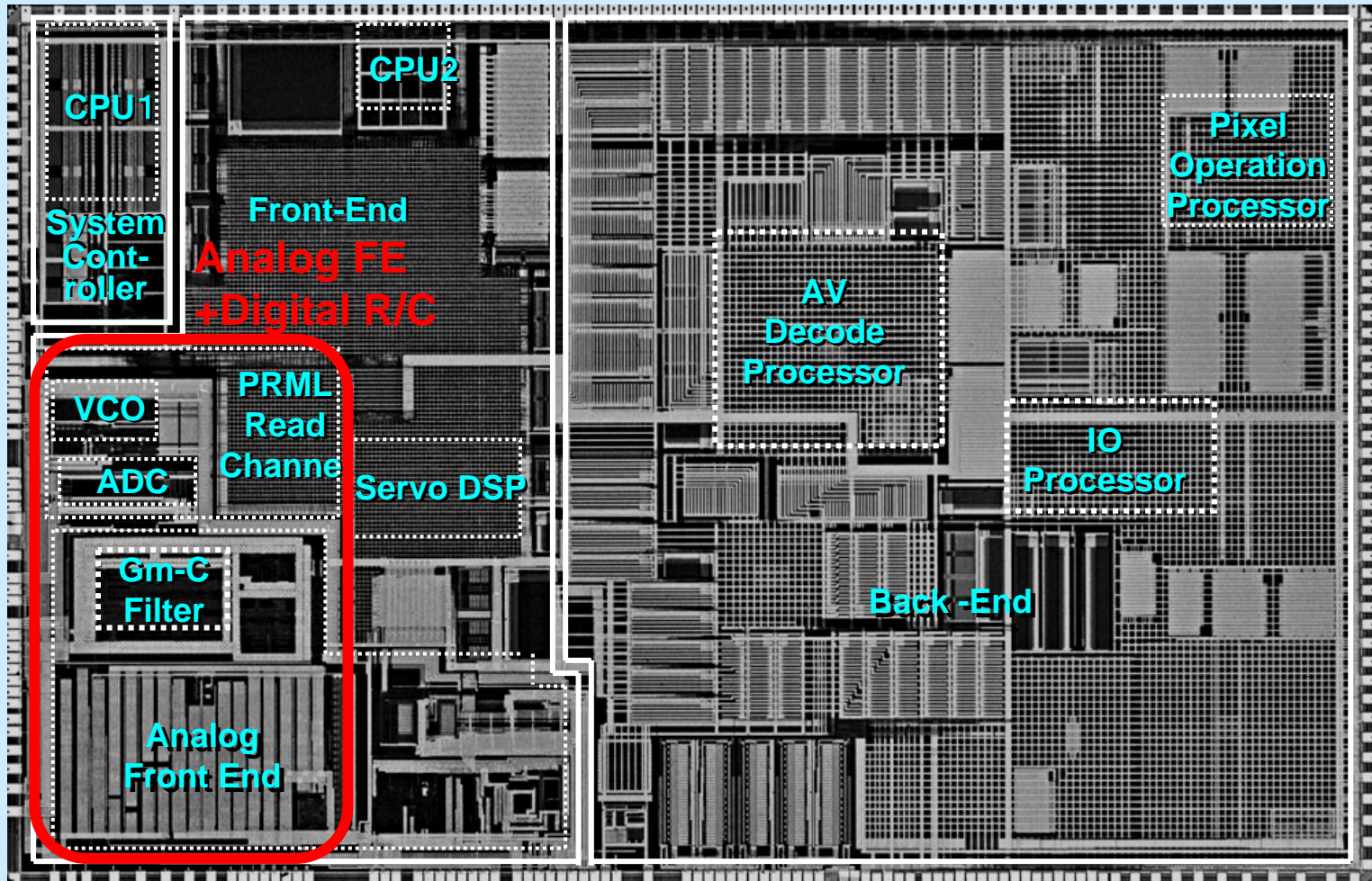
# **Development strategy and design system for mixed signal SoC**

# Full DVD system integration in 0.13um tech.

Advanced mixed signal SoC has been successfully developed.

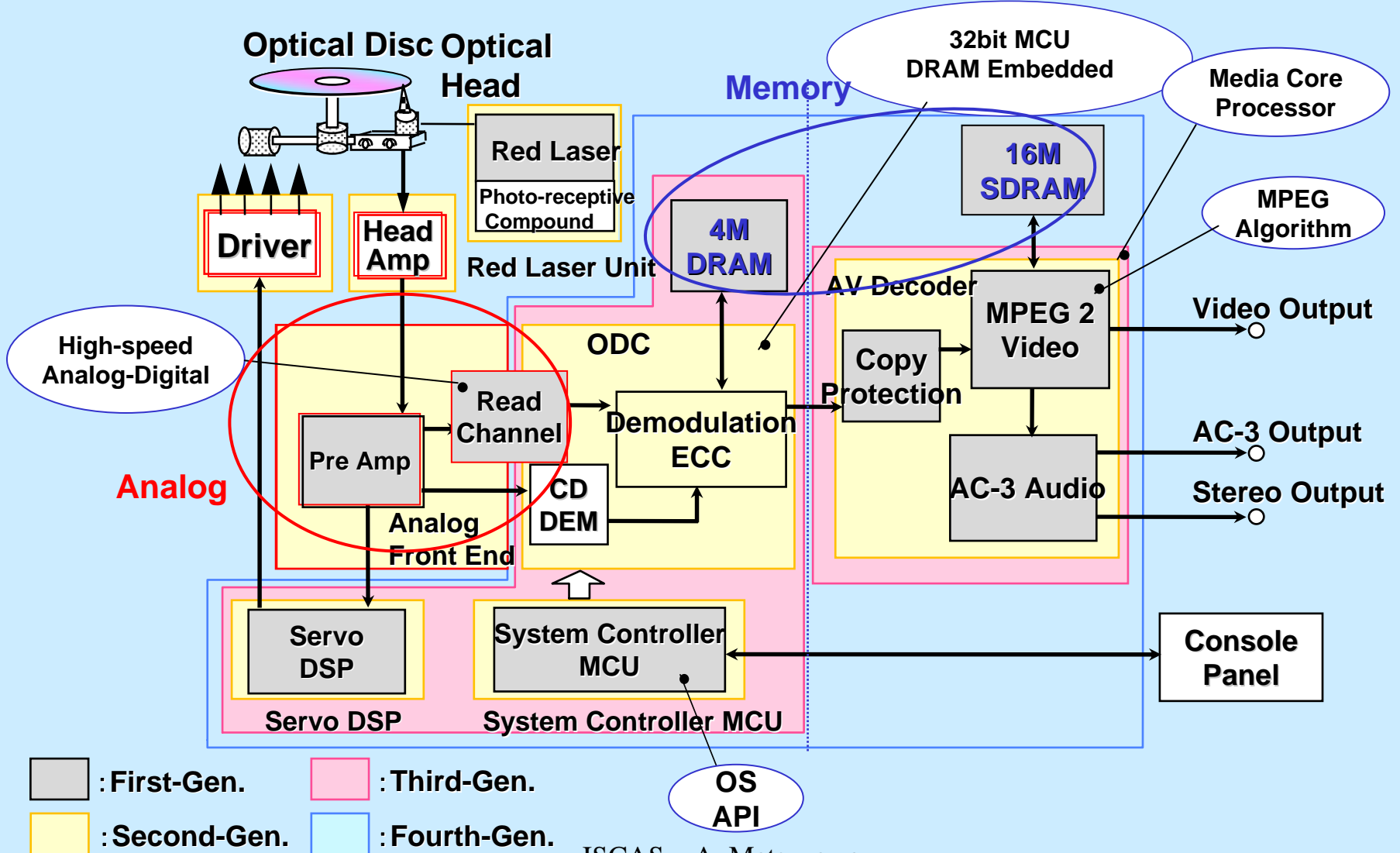
Okamoto, et al., ISSCC 2003

0.13um, Cu 6Layer, 24MTr



# System: DVD player

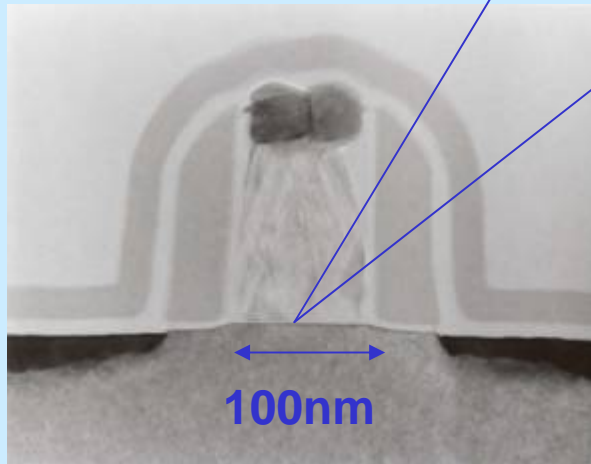
Current electrical system is complicated and needs analog and memory.



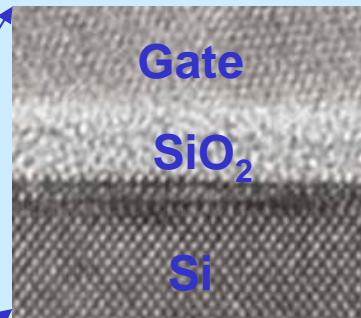
# Scaled CMOS technology

Current Scaled CMOS technology is very artistic.

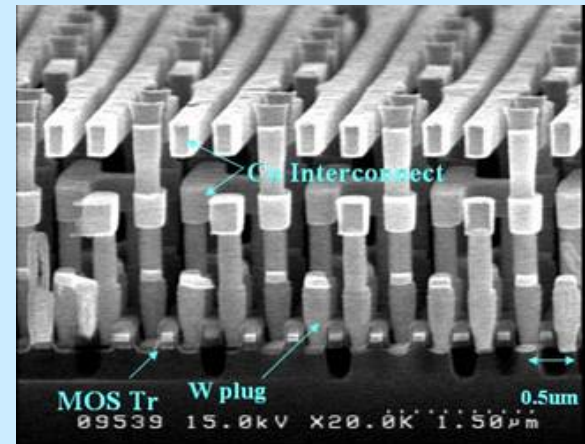
Matsushita's 0.13um CMOS technology



Transistor



Seven lattices



Cu Interconnection

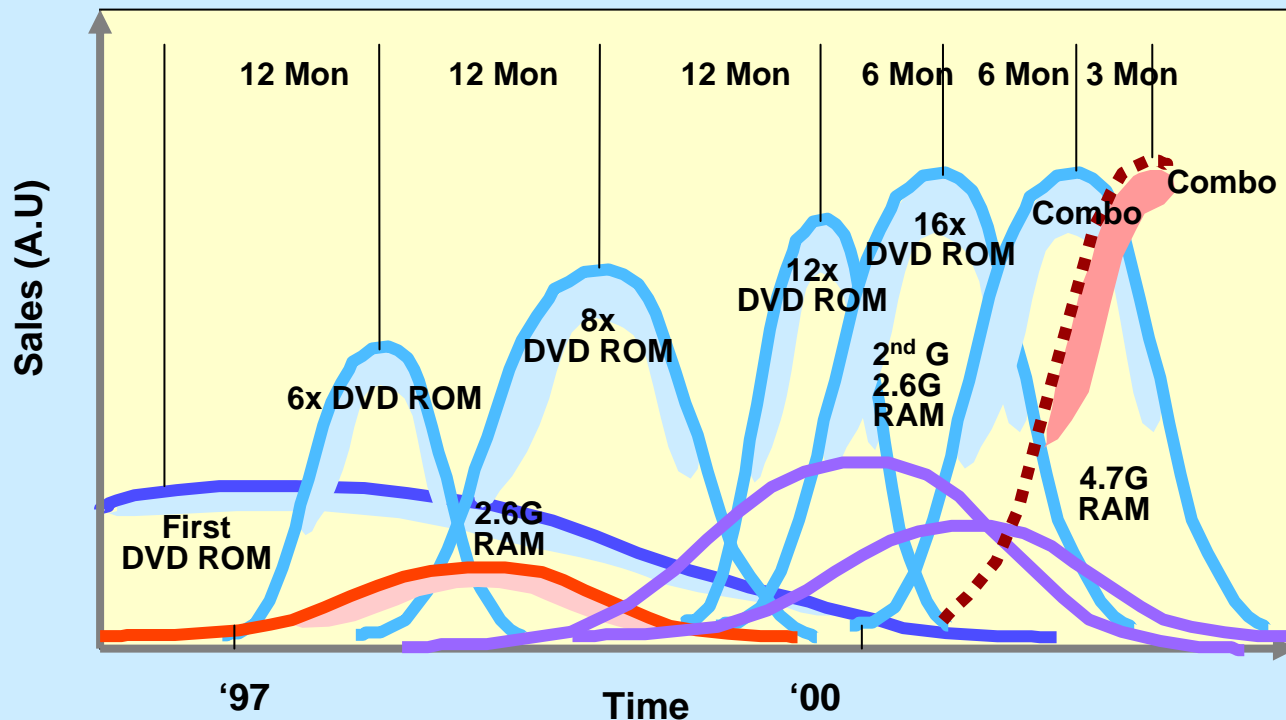


# Development strategy and system

Product time slot is narrow and development cost is huge.

Conventional analog LSI needs 2 or 3 re-designs.  
This can not be accepted to mixed signal SoC

**Advanced development strategy and design system must be established.**



# Strategy for the mixed signal SoC

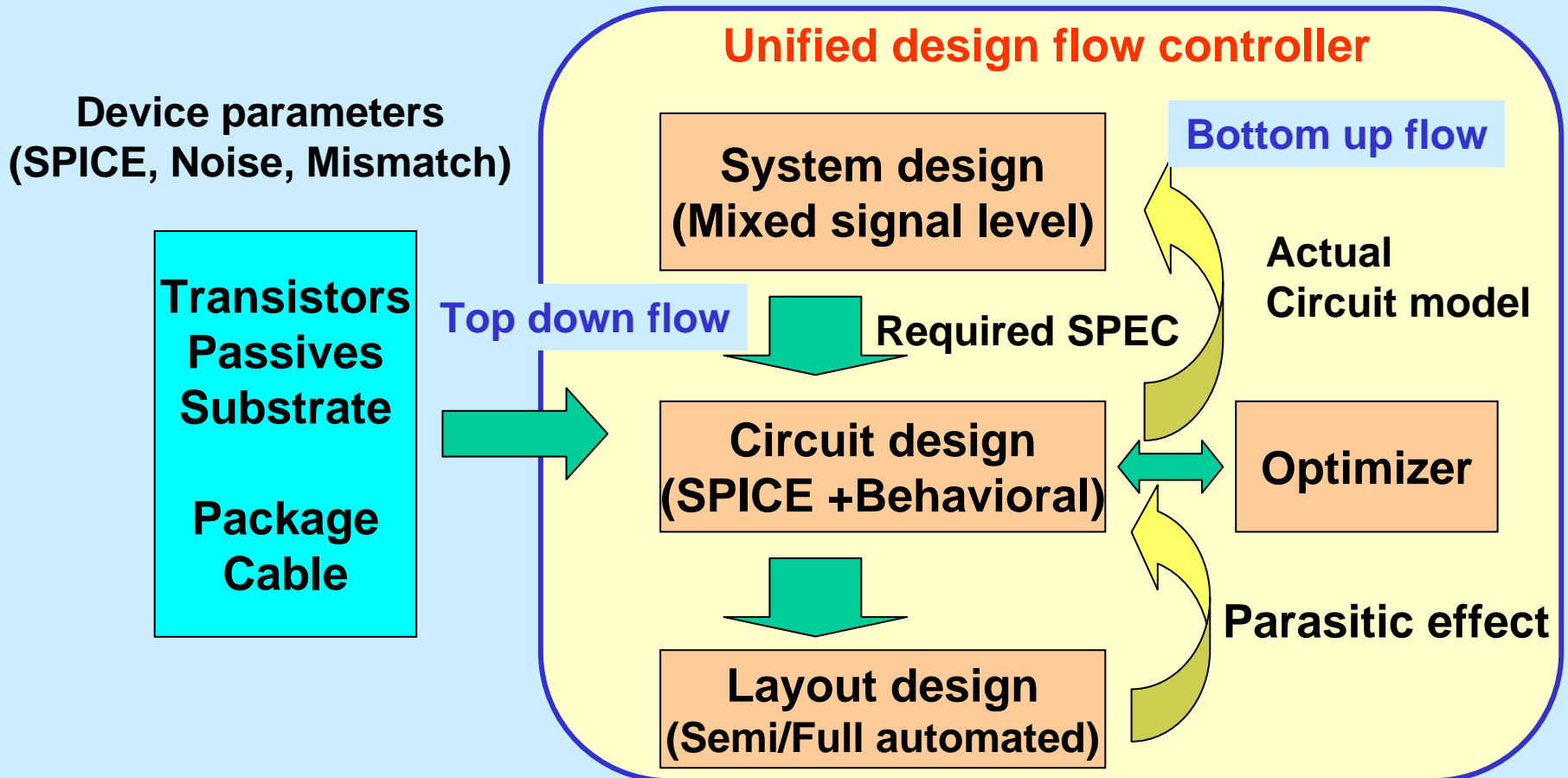
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- **System design**
  - **Digital calibration** for analog adjustment and unknown parameters.
  - **System optimization** to reduce analog area and increase robustness.
- **System verification**
  - Fast and accurate **mixed signal system simulator** with behavioral model to verify and optimize the mixed signal system.
  - Create the **target performance** for circuit blocks.
- **Circuit design**
  - **Ultra fast and accurate circuit simulation for P.V.T** and fluctuation analysis to verify the performance and robustness.
  - **Circuit optimizer** to find the sweet spot of the circuit.
  - **Automated creation of analog behavioral model** for system sim.
- **Process and device development**
  - Develop suitable **analog option device**
  - Early **analog parameter extraction** ( mismatch, temp. and voltage chara.)
  - **Monitor and control** the analog parameters in Fab.

# Design flow for mixed signal SoC

Design flow from System to layout with top down and bottom up process should be used for designing mixed signal SoC.

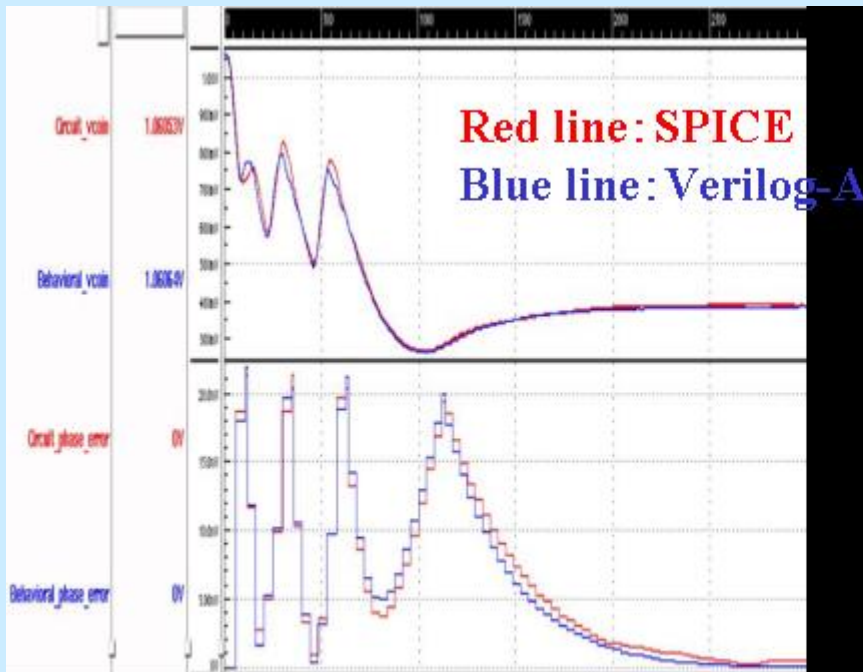
Accurate and a variety of device parameters is an another key.



# Multi-language simulation

Multi-language simulation is **56x** faster than SPICE with same accuracy. This will contribute to shorter design TAT and higher design quality.

## SPICE+Verilog D+Verilog A

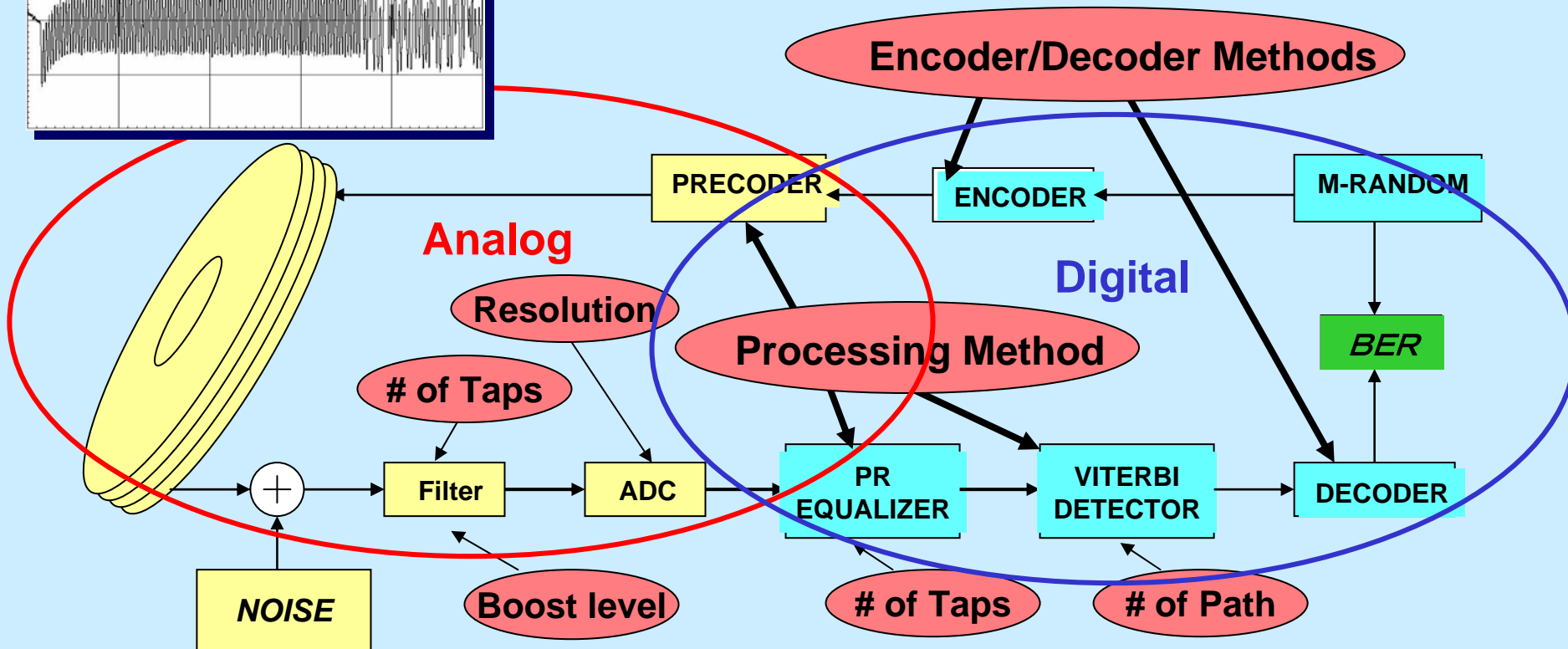
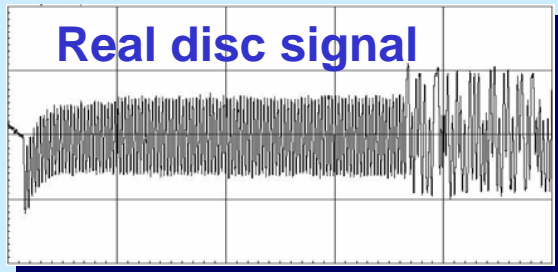


Description	Option	Time	CPU Time (s)	Speed Ratio
PLL Behavioral Lev (Verilog-A+SPICE)		9 min	545	56
PLL Circuit Level (Spice)	Model Opt.	2 hr 12 min	7939	3.8
PLL Circuit Level (Spice)		8 hr 27 min	30414	1

# Mixed signal system design

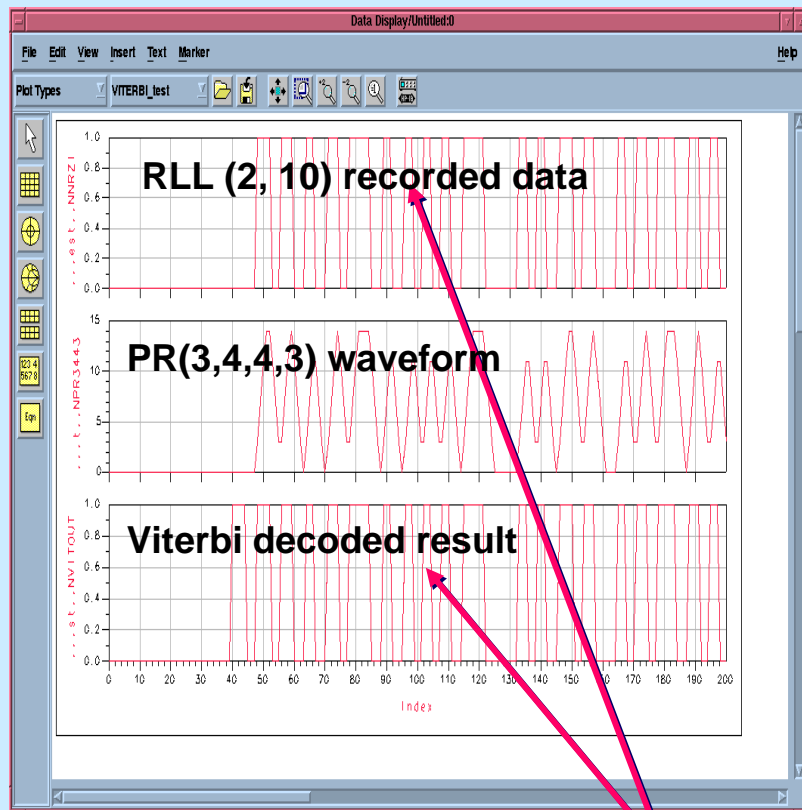
Needs mixed signal Simulation for total signal processing.  
Many parameters and processing methods should be optimized.

Finally, system is checked by real disc signals.



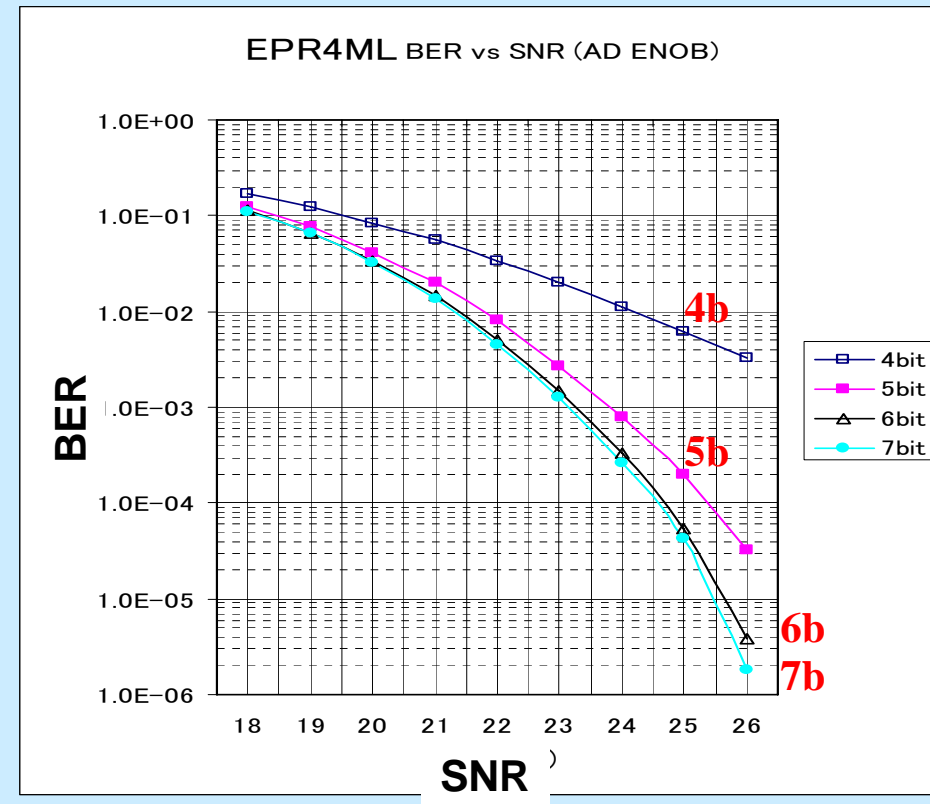
# System simulation

Perfection of the mixed signal system should be verified and optimized by system simulation.



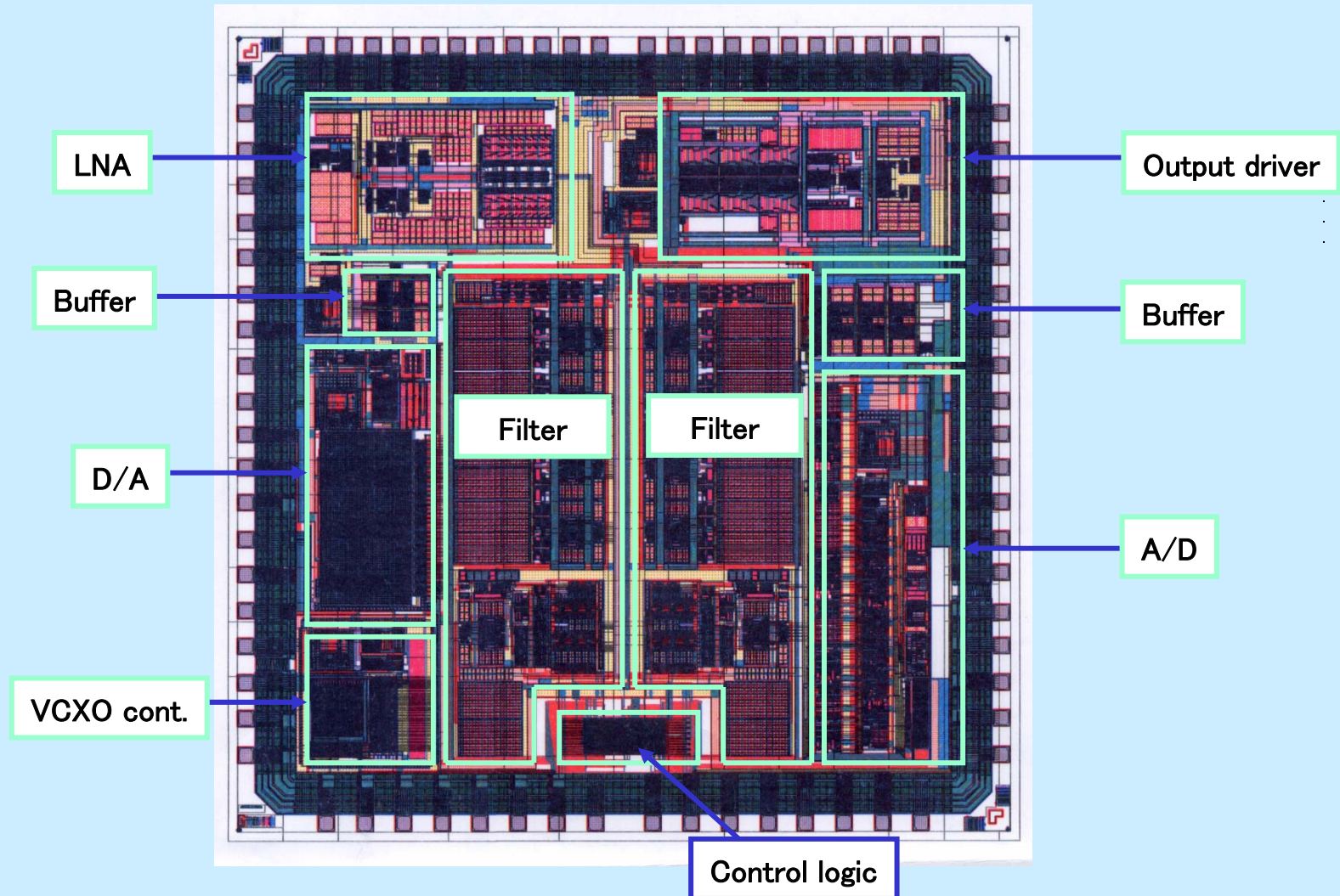
System verification

## ADC resolution effect



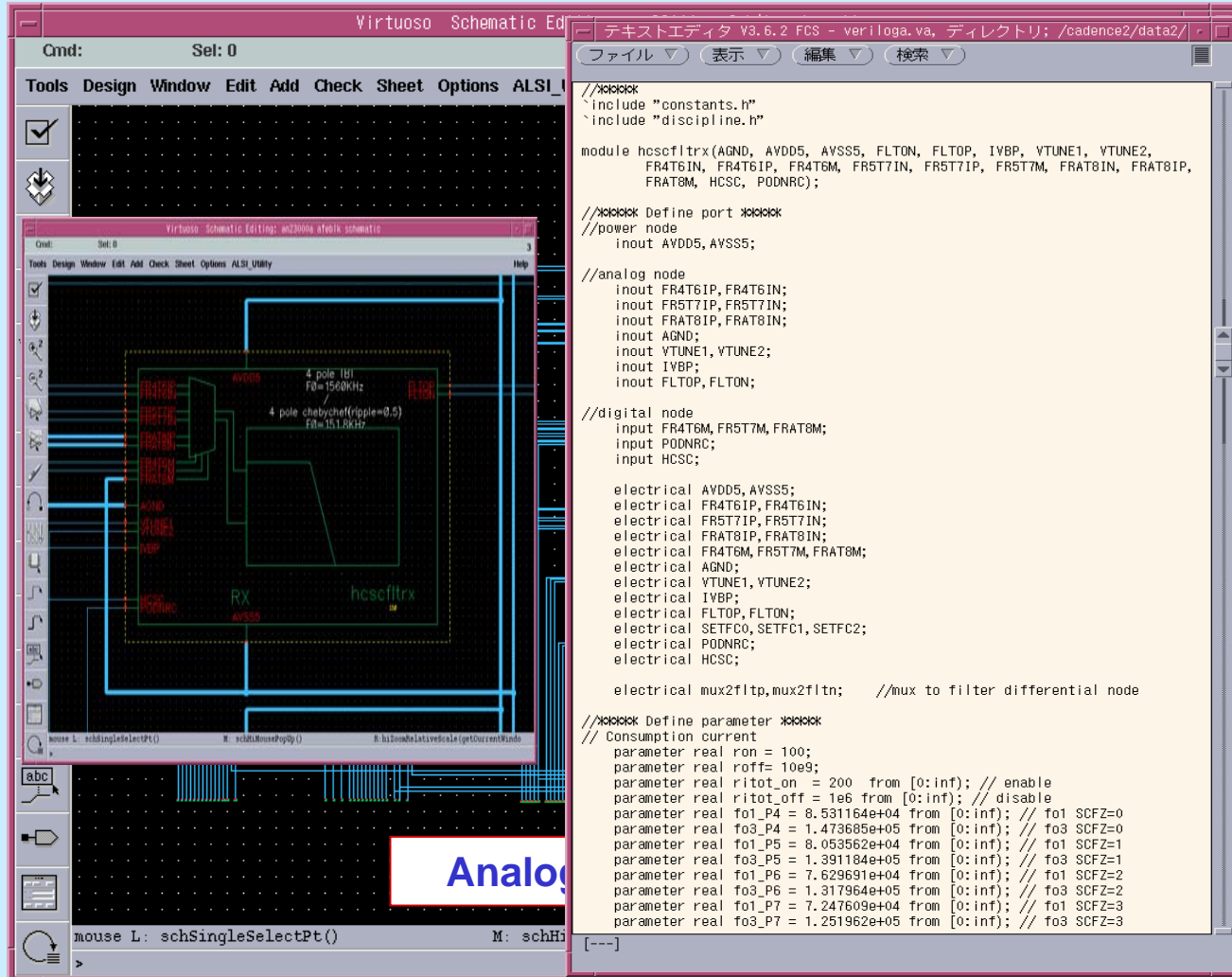
# LSI design using behavioral language

Example: Analog Front End chip for ADSL system.



# Hierarchical and behavioral system design

System should be described in behavioral language, hierarchically.



The image shows a screenshot of the Virtuoso Schematic Editor interface. The main window displays a schematic diagram of a filter system. The schematic includes several blocks: a 4-pole IIR filter with a center frequency of 1500 kHz, a 4-pole Chebyshev filter with a ripple of 0.5 dB and a center frequency of 15.18 kHz, and a filter block labeled 'hscsfltr'. The schematic is connected to various power and signal nodes, including AVDD5, AVSS5, and several FRAT and FLT nodes. A text editor window is open on the right, displaying the Verilog code for the 'hscsfltr' module. The code includes include statements for constants and discipline, module declarations for ports, and electrical annotations for various nodes. It also defines parameters for consumption current and filter characteristics.

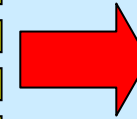
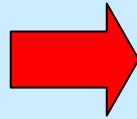
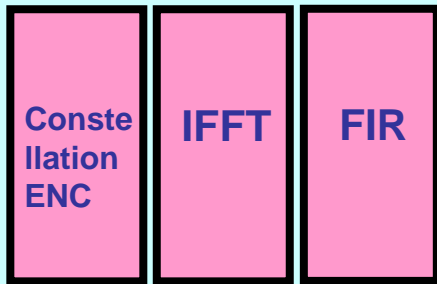
```
//*****  
`include "constants.h"  
`include "discipline.h"  
  
module hscsfltrx(AGND, AVDD5, AVSS5, FLT0N, FLT0P, IVBP, VTUNE1, VTUNE2,  
FR4T6IN, FR4T6IP, FR4T6M, FR5T7IN, FR5T7IP, FR5T7M, FRAT8IN, FRAT8IP,  
FRAT8M, HCSC, PODNRC);  
  
//***** Define port *****  
//power node  
inout AVDD5, AVSS5;  
  
//analog node  
inout FR4T6IP, FR4T6IN;  
inout FR5T7IP, FR5T7IN;  
inout FRAT8IP, FRAT8IN;  
inout AGND;  
inout VTUNE1, VTUNE2;  
inout IVBP;  
inout FLT0P, FLT0N;  
  
//digital node  
input FR4T6M, FR5T7M, FRAT8M;  
input PODNRC;  
input HCSC;  
  
electrical AVDD5, AVSS5;  
electrical FR4T6IP, FR4T6IN;  
electrical FR5T7IP, FR5T7IN;  
electrical FRAT8IP, FRAT8IN;  
electrical FR4T6M, FR5T7M, FRAT8M;  
electrical AGND;  
electrical VTUNE1, VTUNE2;  
electrical IVBP;  
electrical FLT0P, FLT0N;  
electrical SETFC0, SETFC1, SETFC2;  
electrical PODNRC;  
electrical HCSC;  
  
electrical mux2fltp, mux2fltn; //mux to filter differential node  
  
//***** Define parameter *****  
// Consumption current  
parameter real ron = 100;  
parameter real roff = 10e9;  
parameter real rriot_on = 200 from [0:inf]; // enable  
parameter real rriot_off = 1e6 from [0:inf]; // disable  
parameter real fo1_P4 = 8.531164e+04 from [0:inf]; // fo1 SCFZ=0  
parameter real fo3_P4 = 1.473685e+05 from [0:inf]; // fo3 SCFZ=0  
parameter real fo1_P5 = 8.053562e+04 from [0:inf]; // fo1 SCFZ=1  
parameter real fo3_P5 = 1.391184e+05 from [0:inf]; // fo3 SCFZ=1  
parameter real fo1_P6 = 7.629691e+04 from [0:inf]; // fo1 SCFZ=2  
parameter real fo3_P6 = 1.317964e+05 from [0:inf]; // fo3 SCFZ=2  
parameter real fo1_P7 = 7.247609e+04 from [0:inf]; // fo1 SCFZ=3  
parameter real fo3_P7 = 1.251962e+05 from [0:inf]; // fo3 SCFZ=3  
  
[---]
```



# Virtual System test using Verilog AMS and Matlab

We can test the designed mixed signal system virtually, by using Verilog AMS and Matlab.

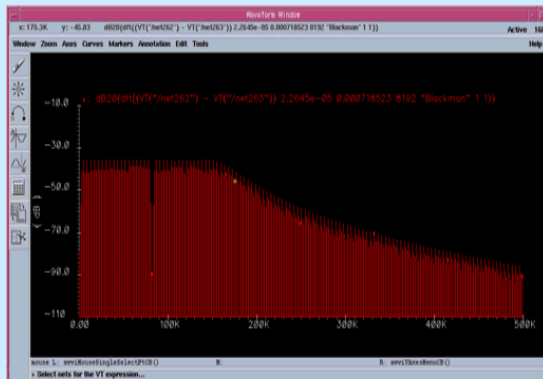
Matlab  
DMT modulation



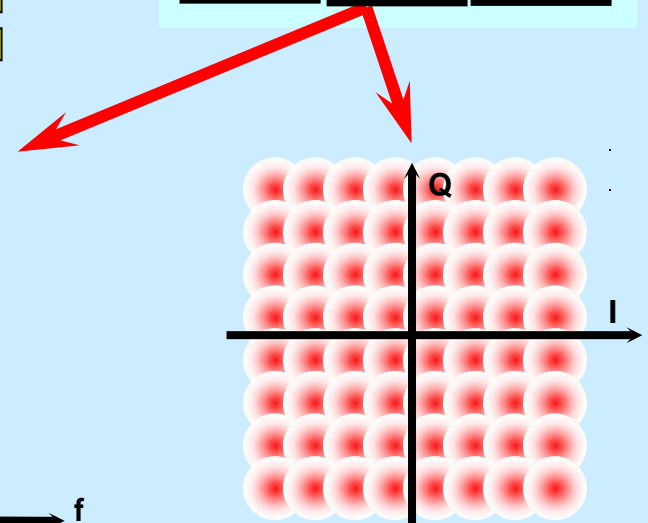
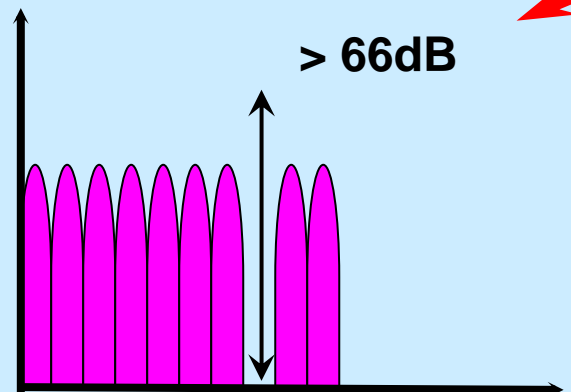
Matlab  
DMT demodulation



Matlab is used as a soft DSP

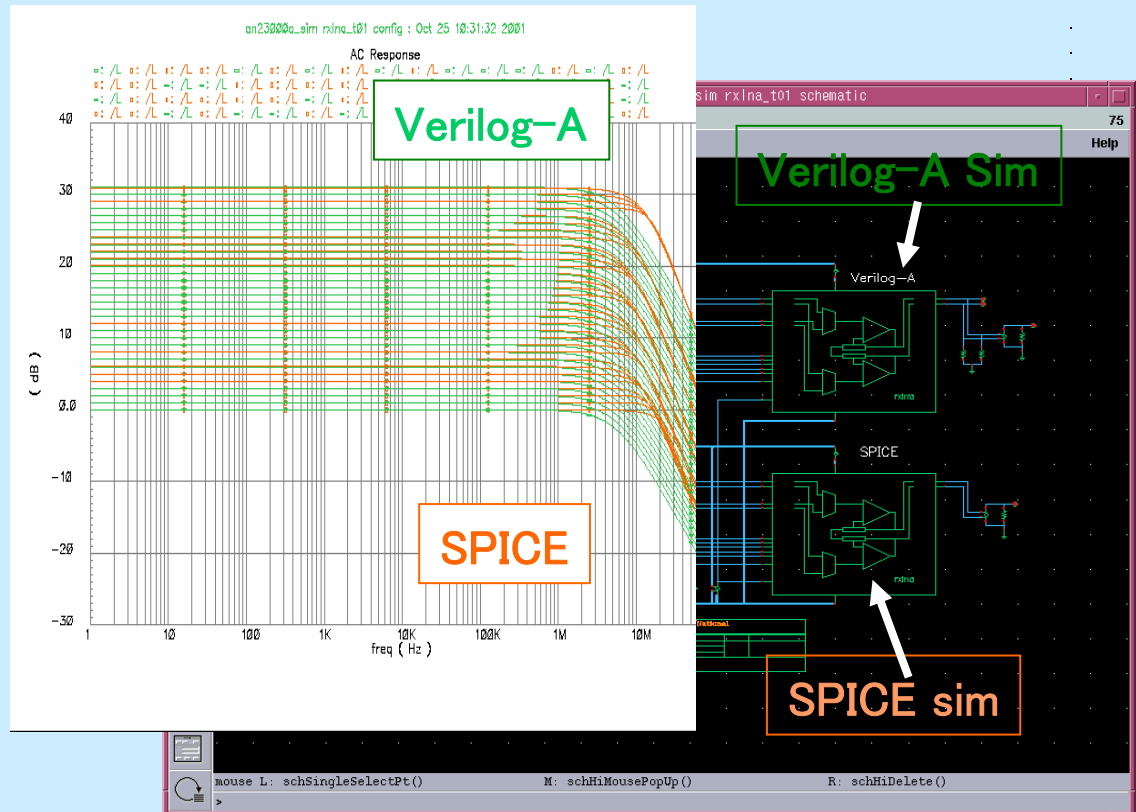
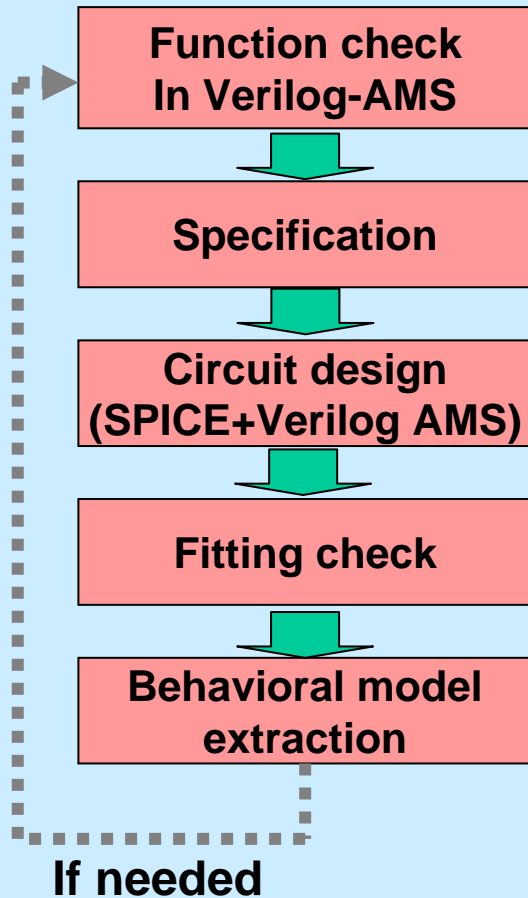


MTPR TEST (DMT Carrier hole)



# Fitting between behavioral and Spice

The combination of Verilog AMS and SPICE assures system perfection.



# Unified mixed signal circuit simulator

New design system can increase design speed, 10x to 50x.

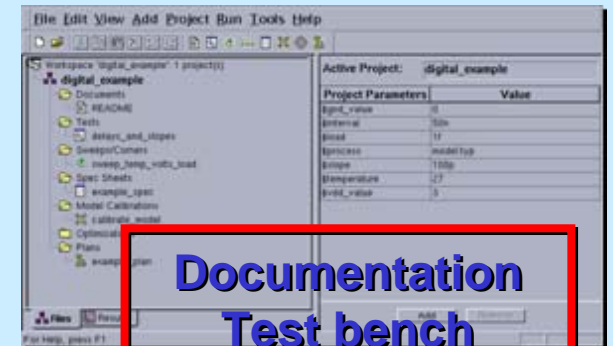
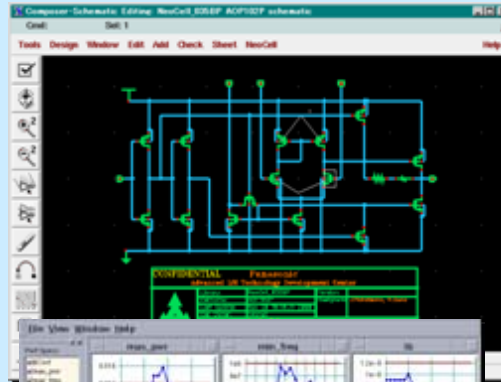
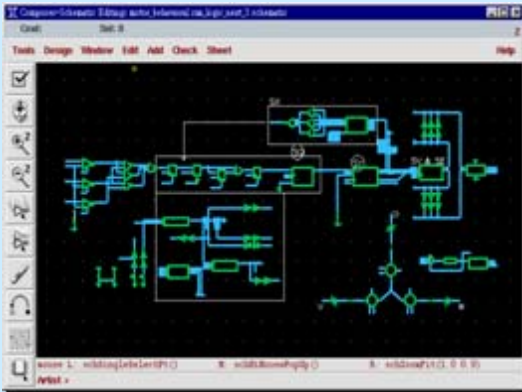
System level

Specification

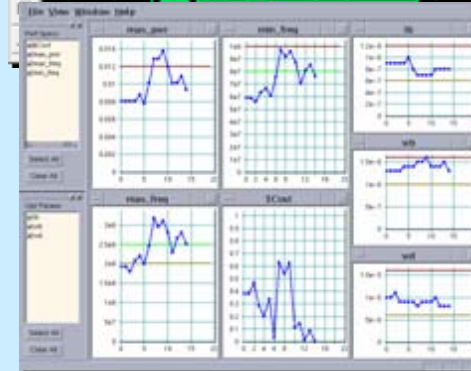
Optimization

Simulation Results

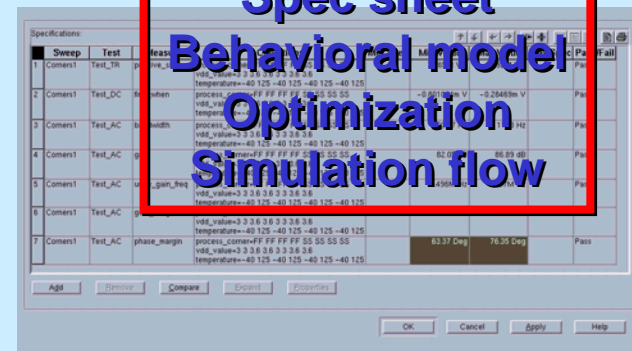
Design flow controller



Verilog-AMS  
+SPICE



Documentation  
Test bench  
PVT analysis  
Spec sheet  
Behavioral model  
Optimization  
Simulation flow



Sweep	Test	Meas	Pass	Fail	
1	Comes1	Test_TR	process=FF FF FF FF 55 55 55 temperature=-40 125 -40 125 -40 125 -40 125	Pass	Fail
2	Comes1	Test_DC	process=FF FF FF FF 55 55 55 vdd_value=-0.28486m V temperature=-40 125 -40 125 -40 125 -40 125	Pass	Fail
3	Comes1	Test_AC	process=FF FF FF FF 55 55 55 vdd_value=3.3 3.3 3.3 3.3 3.3 3.3 temperature=-40 125 -40 125 -40 125 -40 125	Pass	Fail
4	Comes1	Test_AC	process=FF FF FF FF 55 55 55 vdd_value=3.3 3.3 3.3 3.3 3.3 3.3 temperature=-40 125 -40 125 -40 125 -40 125	Pass	Fail
5	Comes1	Test_AC	process=FF FF FF FF 55 55 55 vdd_value=3.3 3.3 3.3 3.3 3.3 3.3 temperature=-40 125 -40 125 -40 125 -40 125	Pass	Fail
6	Comes1	Test_AC	process=FF FF FF FF 55 55 55 vdd_value=3.3 3.3 3.3 3.3 3.3 3.3 temperature=-40 125 -40 125 -40 125 -40 125	Pass	Fail
7	Comes1	Test_AC	phase_margin 63.37 Deg 76.36 Deg	Pass	Fail

# Controller for automated simulation

Simulation controller enables fast and automated simulation steps

The screenshot shows a software window titled "ACV - PLL015" with a menu bar (File, Edit, View, Add, Project, Run, Tools, Help) and a toolbar. The main workspace is divided into a left-hand tree view and a right-hand parameter table. The tree view shows a project named "PLL015" with subfolders: Documents, Tests, Sweeps/Corners, Spec Sheets, Model Calibrations, Model Generators, Optimizations, and Plans. The parameter table on the right lists parameters like \$resolution, \$tran\_duration, and \$VDD with their respective values. Red arrows point from text boxes to specific elements in the interface: "Project name" points to the PLL015 folder; "Test bench (20 types)" points to the Tests folder; "Parameter seep" points to the Sweeps/Corners folder; "Spec sheet" points to the Spec Sheets folder; "Behavioral model calibration" points to the Model Calibrations folder; "Behavioral model generation" points to the Model Generators folder; "Optimization" points to the Optimizations folder; and "Design procedure" points to the Plans folder. A "Remove" button is visible at the bottom right of the parameter table.

Parameter	Value
\$resolution	1n
\$tran_duration	50u
\$VDD	1.35
\$VDD_T17	1.35
\$VDD_T4	1.35
\$VDD_T4	1.35

**Project name** PLL015

**Test bench (20 types)**

**Parameter seep**

**Spec sheet**  
-PLL simulation results  
-Behavioral modeling

**Behavioral model calibration**

**Behavioral model generation**

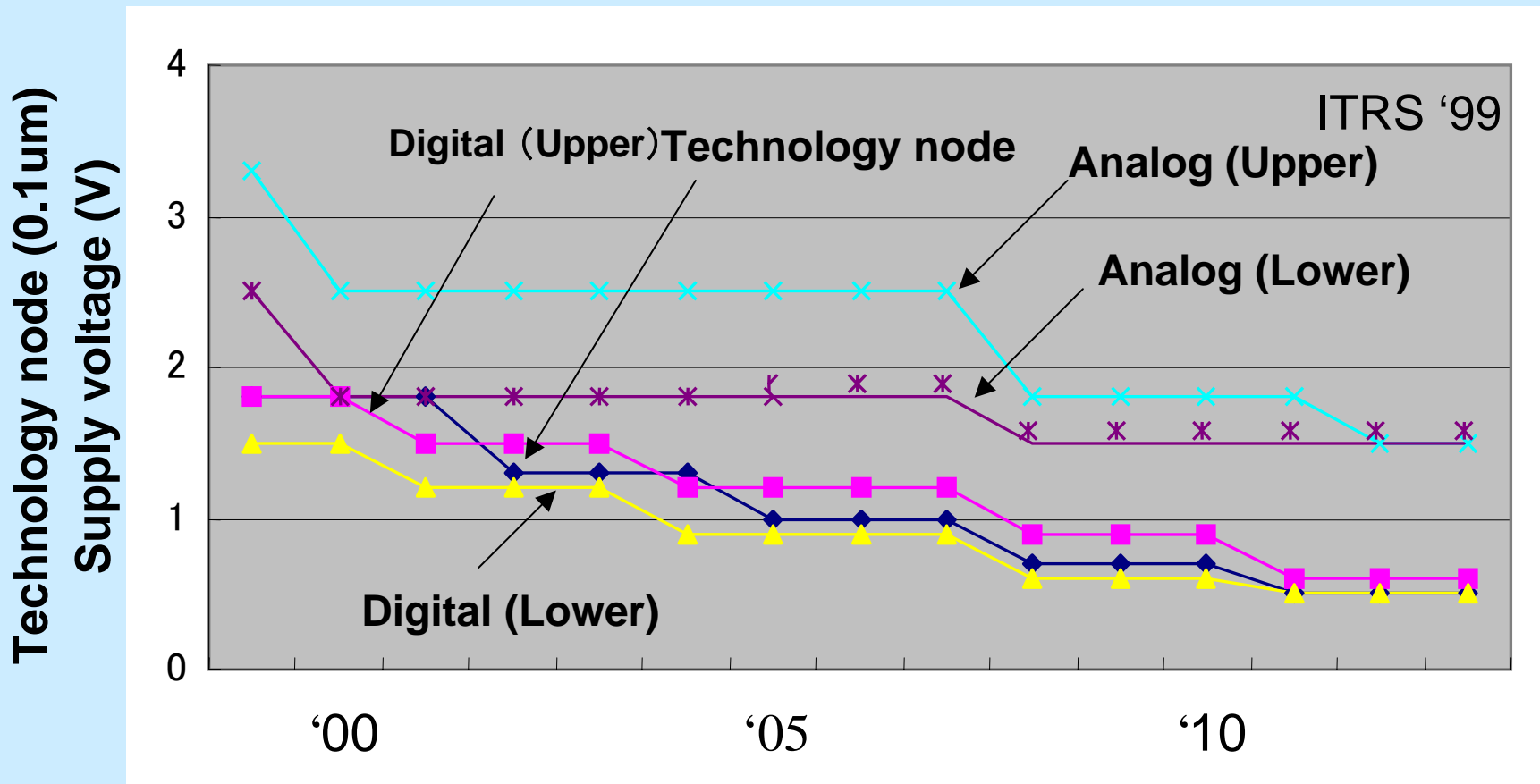
**Optimization**

**Design procedure**

# Issues of mixed signal SoC

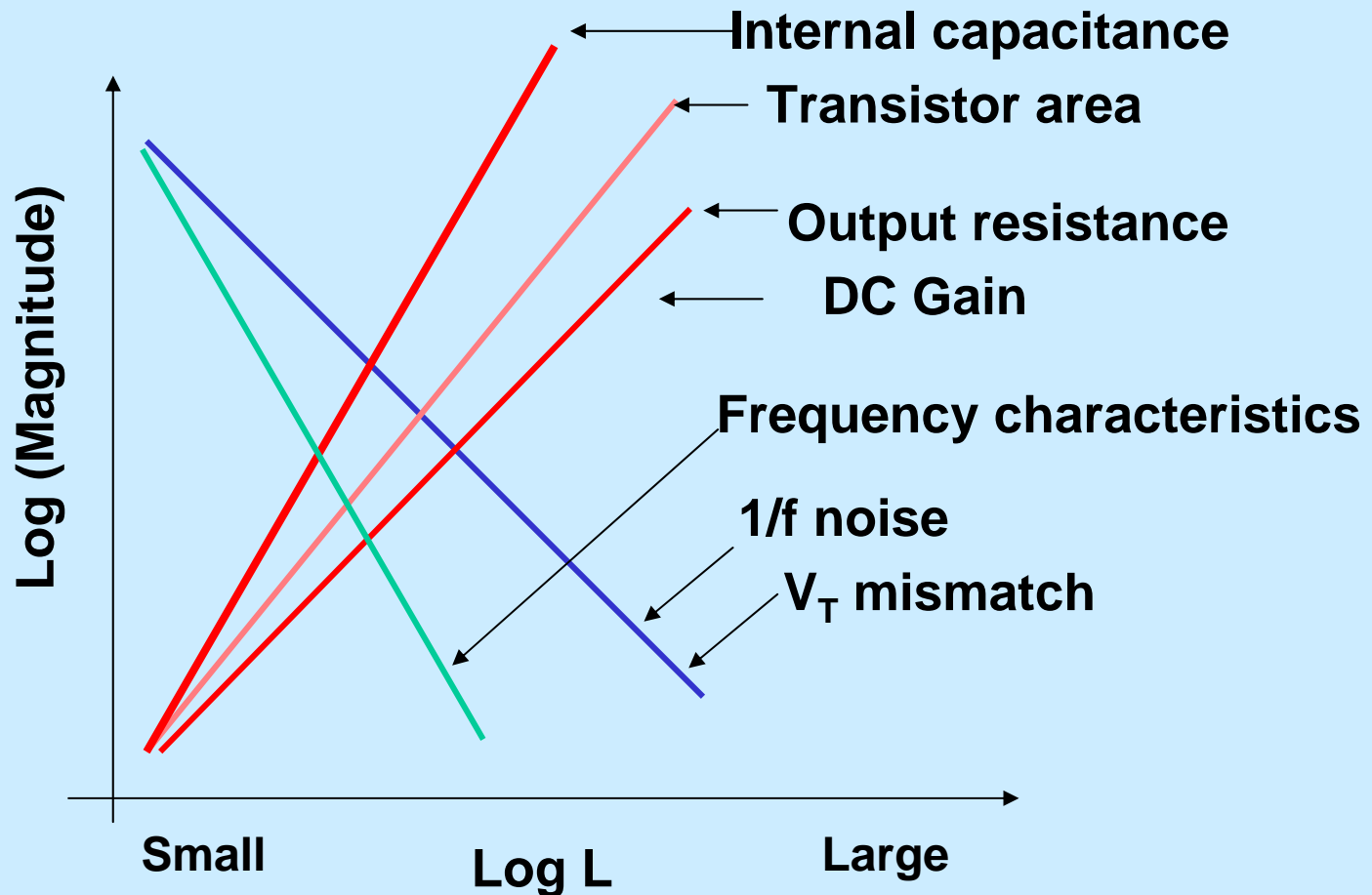
# $V_{dd}$ and CMOS scaling limits in analog

Lowest analog operating voltage must be 1.2V -1.8V.  
Thus 0.18um – 0.13um must be a scaling limit for analog.  
This results in salutation of  $f_T$  and area reduction.



# Optimization in channel parameters

Larger gate length is needed for small mismatch and small noise circuit. However, this results in increase of cost and decrease of performance.

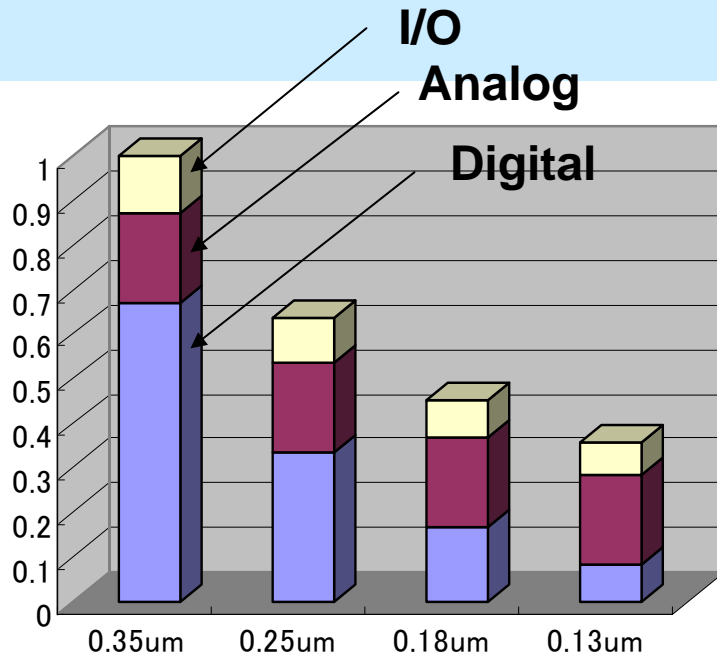


# Cost up issue by analog & I/O

Cost of mixed A/D LSI will increase when using deep sub-micron device, due to the increase of cost of non-scalable analog and I/O parts.

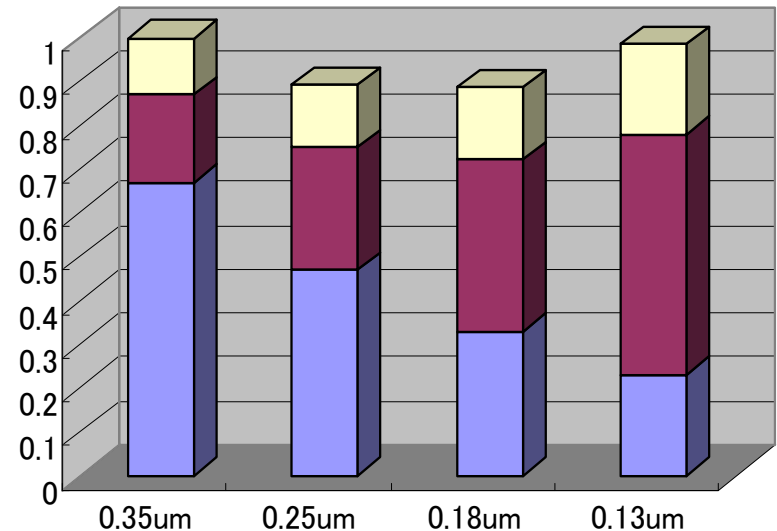
Large analog on SoC must be unacceptable in near future.

Wafer cost increases 1.3x  
for one generation



Chip area

(0.35um : 1)

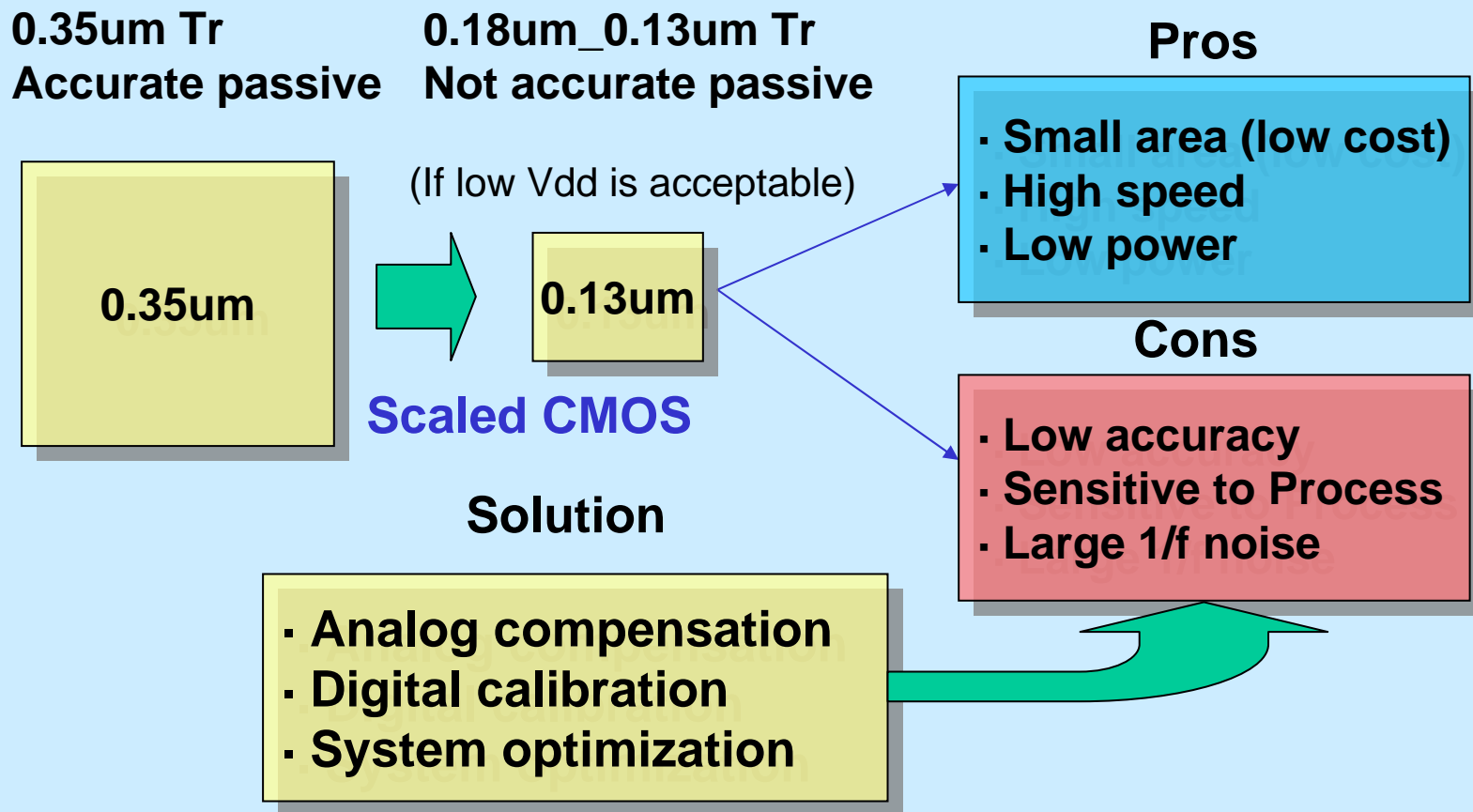


Chip cost



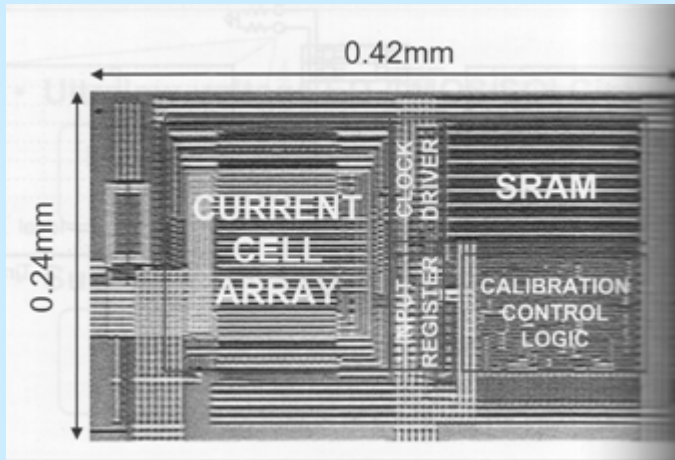
# Solution 1: Scaled CMOS and use of digital

Use scaled CMOS and not accurate passives.  
Address the issues by M/S compensation and system optimization.



# Example: Analog+ digital calibration tech.

Area and power are reduced drastically, by scaled CMOS and digital tech.



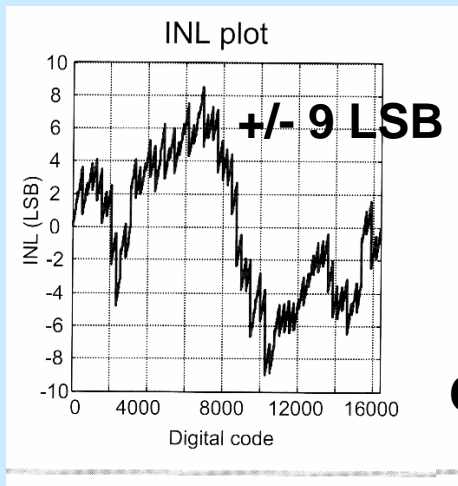
Y. Cong and R. L. Geiger, Iowa state university, ISSCC 2003

14b 100MS/s DAC

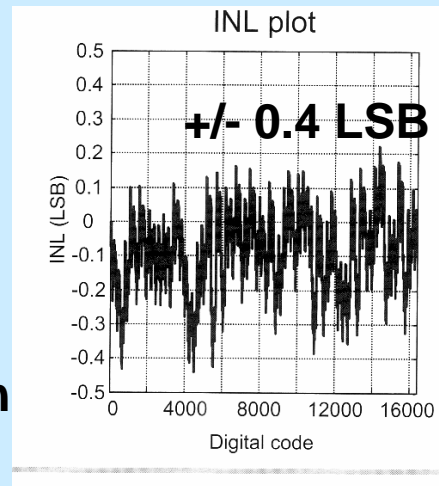
1.5V, 17mW, 0.1mm<sup>2</sup>, 0.13um

0.5 LSB INL,

SFDR=82dB at 0.9MHz, 62dB at 42.5MHz



Calibration



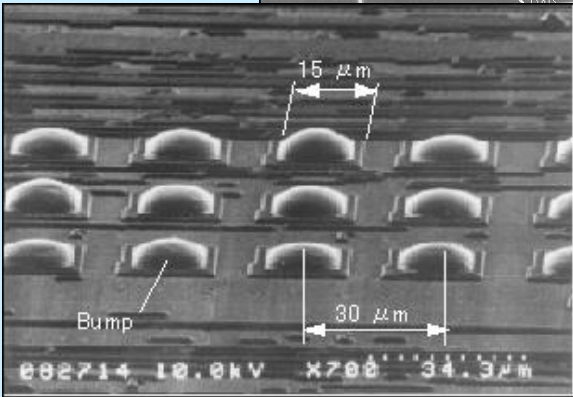
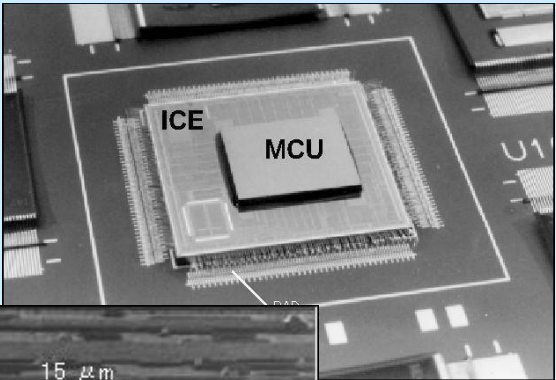
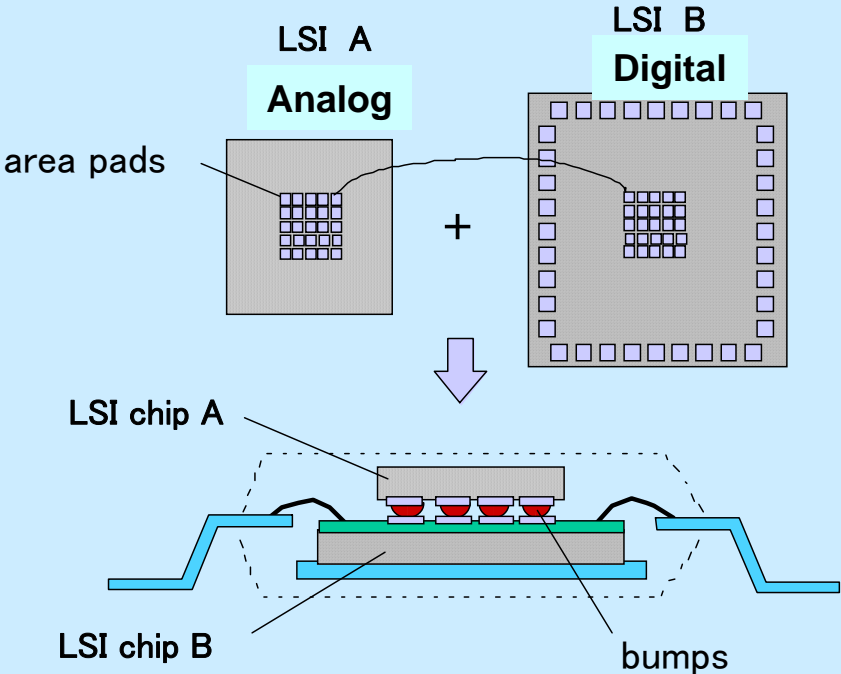
Area: 1/50

Pd: 1/20

# Solution 2: Advanced packaging technology

Some advanced packaging technologies will give the solution.

Analog: using not so much scaled technology.  
Digital: using scaled technology  
Connect with low parasitic cap. and inductance.



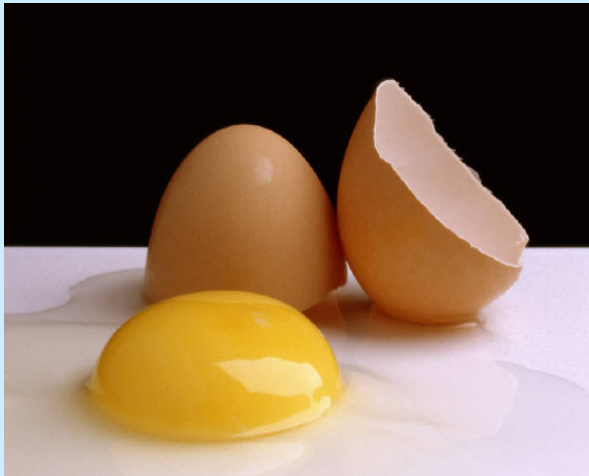
Chip On Chip technology

Same capacitance as on-chip interconnection.  
No interconnection inductance

# Future step: Mixed signal egg.

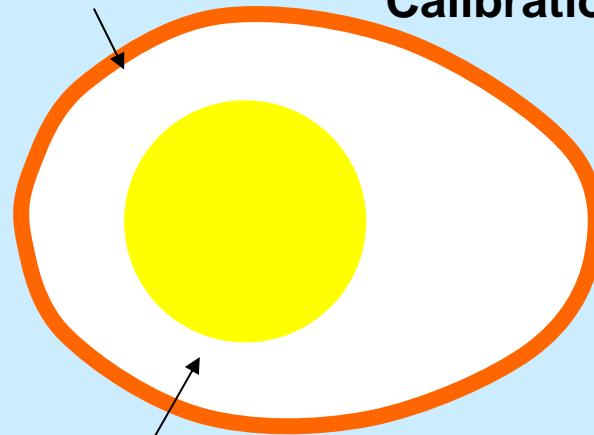
Analog helps digital (digital network and storage...).  
Next step is digital must help analog.

Mixed signal egg ( Analog yolk and white with digital shell)



**Digital shell**

Sustain the analog egg.  
Calibration and adjustment.



**Analog yolk and white**

Ultra-low power signal processing (Weak inversion)  
Ultra-high speed signal processing

**But, very delicate and fancy**

# Summary

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- The mixed signal (Analog+Digital) is essential for almost all the systems. Not analog only, not digital only.
- Effective modeling of analog parts and high speed concurrent simulation with digital is vital for design.
- CMOS is very powerful technology for analog, as well as digital, but scaling limitation is reaching.
- The collaboration between analog and digital, and advanced packaging technology will bring us effective solutions.