SoC and SiP technology for digital consumer electronic systems

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- **Digital consumer electronic systems and SoC**
- **SoC technology for the future digital consumer electronic systems**
- **Module and SiP technology for the future digital consumer electronic systems**
- **Development management**

Digital consumer electronic systems and SoC

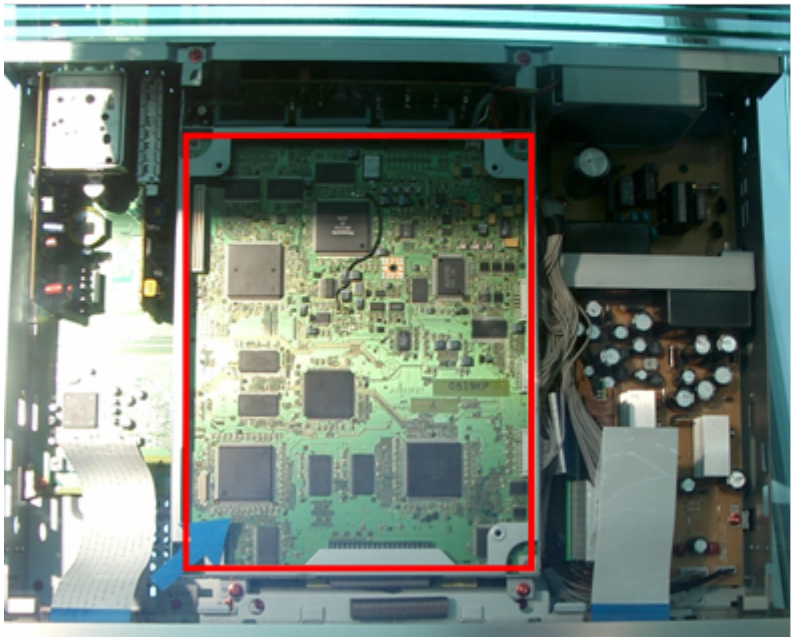
Digital consumer era

The digital consumer era has emerged.

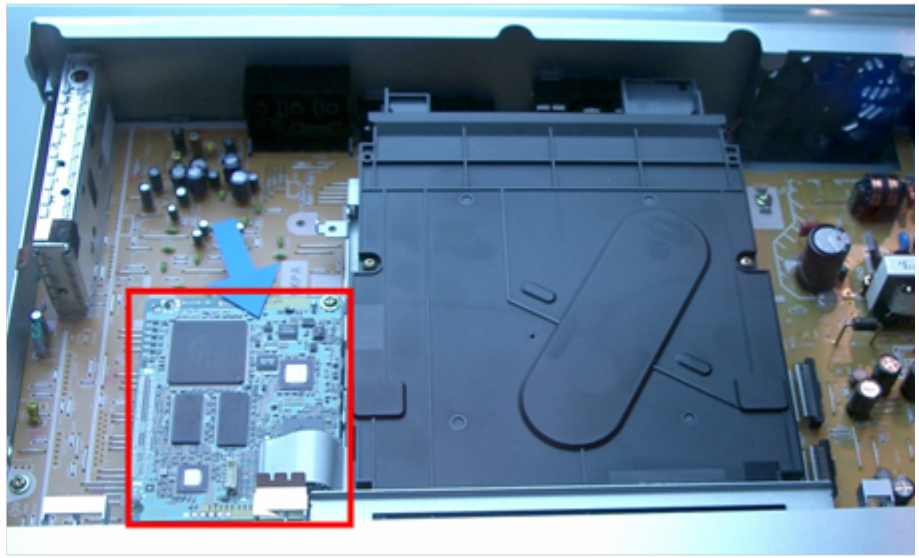
Contribution of SoC

SoC has contributed to the commercialization of the digital consumer technology. The performance has increased and the cost has decreased, drastically.

Model; Year of 2000

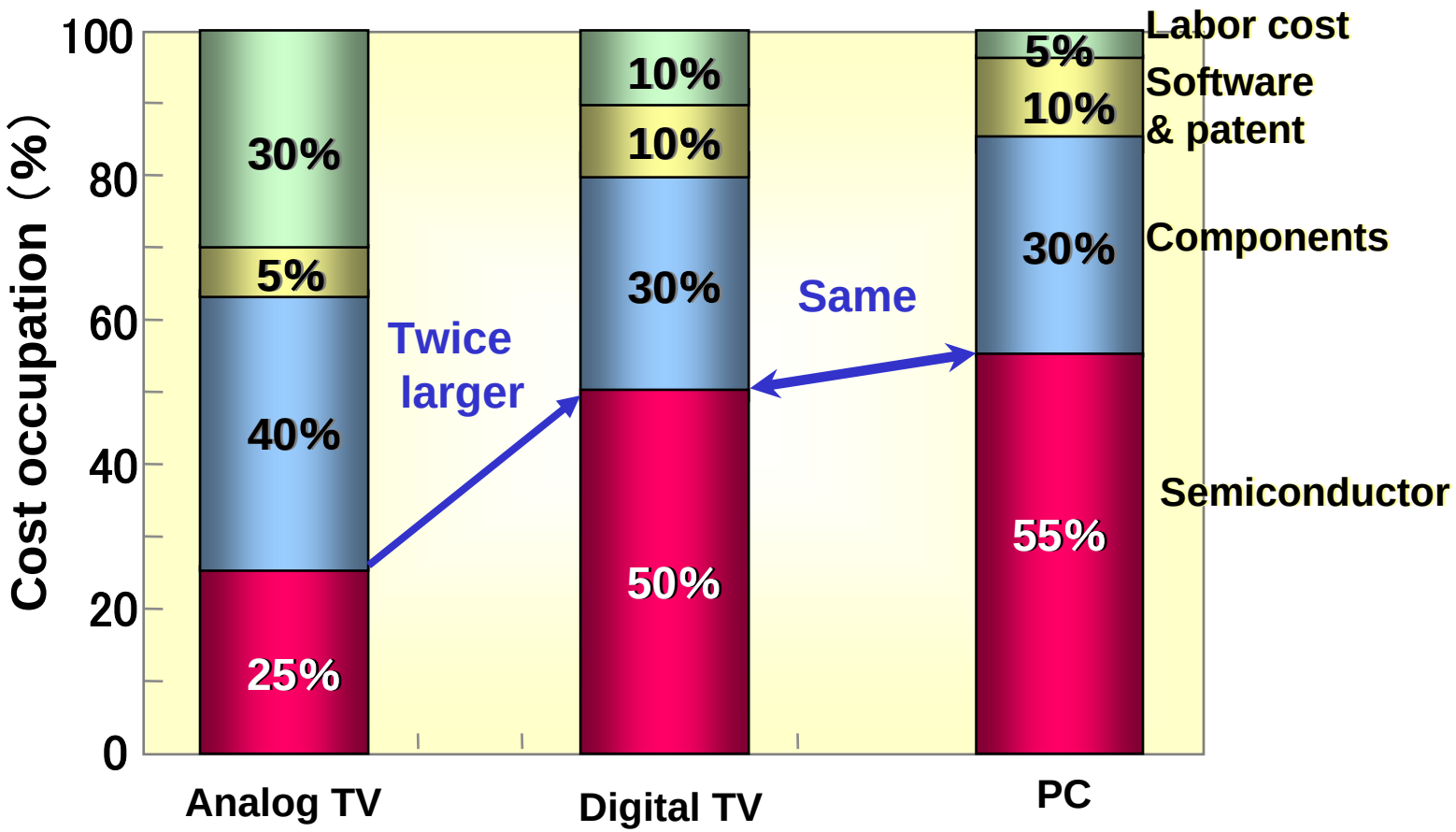


Model; Year of 2003



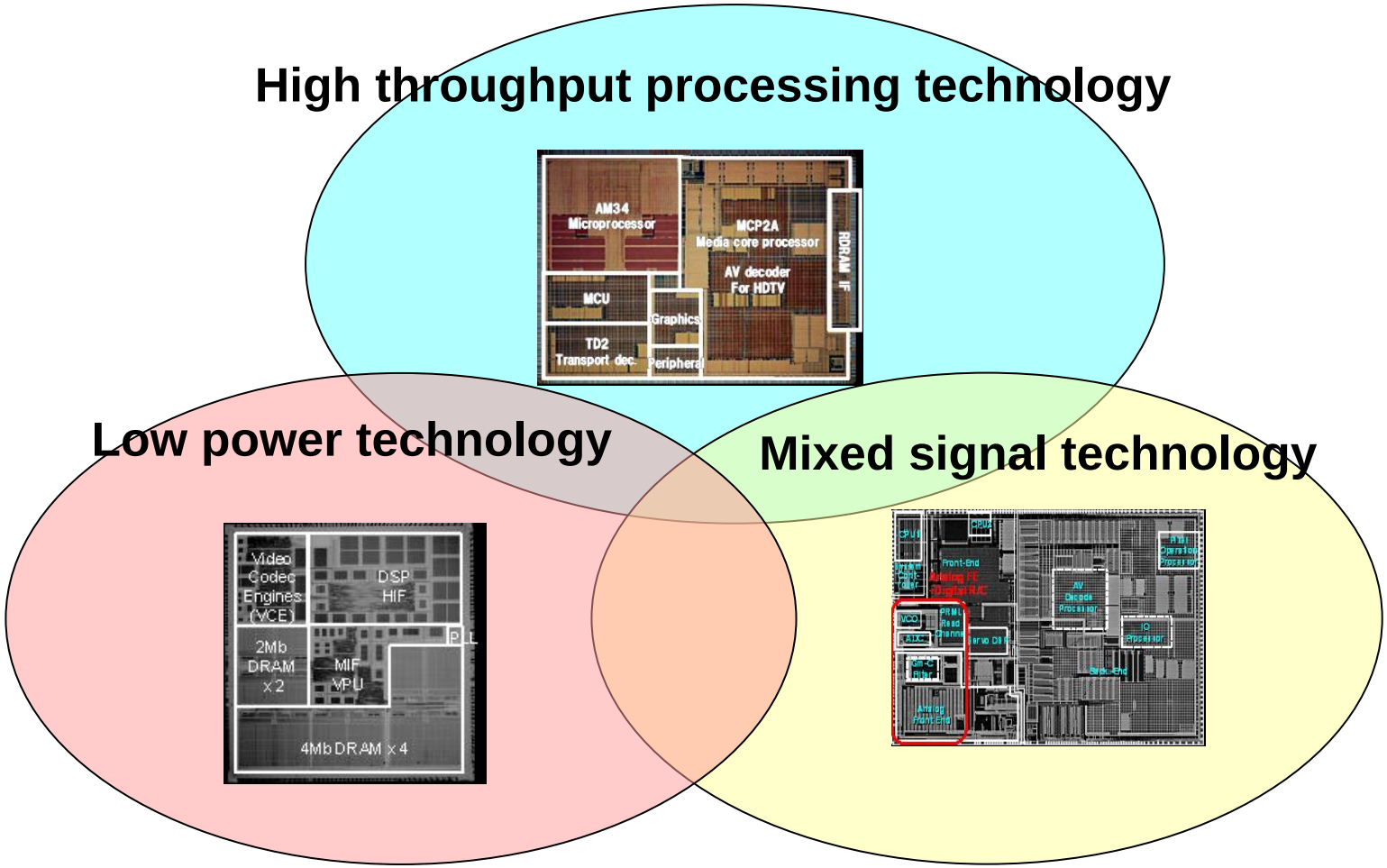
Position of SoC in CE electronics

The digitalization of the CE systems have raised the position of the semiconductor and SoC. About 50% of total cost is due to semiconductors.



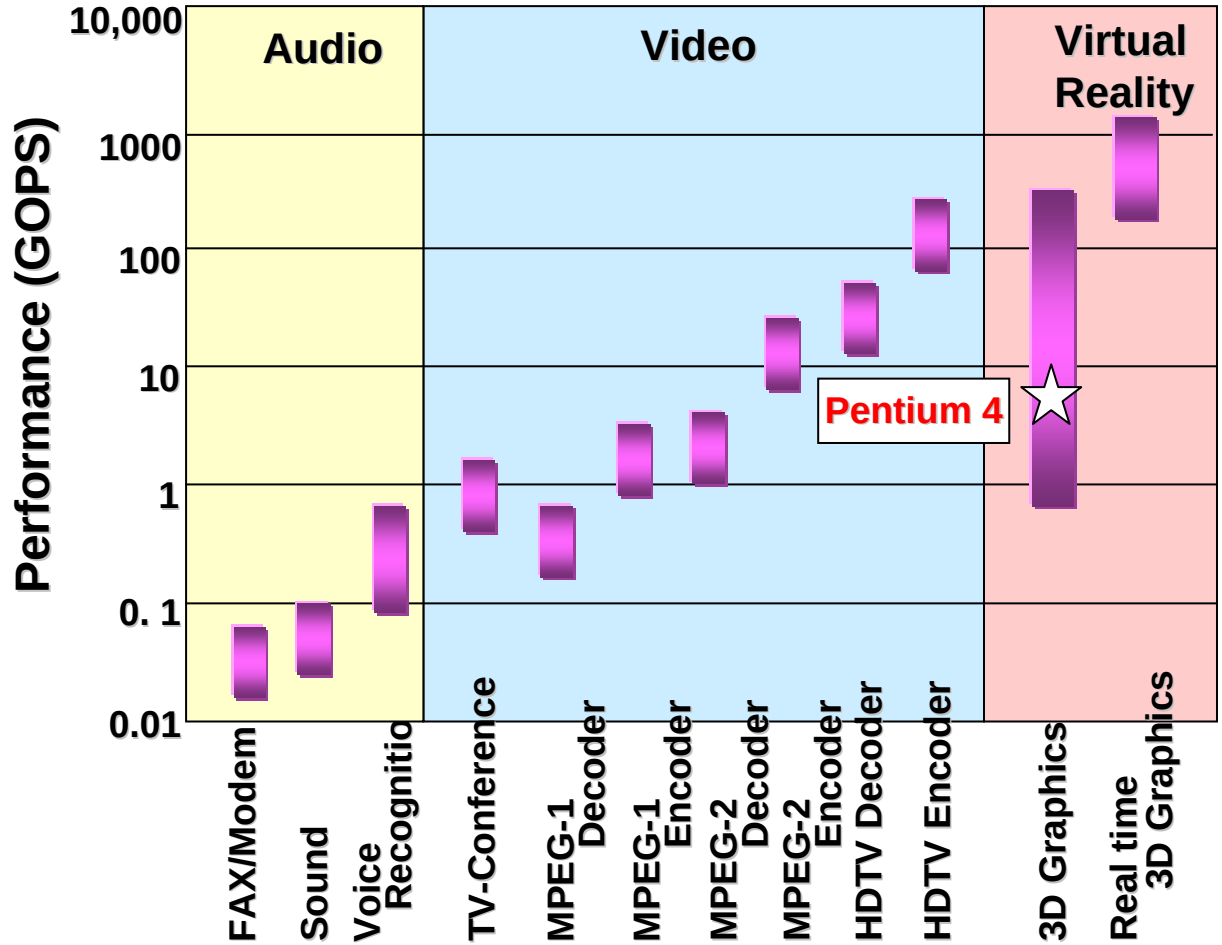
SoC technologies for digital CE

Digital CE systems need these basic SoC technologies.



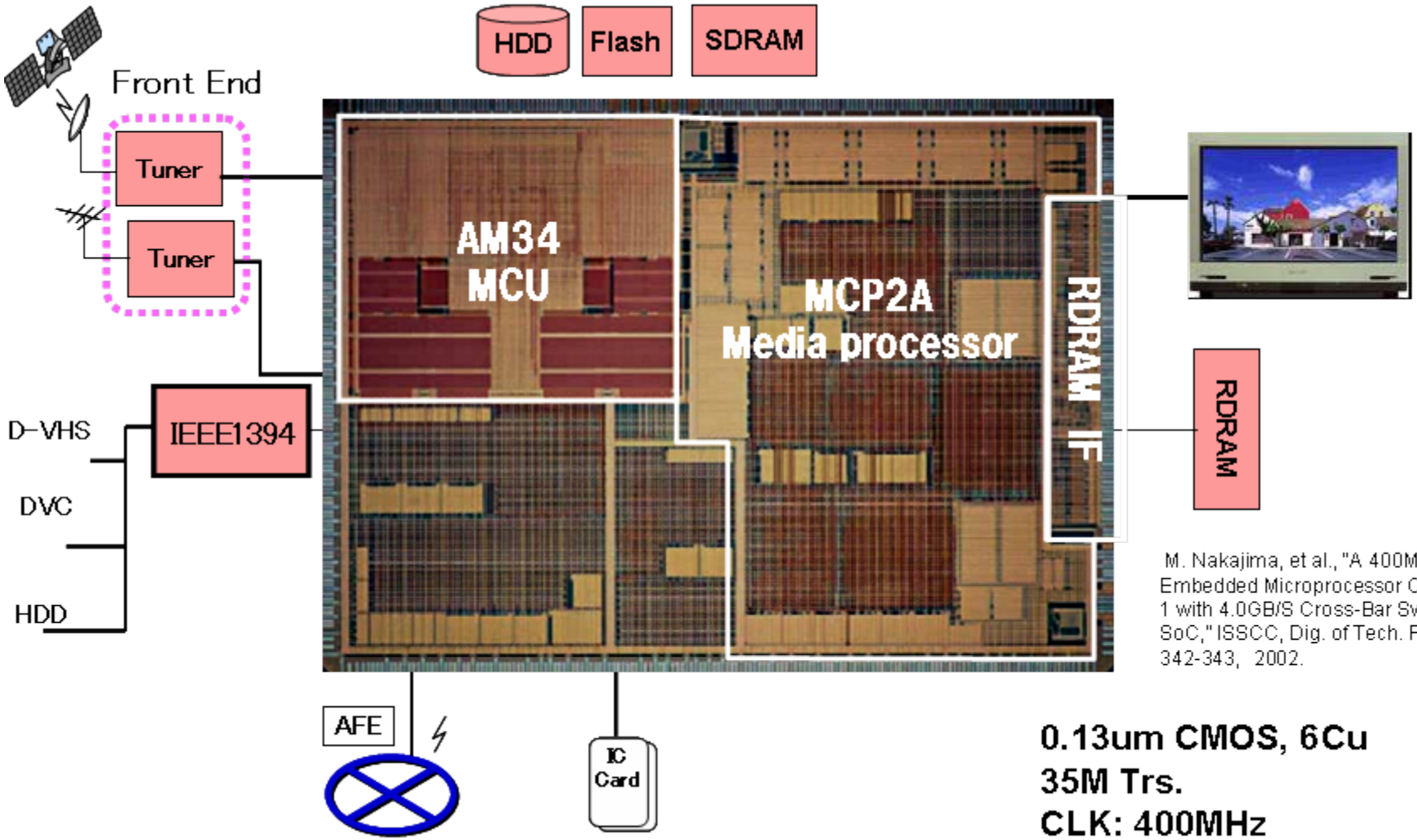
Needed performance for digital video

Necessary performance for the digital video system is one or two order higher than that of PC. Digital CE systems have needed for the progress of the LSI technology.



SoC for Digital TV systems

The progress of LSI technology has realized one chip digital TV systems.



M. Nakajima, et al., "A 400MHz 32b Embedded Microprocessor Core AM34-1 with 4.0GB/S Cross-Bar Switch for SoC," ISSCC, Dig. of Tech. Papers, pp. 342-343, 2002.

0.13um CMOS, 6Cu
35M Trs.
CLK: 400MHz

Low power SoC

Low power, yet high performance SoCs are required for the CE systems.

MPEG4 Codec

0.18um e-DRAM
31M Tr
90 mW@54MHz

1.5 GOPS: Simple@L1
12 GOPS: Simple@L3
6 GOPS: Core@L1

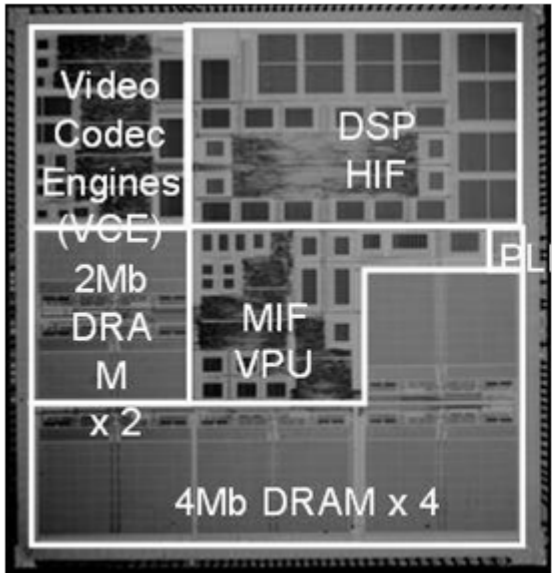
T. Hashimoto, et al., "A 90mW MPEG4 Video Codec LSI with the Capability for Core Profile," ISSCC, Dig. of Tech. Papers, pp. 140-141, 2001.

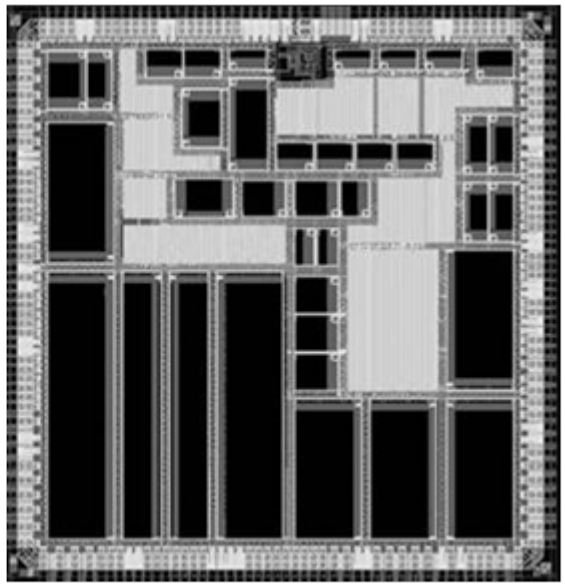
MPEG4 Decoder

0.18um CMOS
11M Tr
11 mW@27/54MHz

M. Ohashi, et al., "A 27MHz 11.1 mW MPEG4 Video Decoder LSI for Mobile Application," ISSCC, Dig. of Tech. Papers, pp. 366-367, 2002.

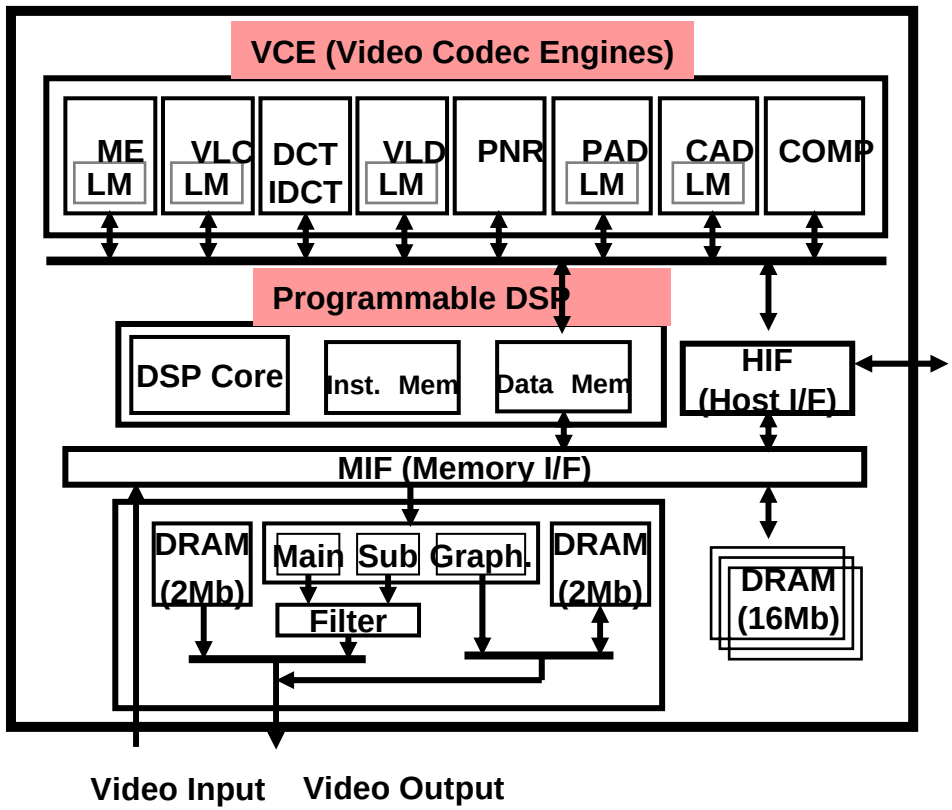
15fps (Core@L1 decode)





Low power technology

Low power and high performance architecture dedicated for the application has been developed.



1.5 GOPS: Simple@L1
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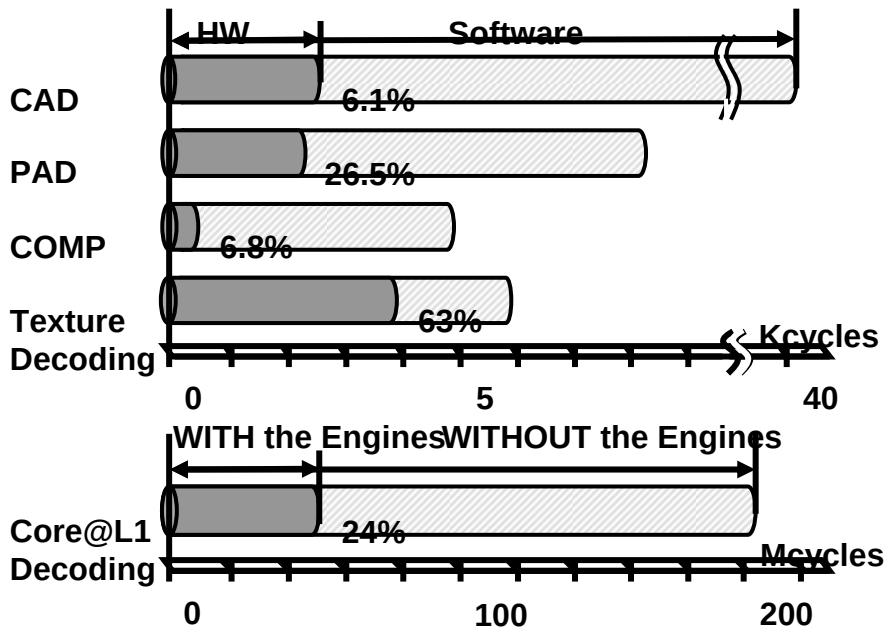
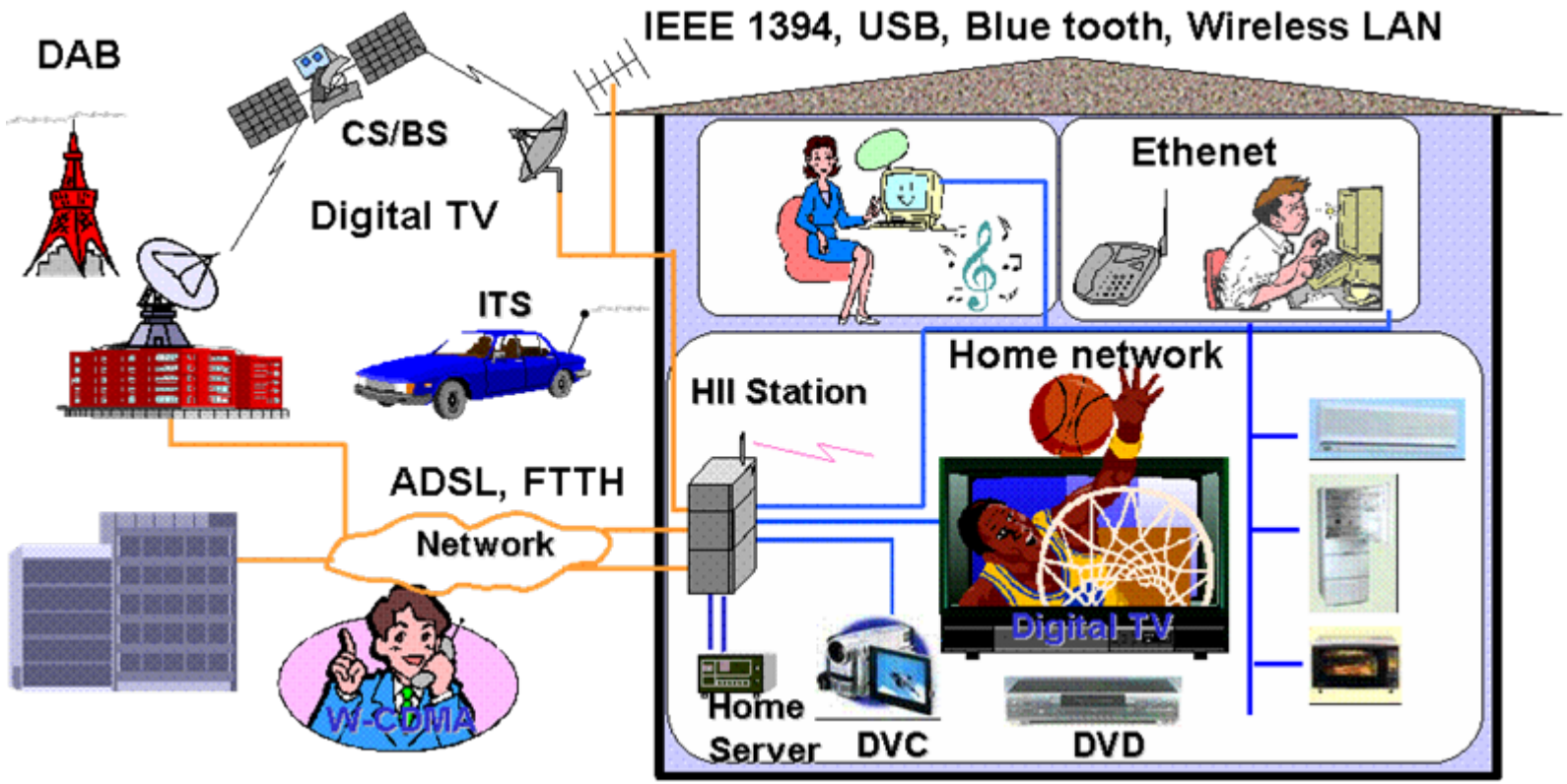


Digital network society

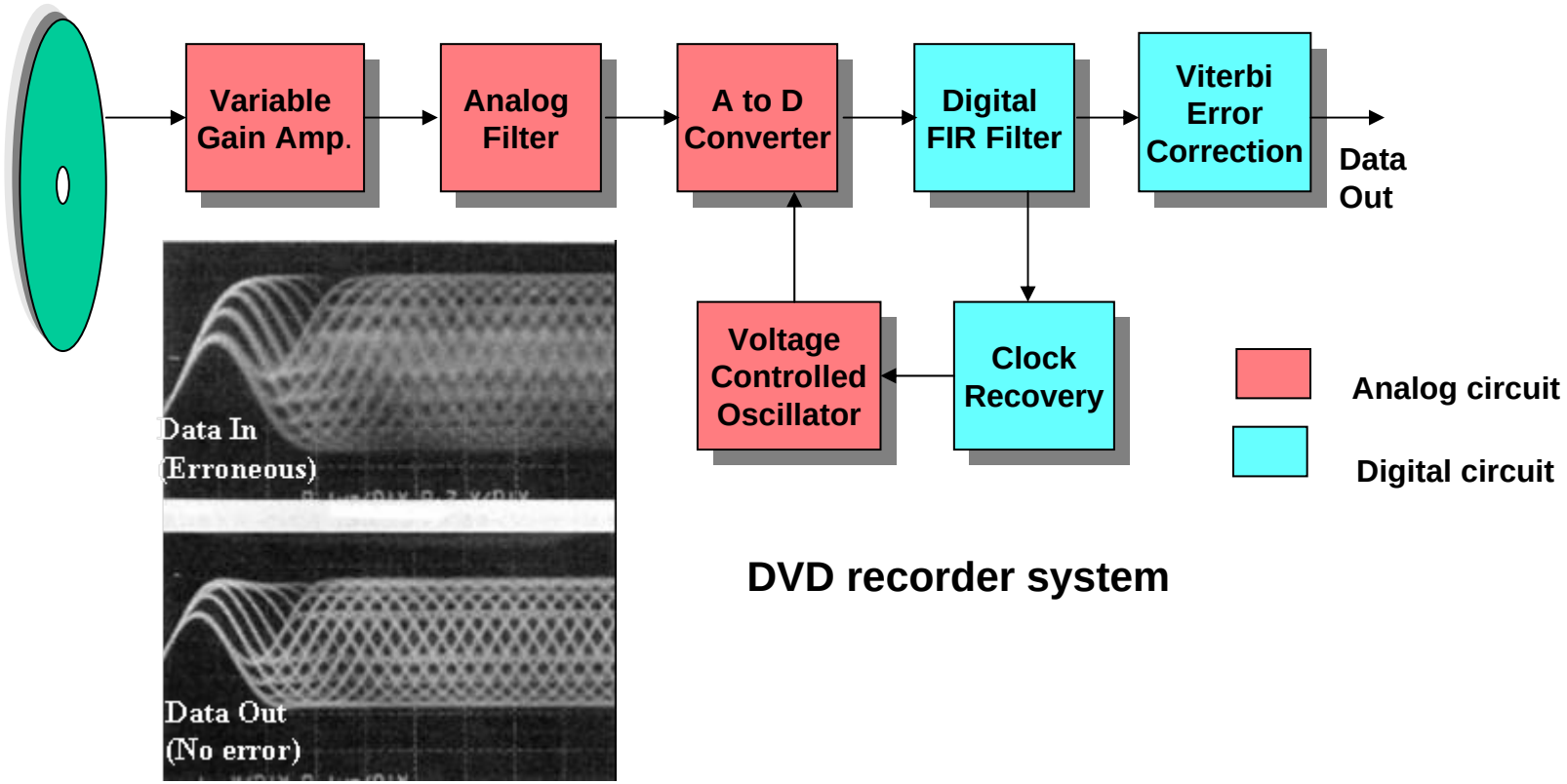
The digital network era has emerged. All digital consumer systems will connect each other through the networks.
The mixed signal (RF) technology plays an important role.



Mixed signal technology

Current electric systems need the mixed signal technology.
SoC needs analog circuits.

- **Digital networks, communication, broad casting (DTV, ADSL, Ethernet, USB）**
- **Digital recording（HDD, DVD, DVC）**
- **Digital camera and display**



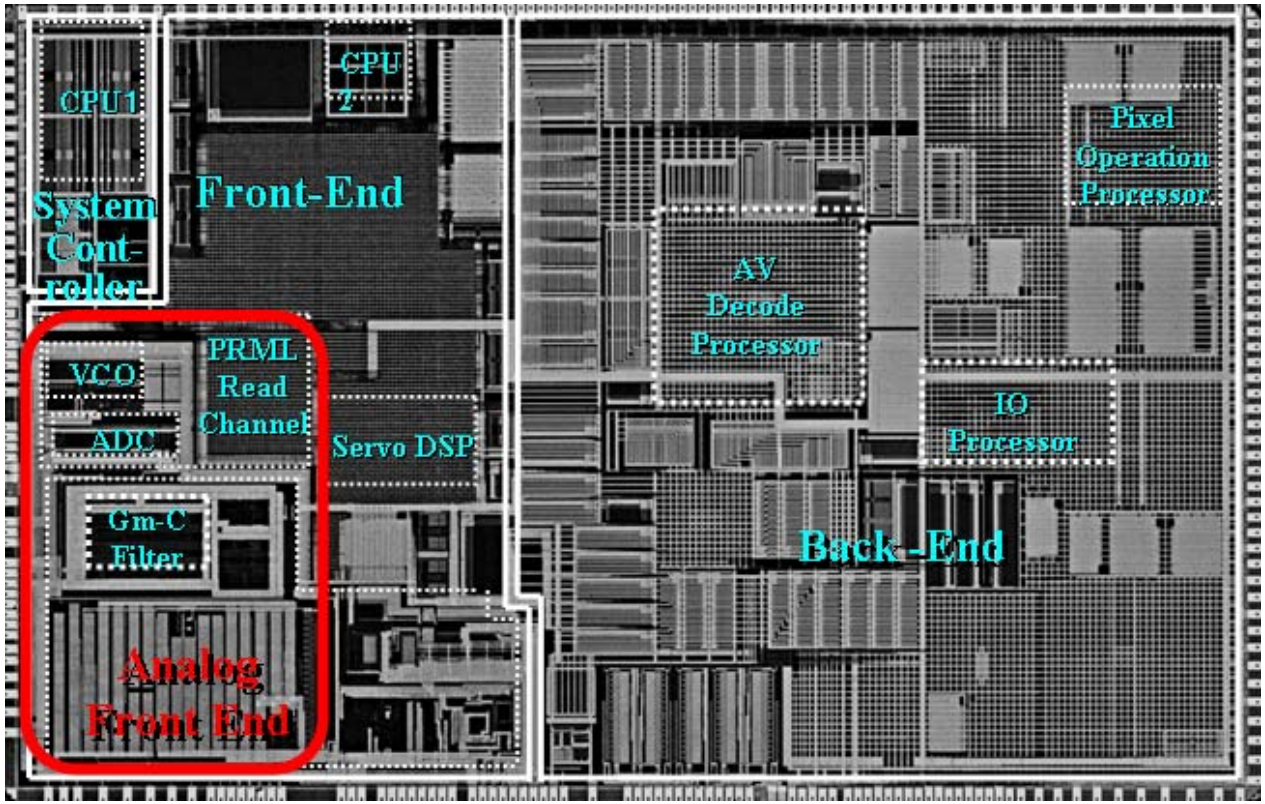
DVD recorder system

Mixed signal SoC

The mixed signal SoC technology has realized one chip DVD system.

0.13um, Cu 6Layer, 24MTr

Okamoto, et al., ISSCC 2003



SoC technologies for digital CE

Digital CE systems have been realized by the progress of SoC technology.

System requirements

High throughput processing

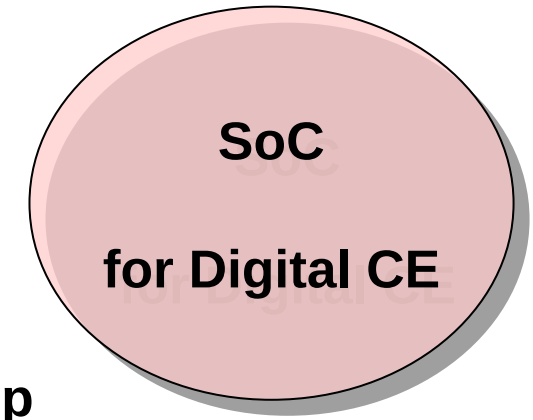
10-100 GOPS

Low power

2-3 W for conventional
100mW for portable

Total system on a chip

Analog and interface



SoC technologies

Technology scaling

Moor's law

Dedicated architecture for the application

Massive parallel
Media processor
Dedicated processor engine

Mixed signal technology

On-chip analog
RF-CMOS

Function of Consumer Electronics

Audio recording and playback

Video recording and playback

Putting broadcasting programs on Radio or TV

Personal communication

Personal amusement

Essential trends of consumer electronics

Lighter, Smaller, Cheaper

Military → Industrial → Home →Personal →Portable

Vacuum tube →Transistor →IC →LSI →SoC

→ Solid state

(CRT → LCD, EL)

(Tape → MD → HDD → Semiconductor memory)

Single function → Multi functions (Cellular phone)

Analog → Digital → Network

Digitalization

- Free from the materials
  Analog depends on the materials, however digital is free from the materials.
  - Multiple use without degradation → Copy issues
  - The fabrication technology doesn't affect the quality so much → Easy to make → Rapid cost decrease

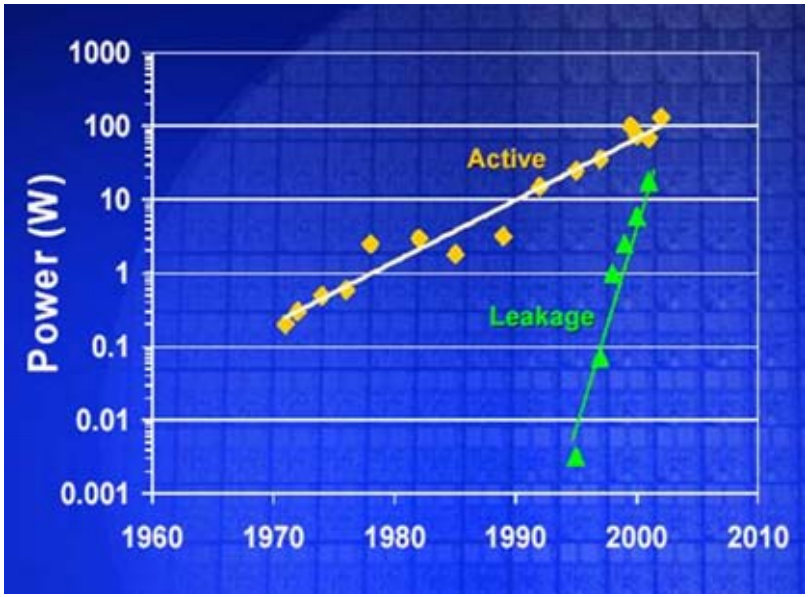
- Unification
  Once digitized, data looses its native properties.
  - Loosing individuality and going unification
  - Move to the software oriented technology
  - Networking and broadcasting

SoC technology for the future digital consumer electronic systems

Biggest Crisis of LSI technology

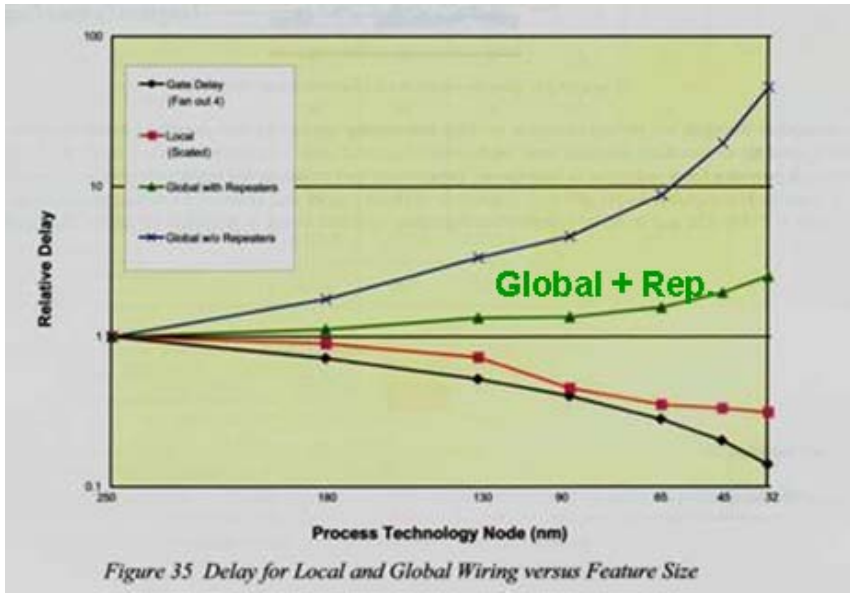
Power consumption has already reached the limitation.
The wire delay can't be reduced any more.
These will change the SoC architecture.

Power consumption of MPU



Gordon E. Moore, ISSCC 2003.

Wire delay roadmap



ITRS 2001 Edition, pp. 261.

Processor system structure

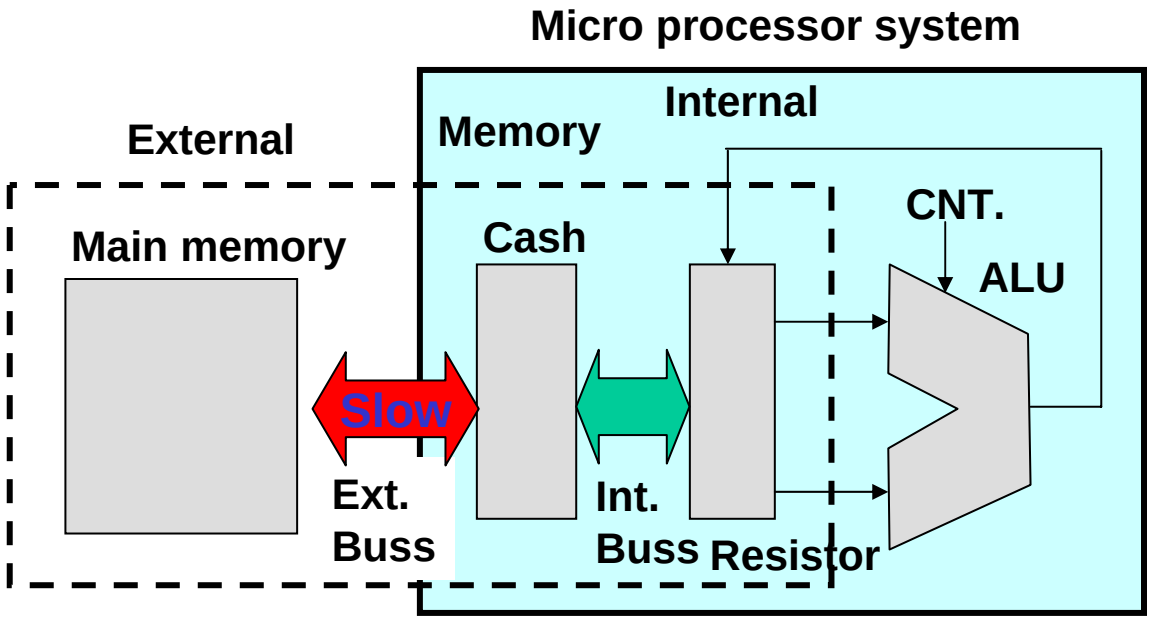
Issue: 2 or 3 operations / clock (Very slow)

High throughput → High freq. → High power consumption.

Solution: Parallel processing units, multi-core, PE engine.

Issue: Memory access time takes 3x longer time than execution time.

Solution: CoC technology, instead of conventional ext. buss.



Architecture and power consumption

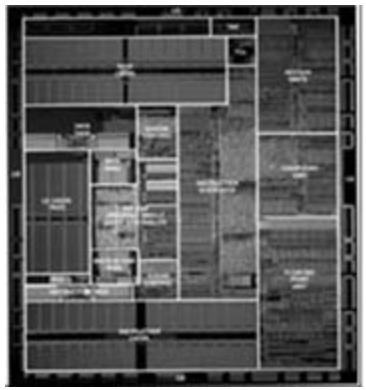
The power crisis is not only due to the device technology but also due to the SoC architecture.

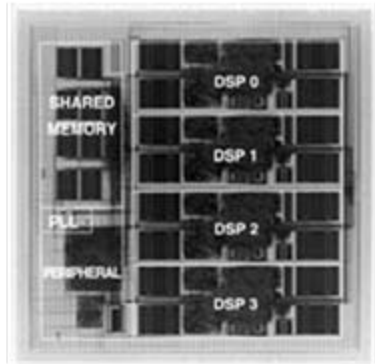
Software oriented ⟷ **Hardware oriented**

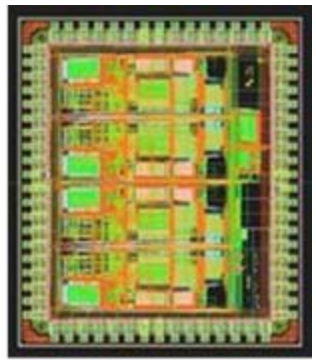
	MPU for PC	DSP	SoC for CE
Parallelism	2	16	96
GOPS	0.9	0.8	2.4
Pd (mW)	7000	110	12
Pd (mW)/GOPS	7800	138	5

3 order's magnitude of difference

Courtesy,
Prof. Brodersen,
UCB



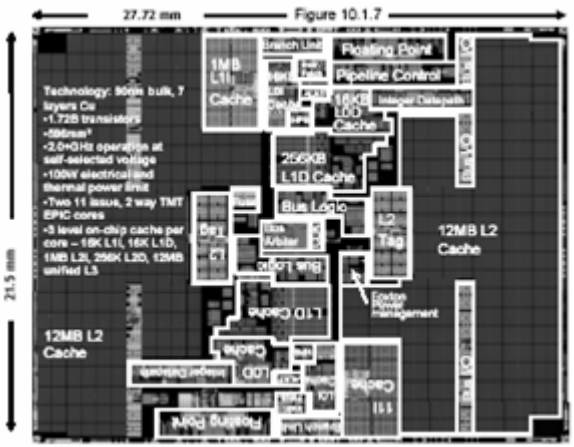




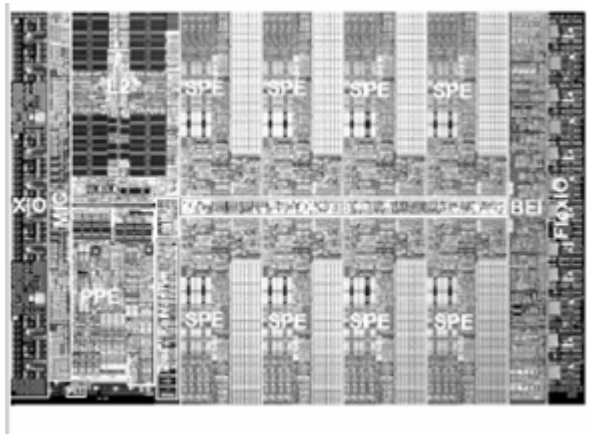
Multi-core processor

Several multi-core processors were announced on ISSCC 2005.

Intel *2 CPU*

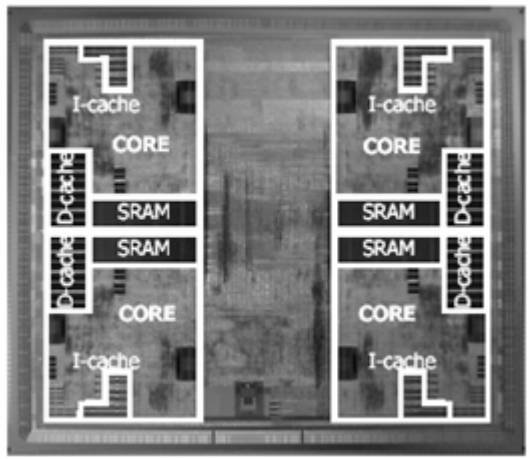


IBM, Sony, Toshiba *(1+8) CPU*



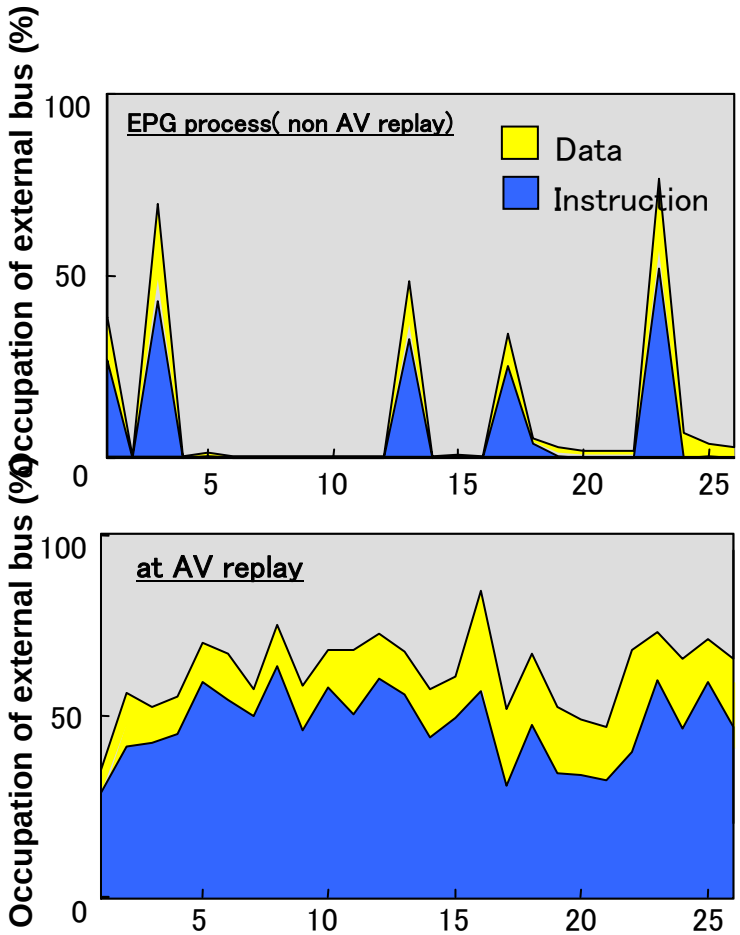
NEC *3 CPU*

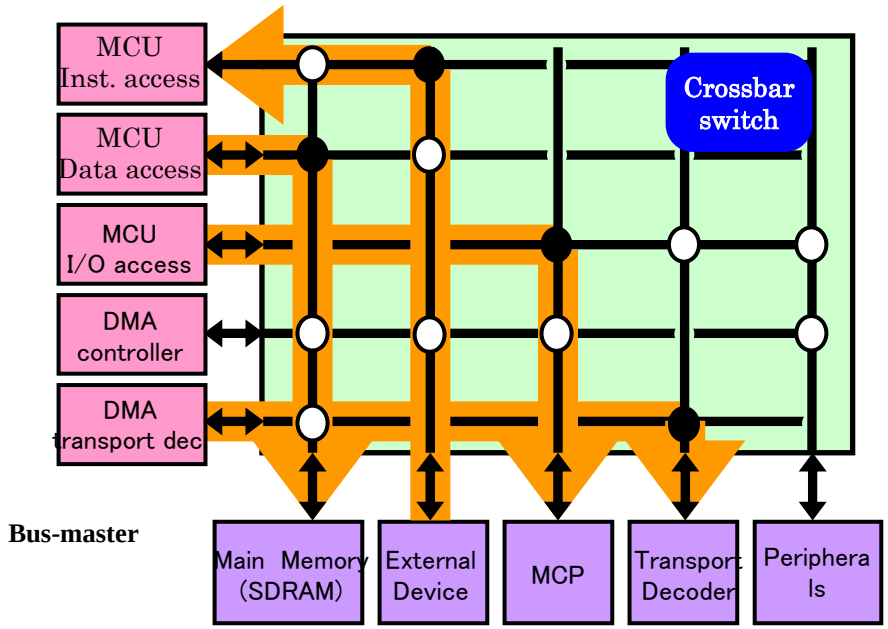
Fujitsu *8W VLIW*



Dedicated buss structure

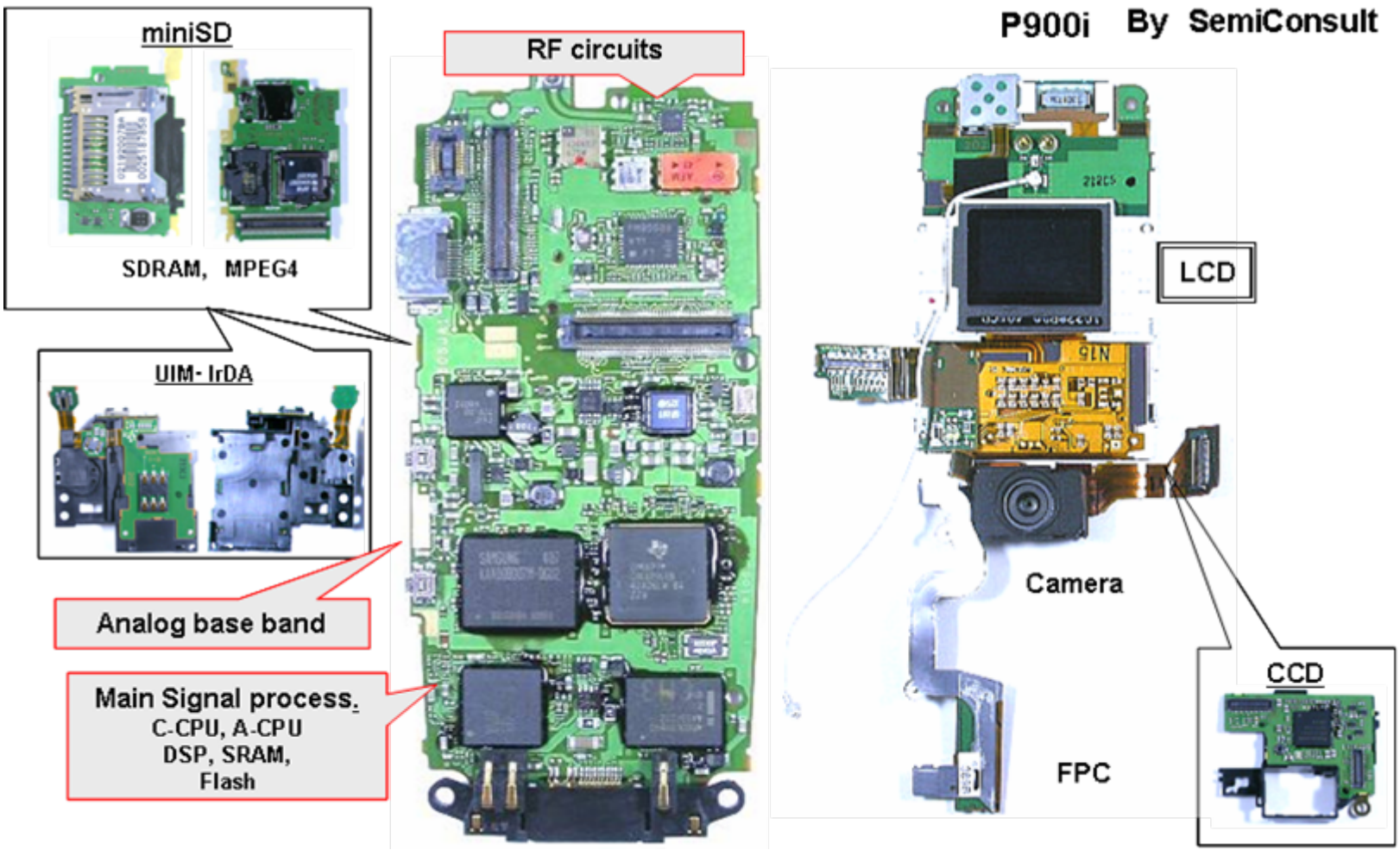
The occupation of an external buss at the AV processing is unacceptably high compared with that at the conventional PC processing.
Dedicated crossbar switch can increase processing throughput by a factor of 2.





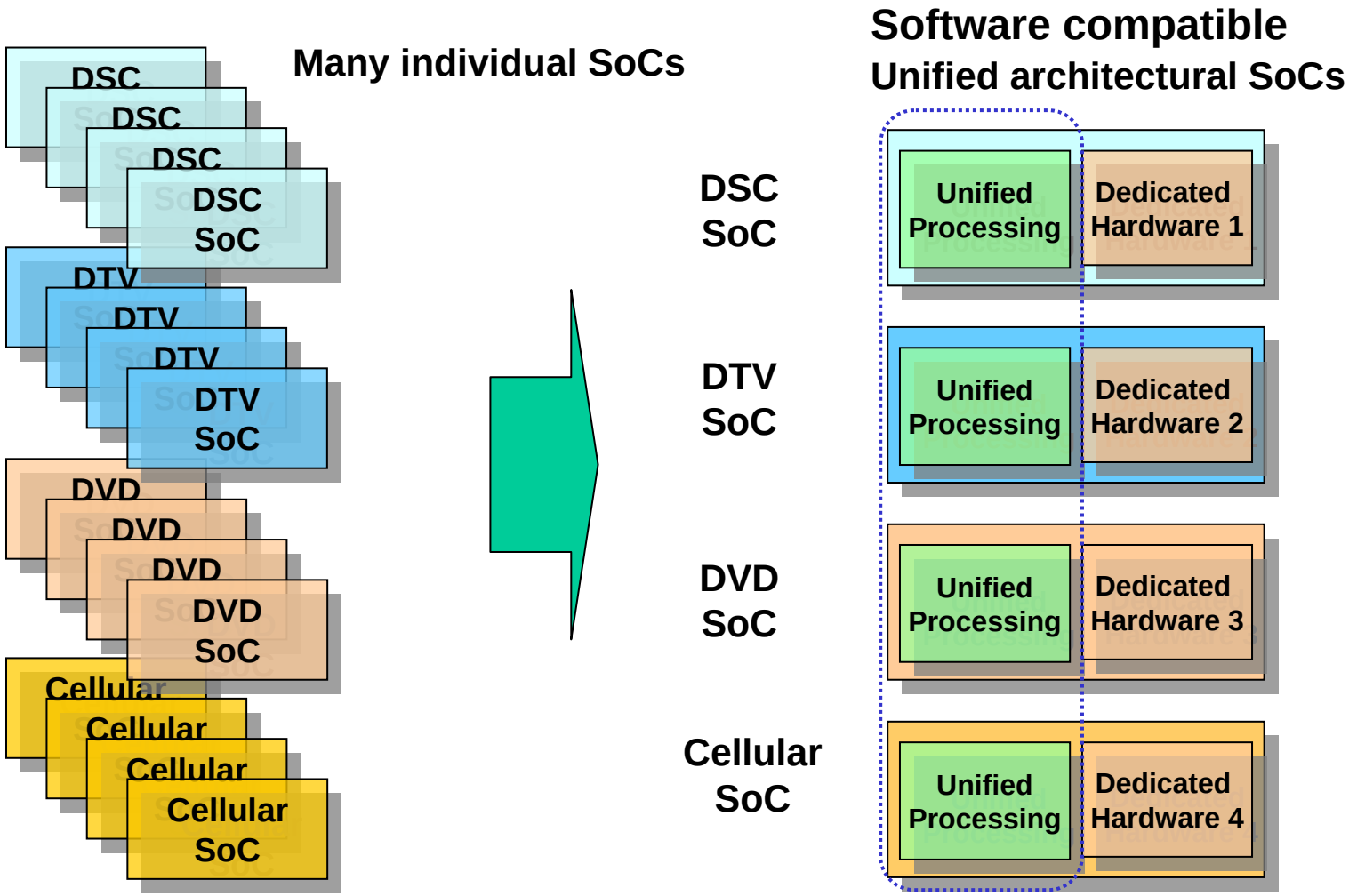
Convergence to cellular phone

Cellular phones will integrate almost all digital consumer functions.



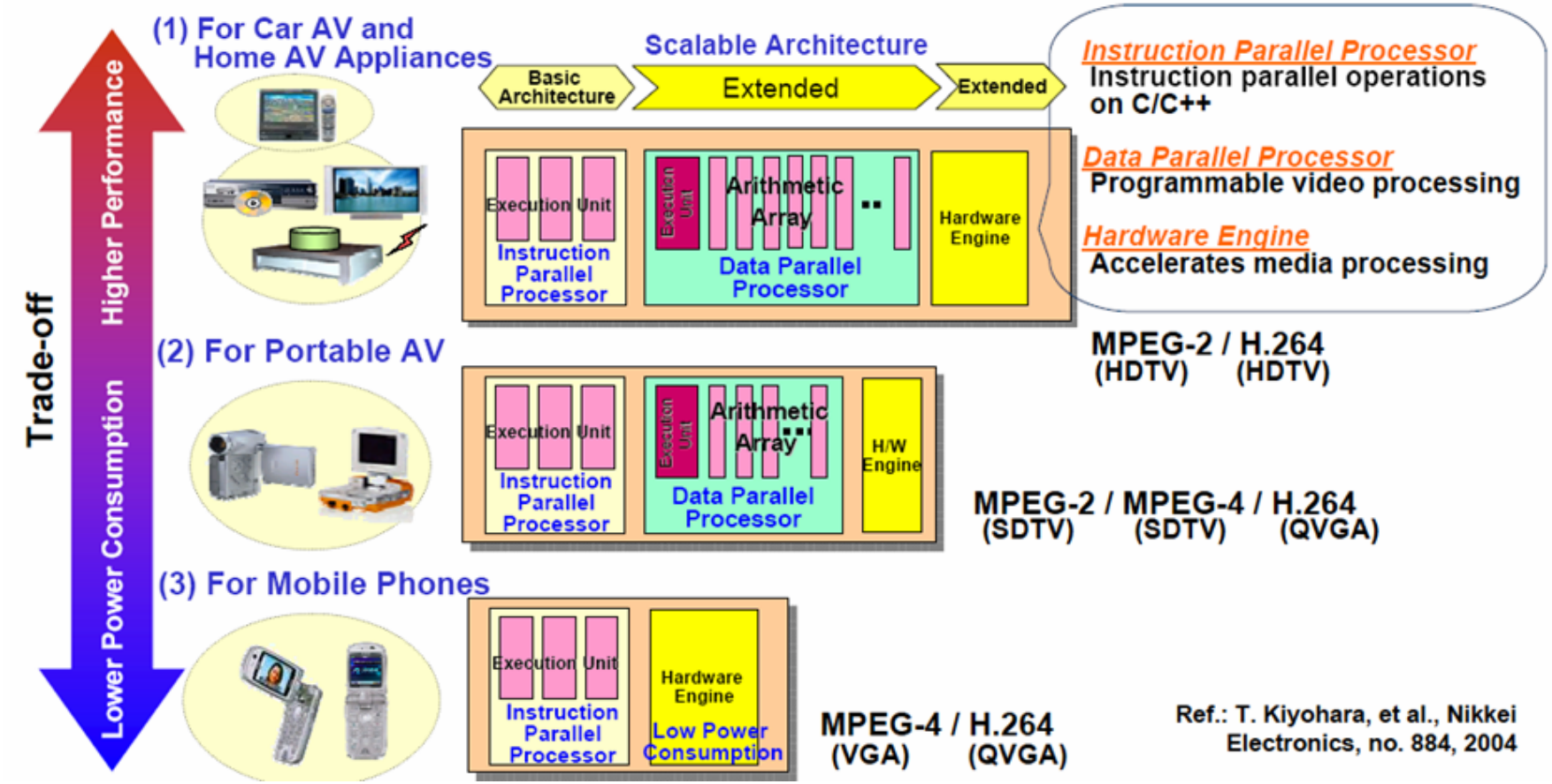
Direction of SoC for digital CE

Future SoC will use unified processor and dedicated circuits for several applications to increase the software development efficiency.



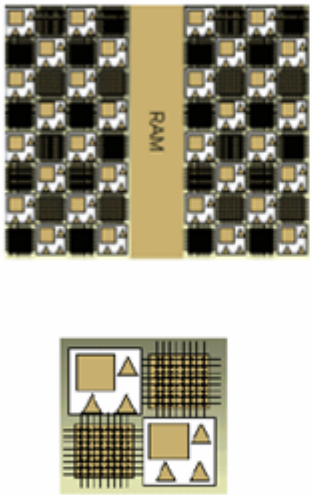
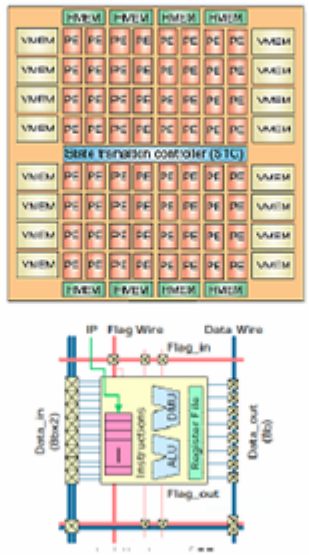
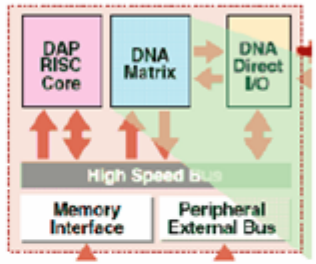
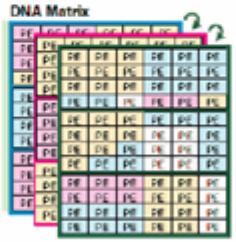
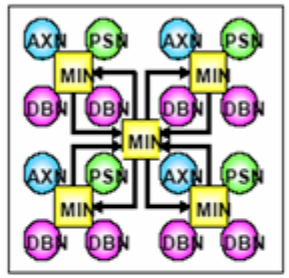
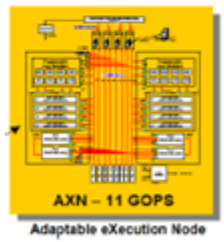
Unified architecture for digital CE

An unified and a scalable architecture is the direction.



Reconfigurable logic

Reconfigurable logics will be embedded onto SoC,

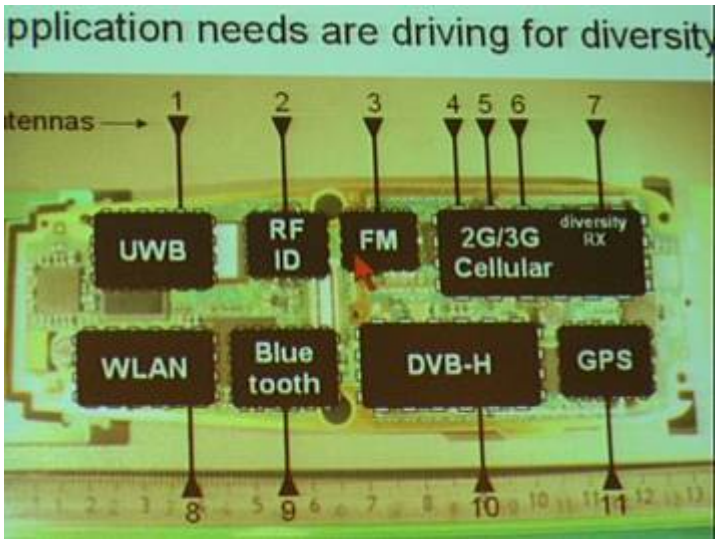
Company	Elixent	NEC	IP Flex	Quick Silver Tech
Granularity	Small (Arithmetic unit) ⟷ Large (Processor)			
Structure			 	 
Element	Homogeneous	Homogeneous	Heterogeneous	Heterogeneous

Ref.: Website of each company, see the last page.

Wireless communication

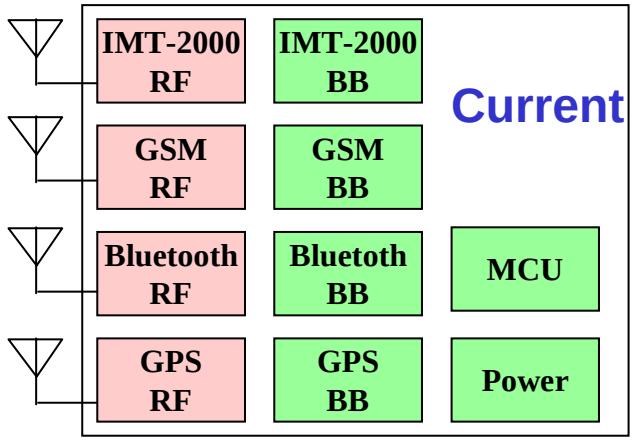
Cellular phones must need many wireless standards in the future.
RF circuits and DSP should be unified.
Re-configurability and Programmability are keys.

Future cellular phone needs 11 wireless standard!!



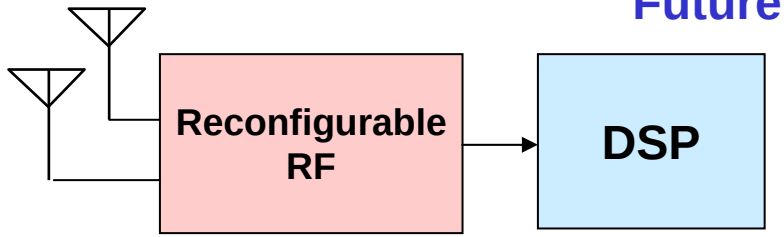
Yrjo Neuvo, ISSCC 2004, pp.32

Multi-standards and multi chips



Unification

Future

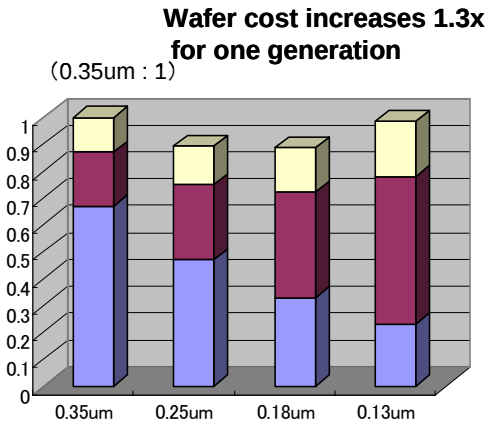


Unified wireless system

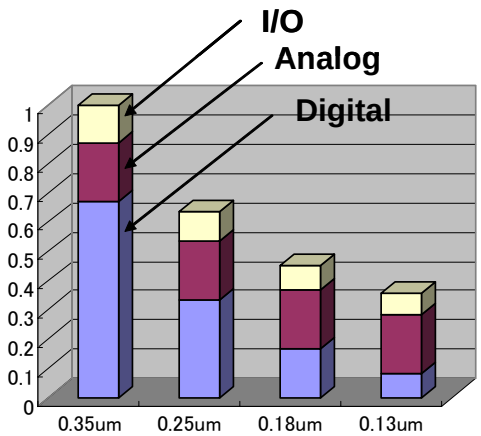
Issues of mixed signal technology

Mixed signal technology will continue to be needed to realize the interface , communications, and the network. However many issues will be faced.

1) Cost increase due to the difficulty of area reduction
2) Low voltage operation (<1.2V)
3) Low dynamic range
4) Low voltage gain

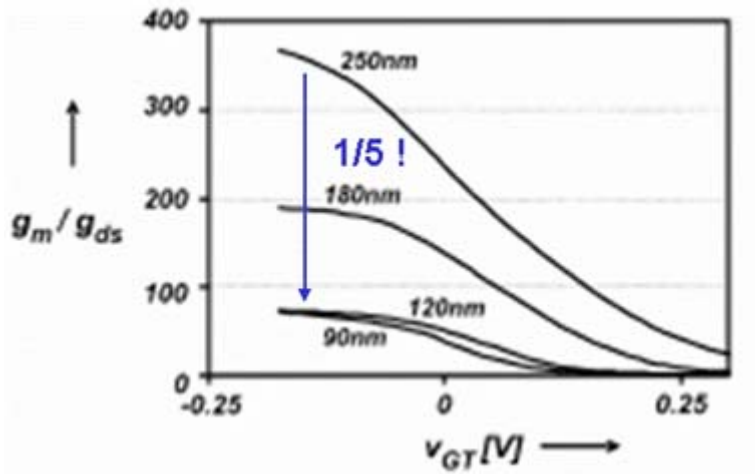


Chip cost



Chip area

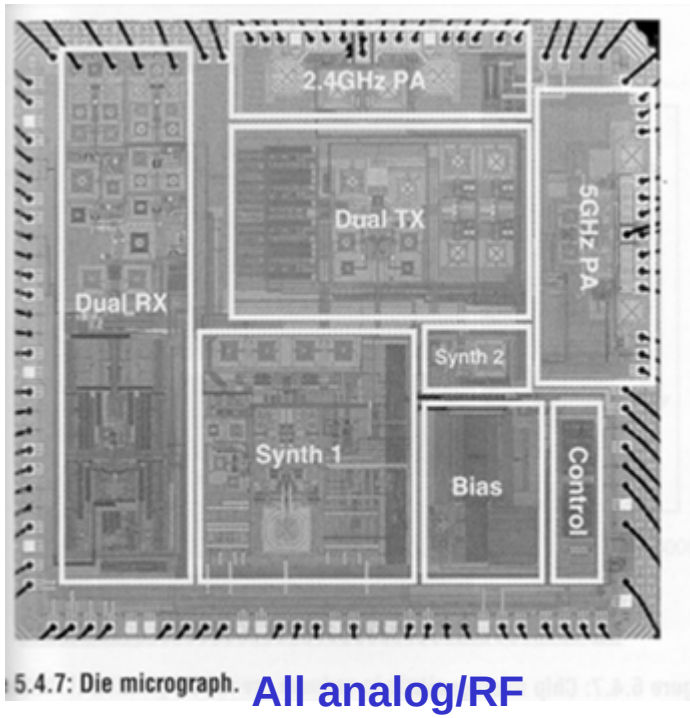
Voltage gain



Recent RF CMOS LSI

Mixed signal SoC has emerged for wireless communication systems.
Small analog/RF circuits is a key.

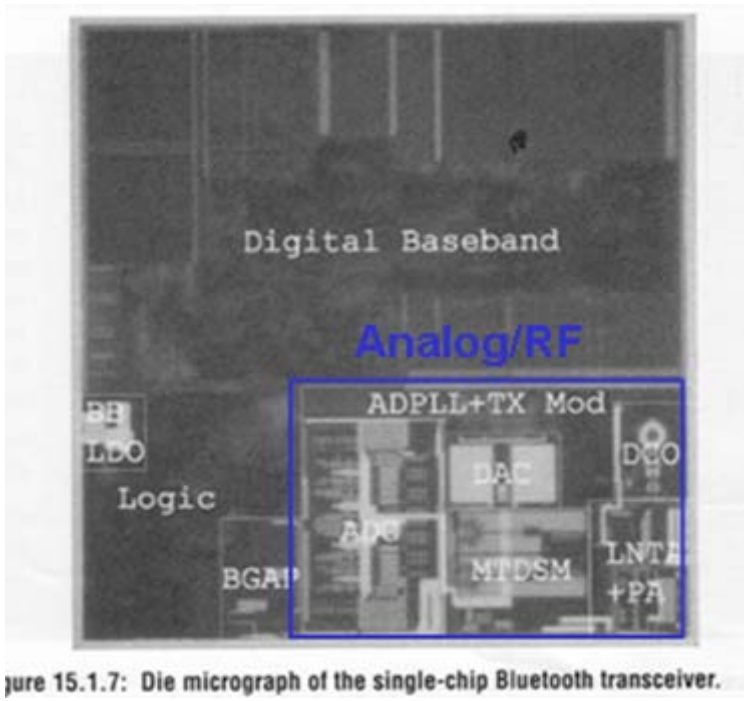
Wireless LAN, 802.11 a/b/g
0.25um, 2.5V, 23mm^2, 5GHz



5.4.7: Die micrograph. **All analog/RF**

SoC

Discrete-time Bluetooth
0.13um, 1.5V, 2.4GHz



ure 15.1.7: Die micrograph of the single-chip Bluetooth transceiver.

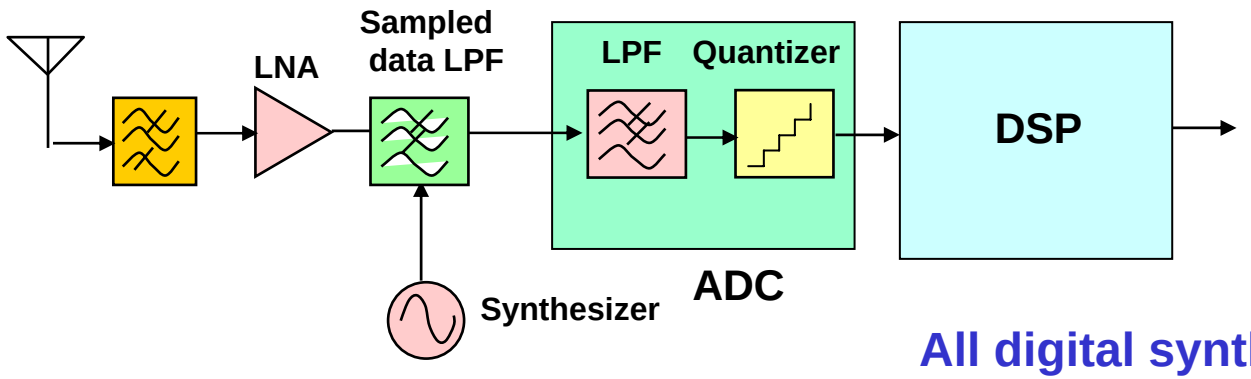
M. Zargari (Atheros), et al., ISSCC 2004, pp.96

K. Muhammad (TI), et al., ISSCC2004, pp.268

Digital oriented Wireless SoC architecture

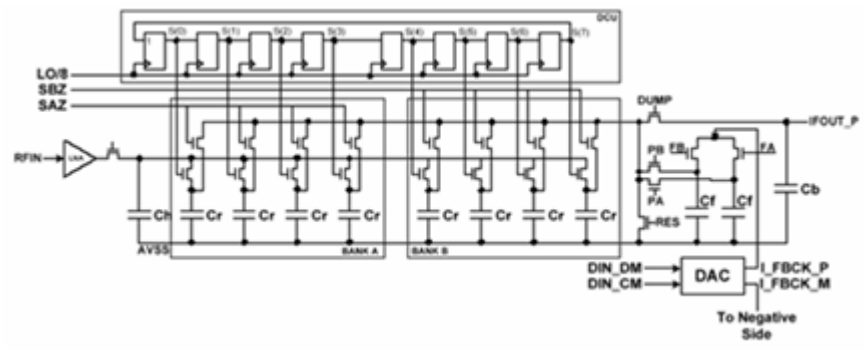
Analog/RF circuits will continue to be needed, but many analog RF circuits will be replaced by digital like circuits.

Digital oriented architecture

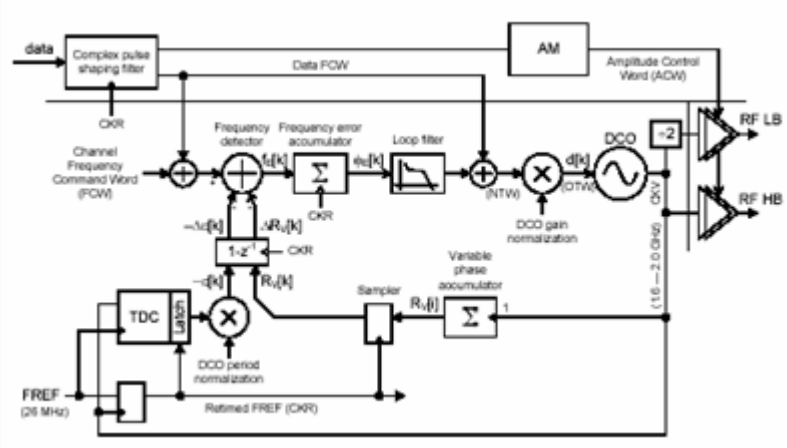


Bluetooth receiver
0.13um CMOS 1.5V

RF sampling mixer



All digital synthesizer



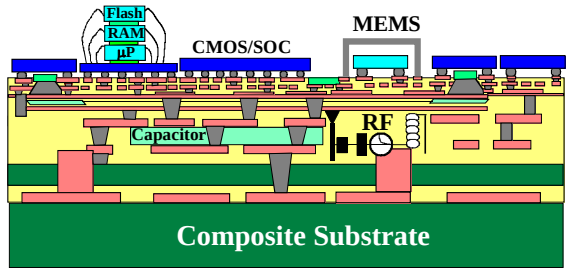
K. Muhammad (TI), et al., ISSCC2004, pp.268

Module and SiP technology for the future digital consumer electronic systems

Why module and SiP technology is important

- **Higher integration in small space**
  - **Cellular phone**
  - **Memory module**
- **Heterogeneous devices integration**
  - **Camera module: Lens + Imager + DSP + Flash+ (Power supply)**
  - **Wireless module: Filter, LCR, GaAs, Bipolar, CMOS**
- **Easy to use**
  - **Less adjustment points**
  - **Less EMI issues**
- **High cost and time performance**
  - **Optimum design rules; Analog + Digital**
  - **Can use cheep standard products; DRAM, Flash**
- **High performance and low power**
  - **SiS technology between CPU and DRAM**

RF module

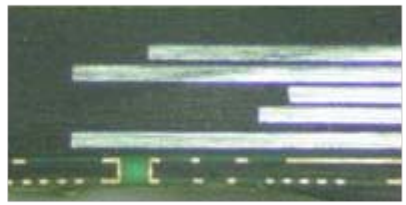


SiP for cellular phone

Many SiPs have been used in the cellular phone.

Chip stacked CSP

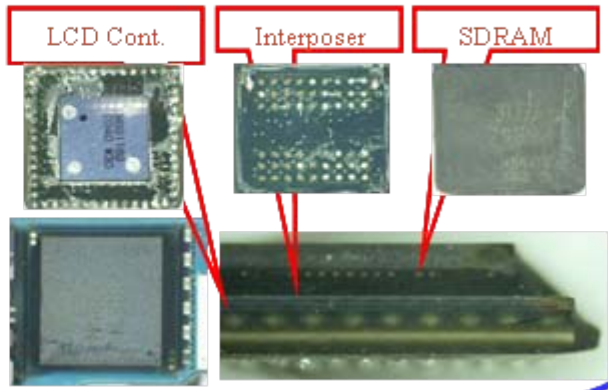
Package Stacked CSP



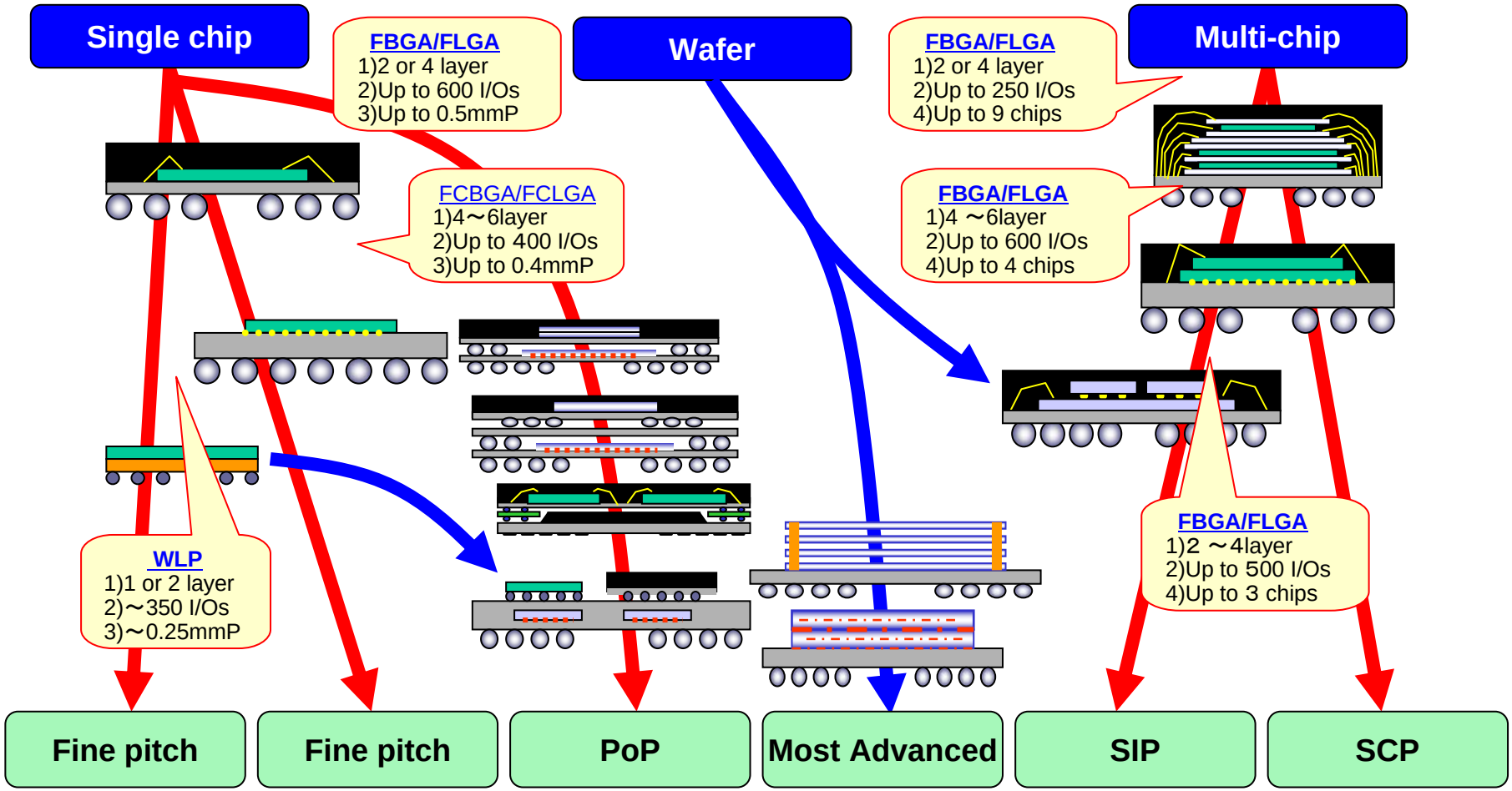
By SemiConsult

Chip stacked CSP

Package Stacked CSP



Direction of LSI Packages/Substrate

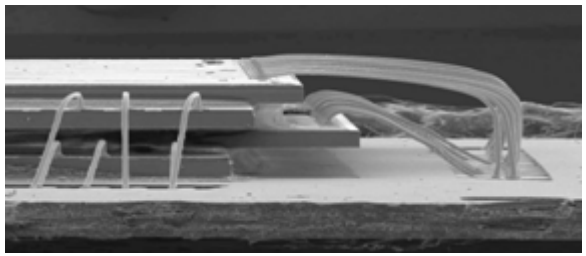
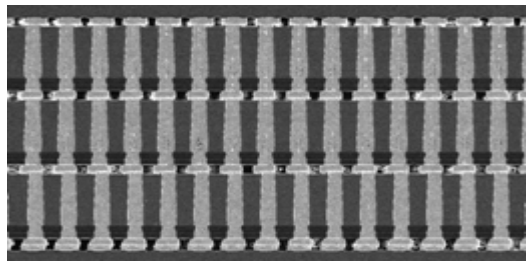


Remarks: 1) Necessary substrate layers, 2) Existing pin count, 3) Terminal pitch

By Semiconsult

3D integration technology

3D integration can realize high electric performances equal to on-chip interconnection.

	Conv. SiP	TCV
Figure		
Interconnect method	Wire bond	Bamp + Inner bia
Wire length	Several mm～several 10mm	<100 μm
Inductance	10 nH	**19 pH**
Capacitance	8 pF	**0.1 pF**
Minimum package size	> Chip size＋5 mm	Chip size
Thickness（4 chip）	490 μm	240 μm

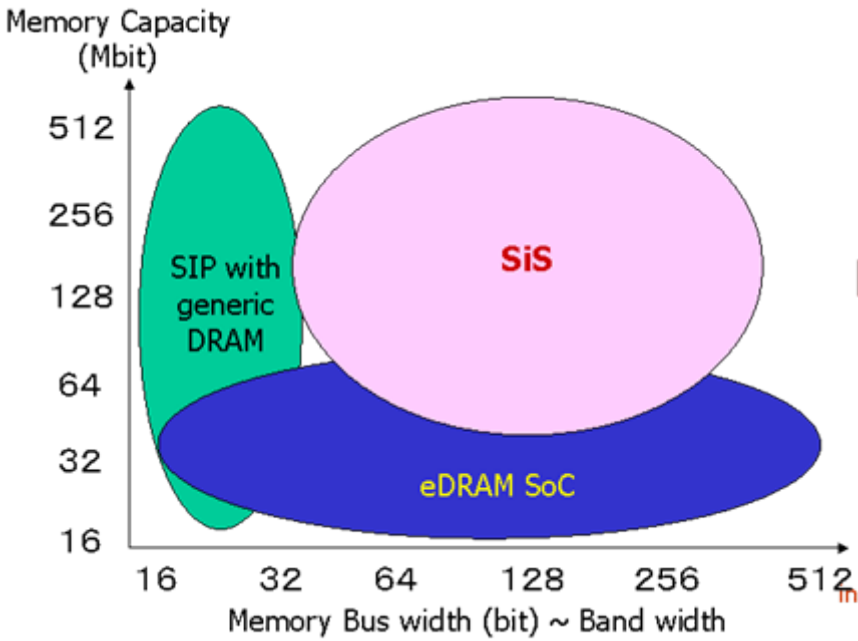
By Toshiba

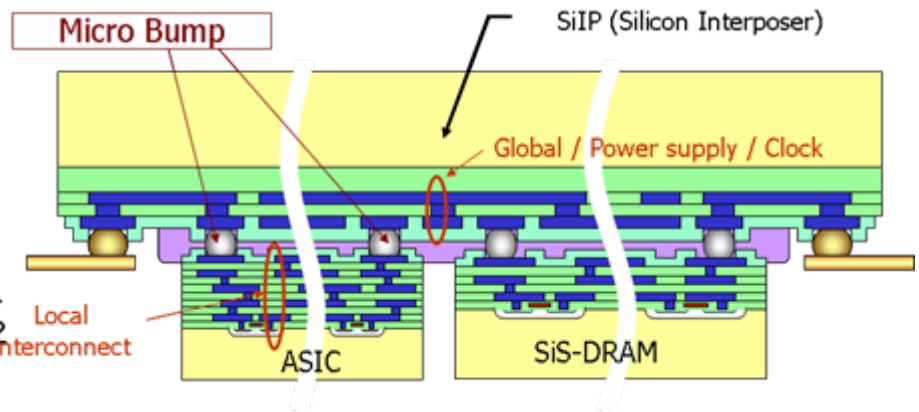
System in Silicon technology

Dedicated DRAM with 1024 (512 x 2) parallel connections realizes 19GB/s data transfer, which is higher than DDR3 (13GB/s).

- **Block-base SoC design and multi-chip fabrication**
- **The system is encapsulated by Silicon (→SiS)**
- **Global routing over different substrates using SiIP**
- **Micro-bumps for the high density connection**

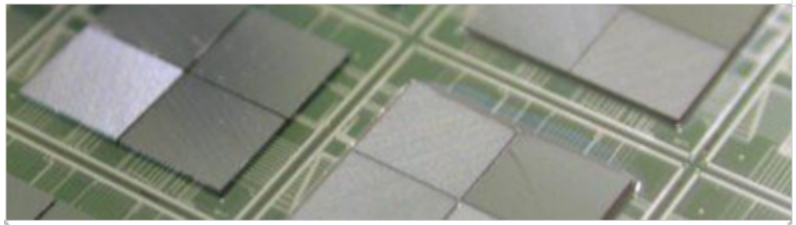
	SIP with generic DRAM	eDRAM SoC
Bus width	NG (~32bit)	OK
Capacity	OK(16M~1G)	NG(~64M)
Power	NG	OK
TTM / TTV	OK	NG
Cost (NRE)	OK	NG
ASIC pin-count	NG (Bonding limit)	OK





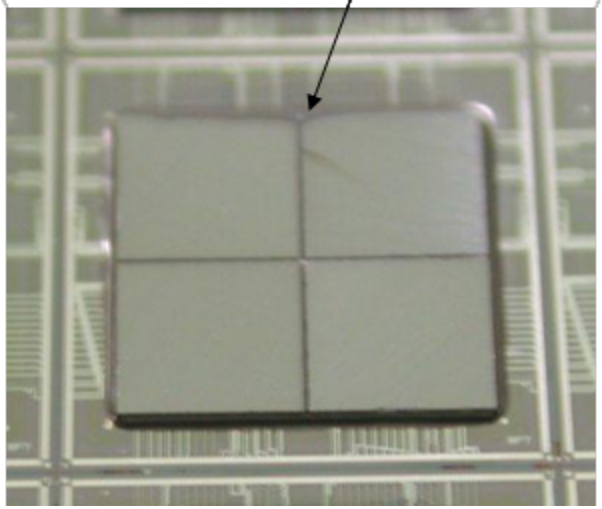
System in Silicon technology

SiS with SiIP wafer

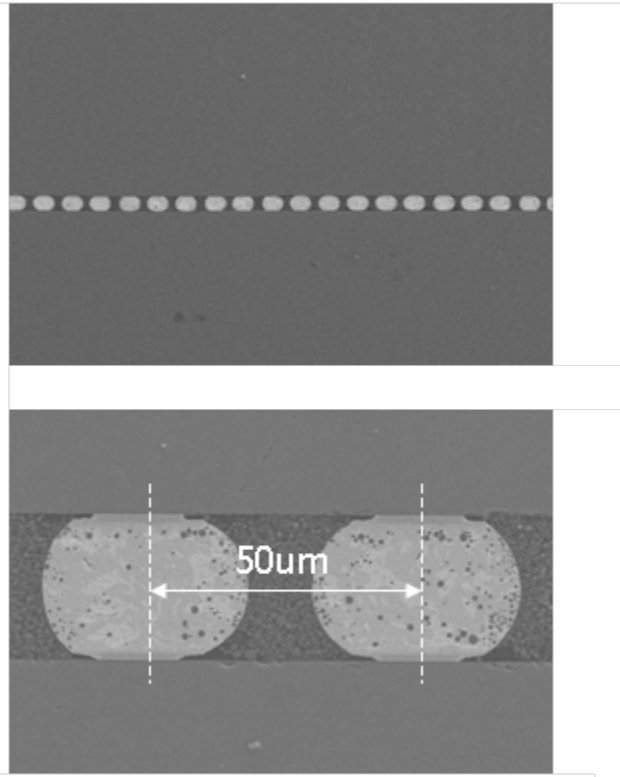


(Bump: 40um / 50um pitch)

Under Fill



a partial cross section for 50um pitch

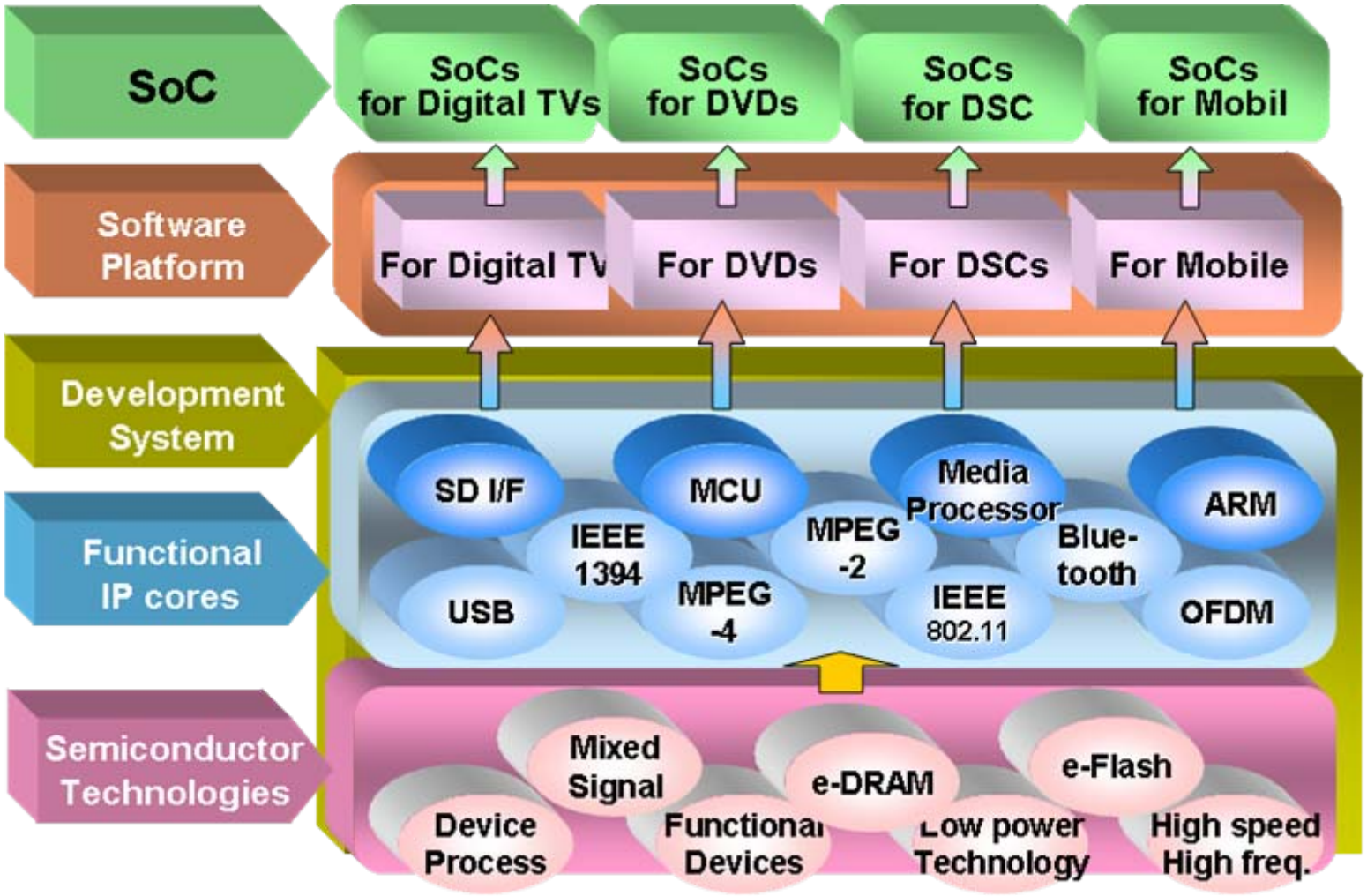


Pictures are provided by

Development management

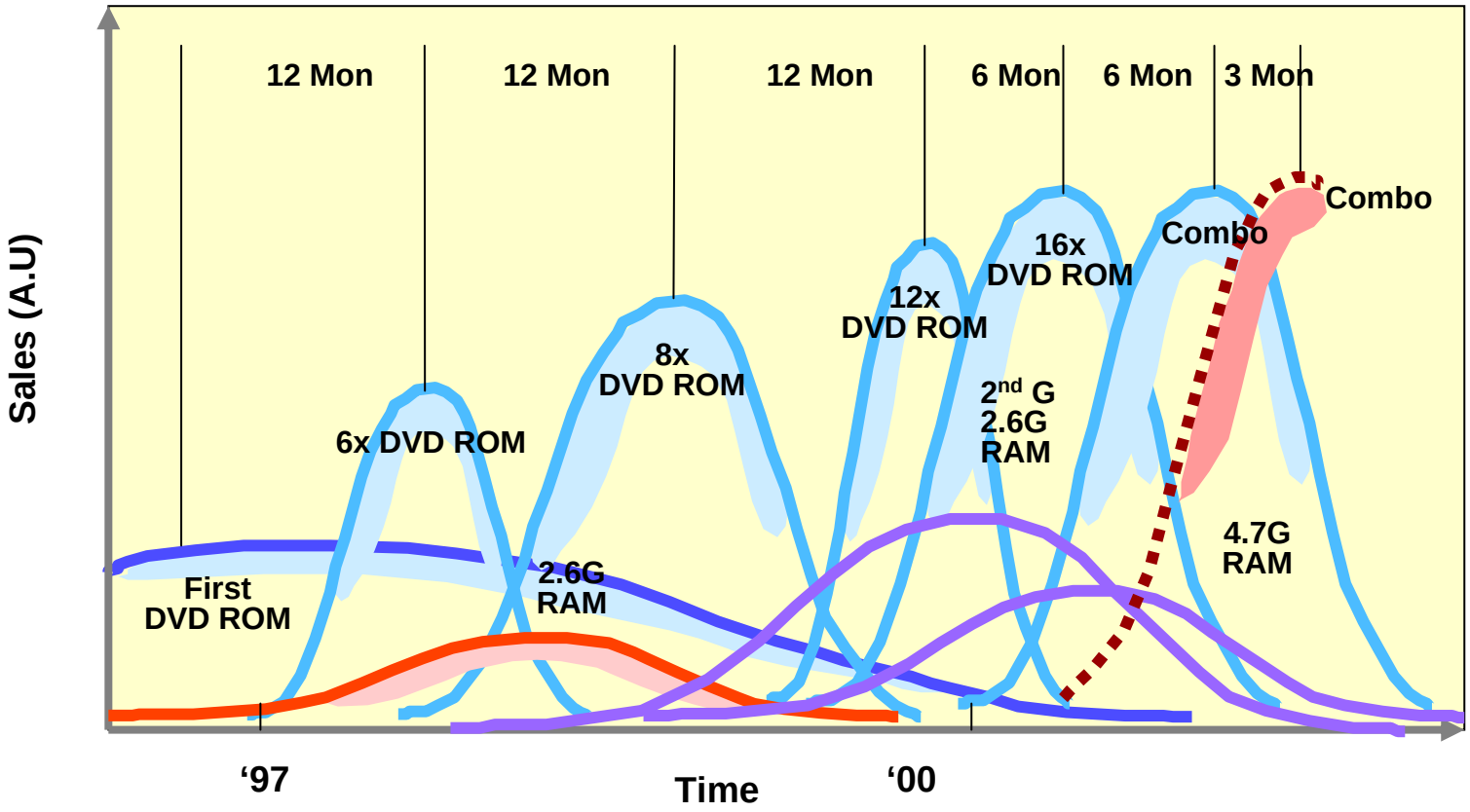
Technology platform of SoC for digital CE

SoC for digital CE needs a technological platform from device/circuits to software.



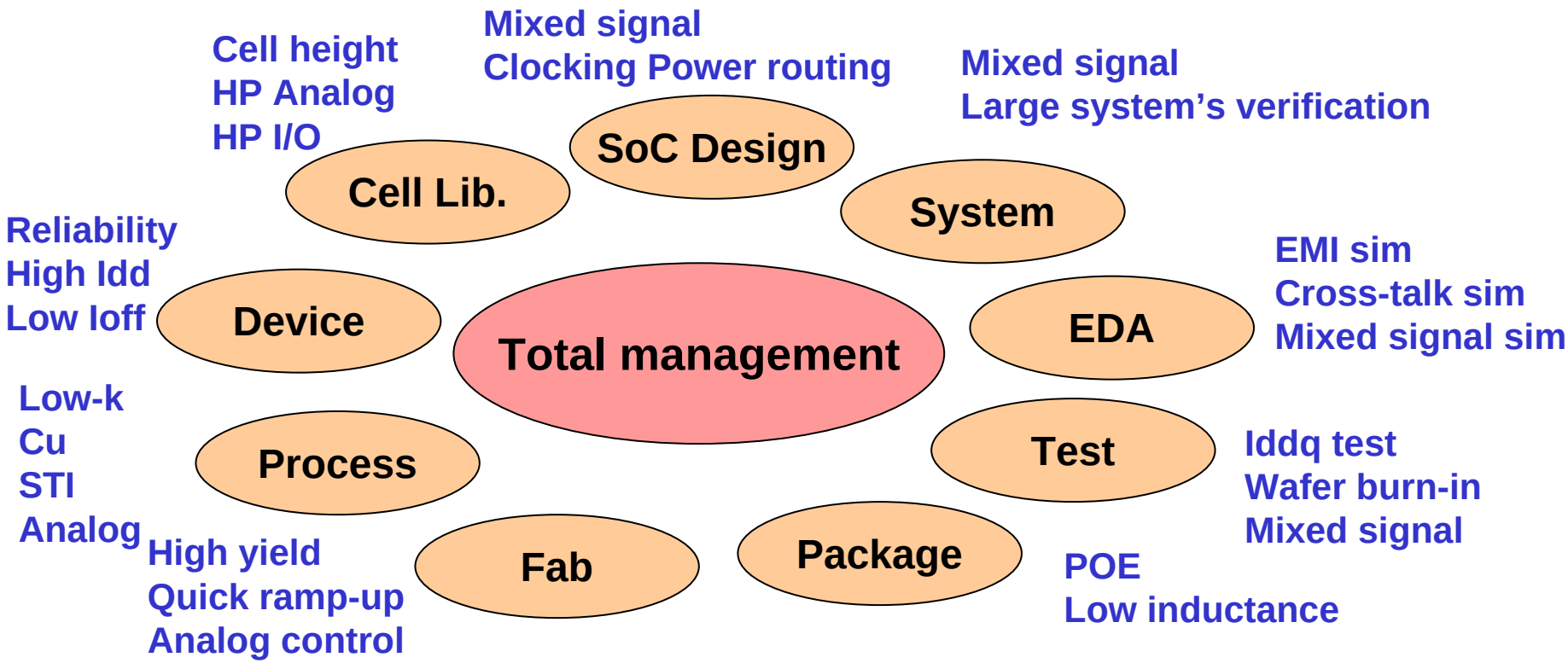
Reduction of development TAT

Unfortunately, production cycle time of digital CE becomes shorter.
Short development TAT and tangible development are vital.



Total management for SoC development

The SoC development needs a total management system for the optimization over several technology areas. DFM becomes crucial.
Making the roadmap must be effective to find future demands, issues, and solutions



Roadmap: Future demands, issues, and solutions

Summary

- **The digital consumer systems need the high throughput and low power processing capability and mixed signal interfaces, however the cost should be suppressed.**
- **The progress of LSI technology has realized it as System on a Chip (SoC). The use of application oriented architecture has attained the targets.**
- **However, the next generation SoC for the digital CE should use the software conscious unified architecture to address the issue of the software development limitation and the multimedia convergence.**
- **The SiP is essentially needed for not only the realization of high density systems but also the realization of high cost-performance systems.**
- **Furthermore, SiP (SiS) has a great potential to solve the essential memory bottleneck which limits the processing throughput and to solve the noise and power issues.**
- **Developing technology platform and total management systems for SoC development are vital for the business success.**