

# **Driving the SoC development for digital consumer electronics**

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# Contents

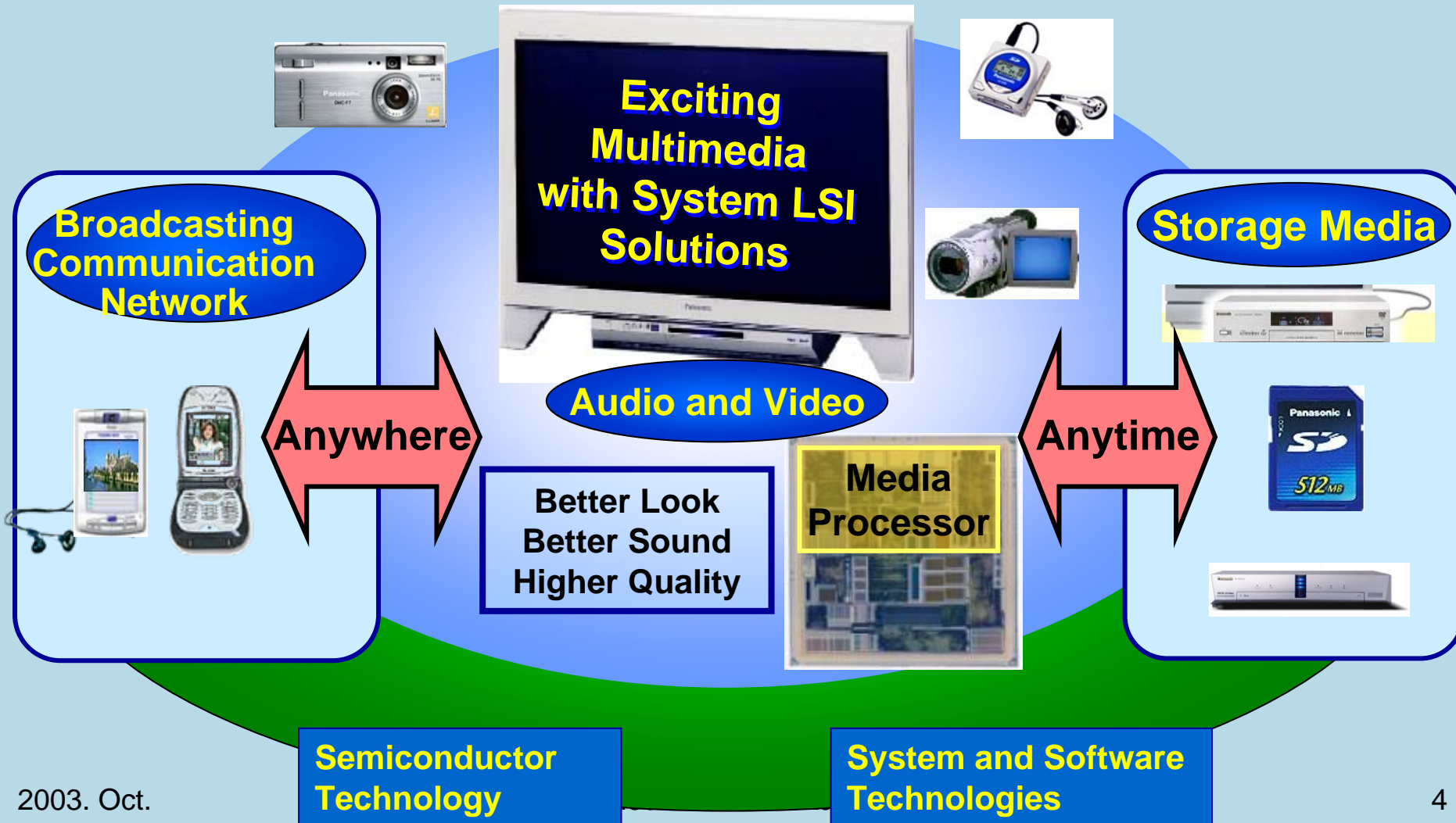
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- **Digital consumer electronics and SoC**
- **Architecture design**
- **Mixed signal technology**
- **Global development management**

# Digital consumer electronics and SoC

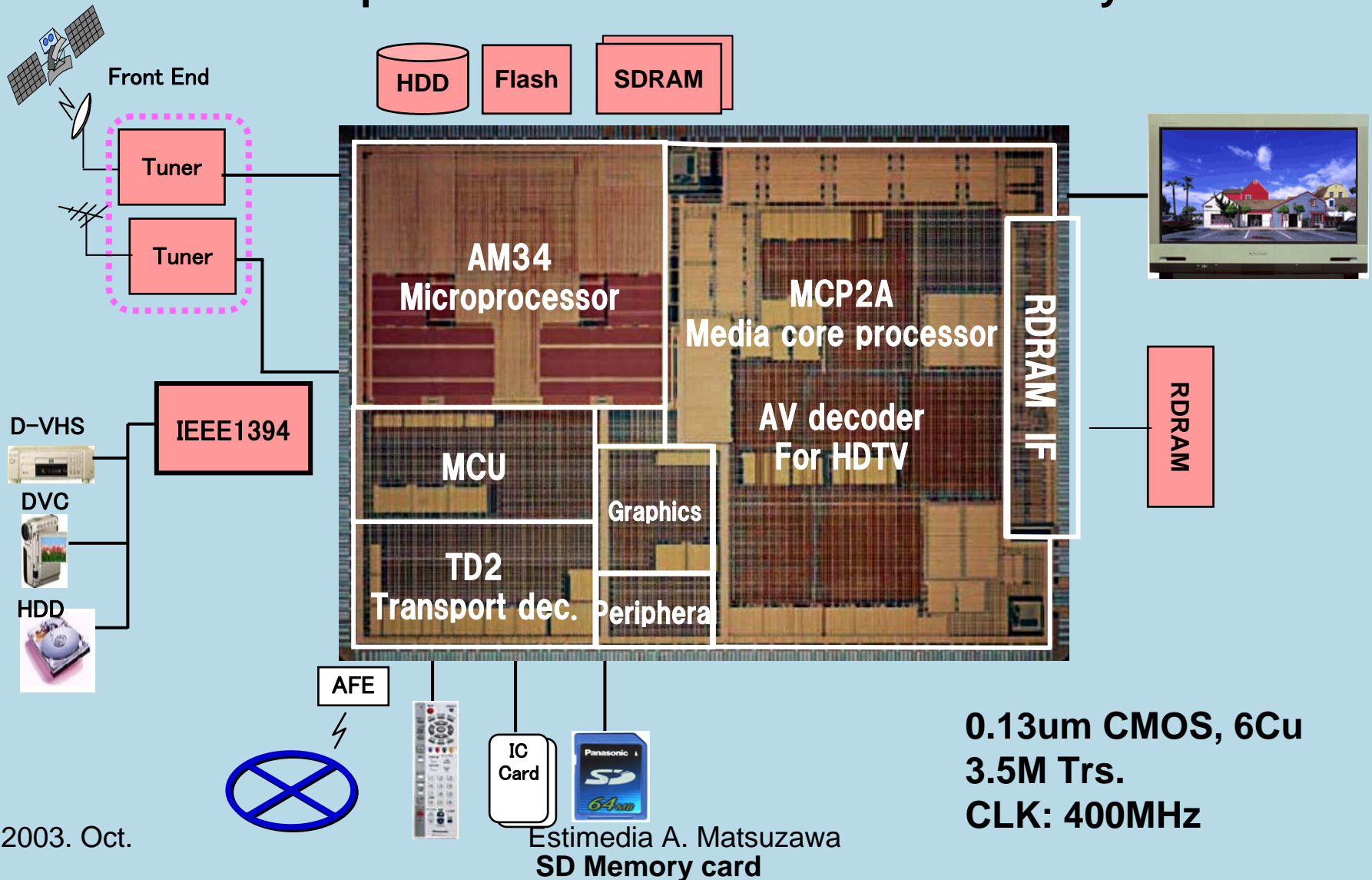
# Exciting Multimedia world with SoC!

The new consumer electronics era has been emerged.  
The key technologies are digital multimedia and System on a Chip.



# System configuration of Digital high-definition TV

One chip SoC realizes almost whole electric systems

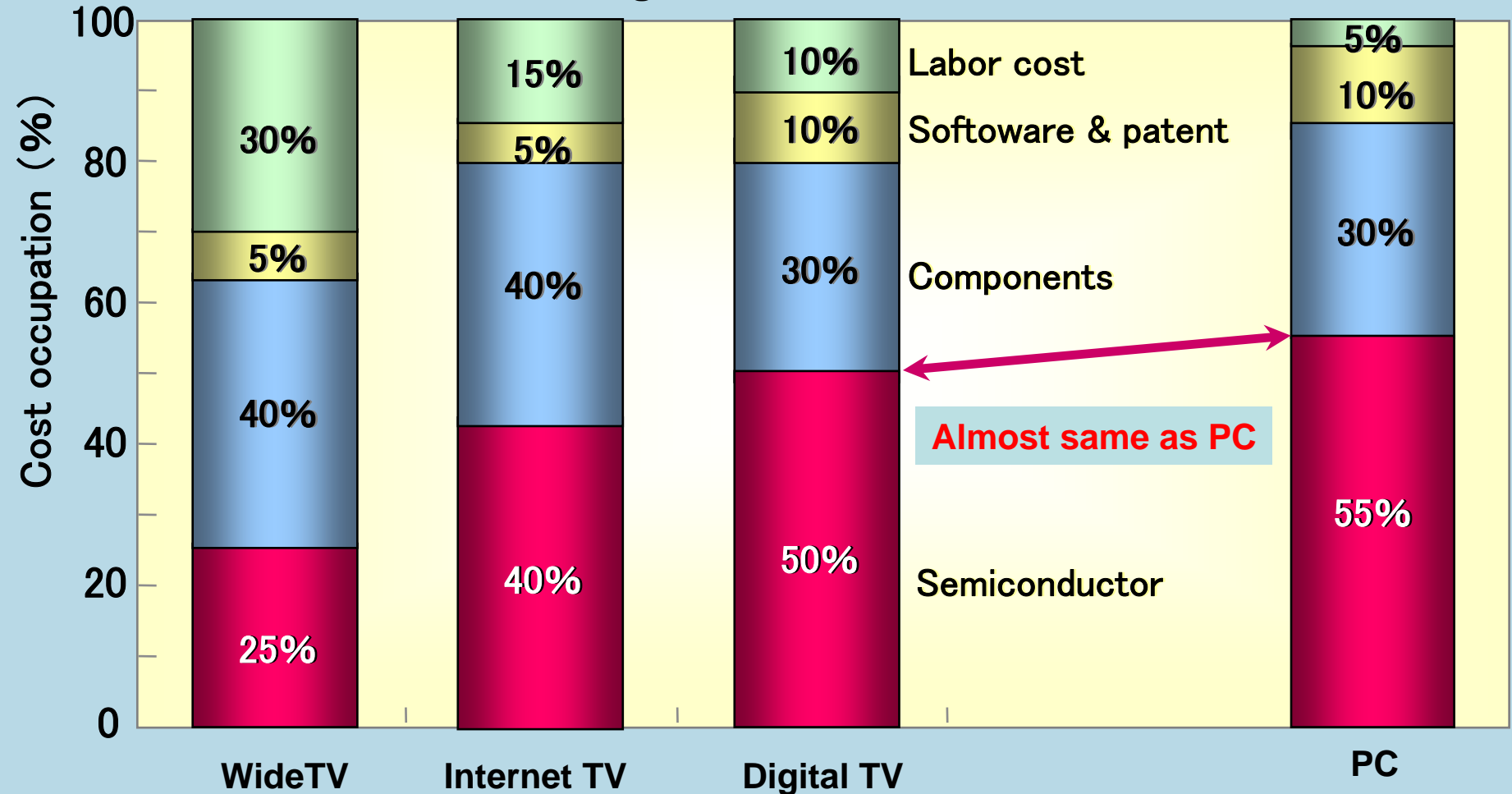


# Impact of digital tech. on consumer business

LSI = System !, technically and in business

Analog base

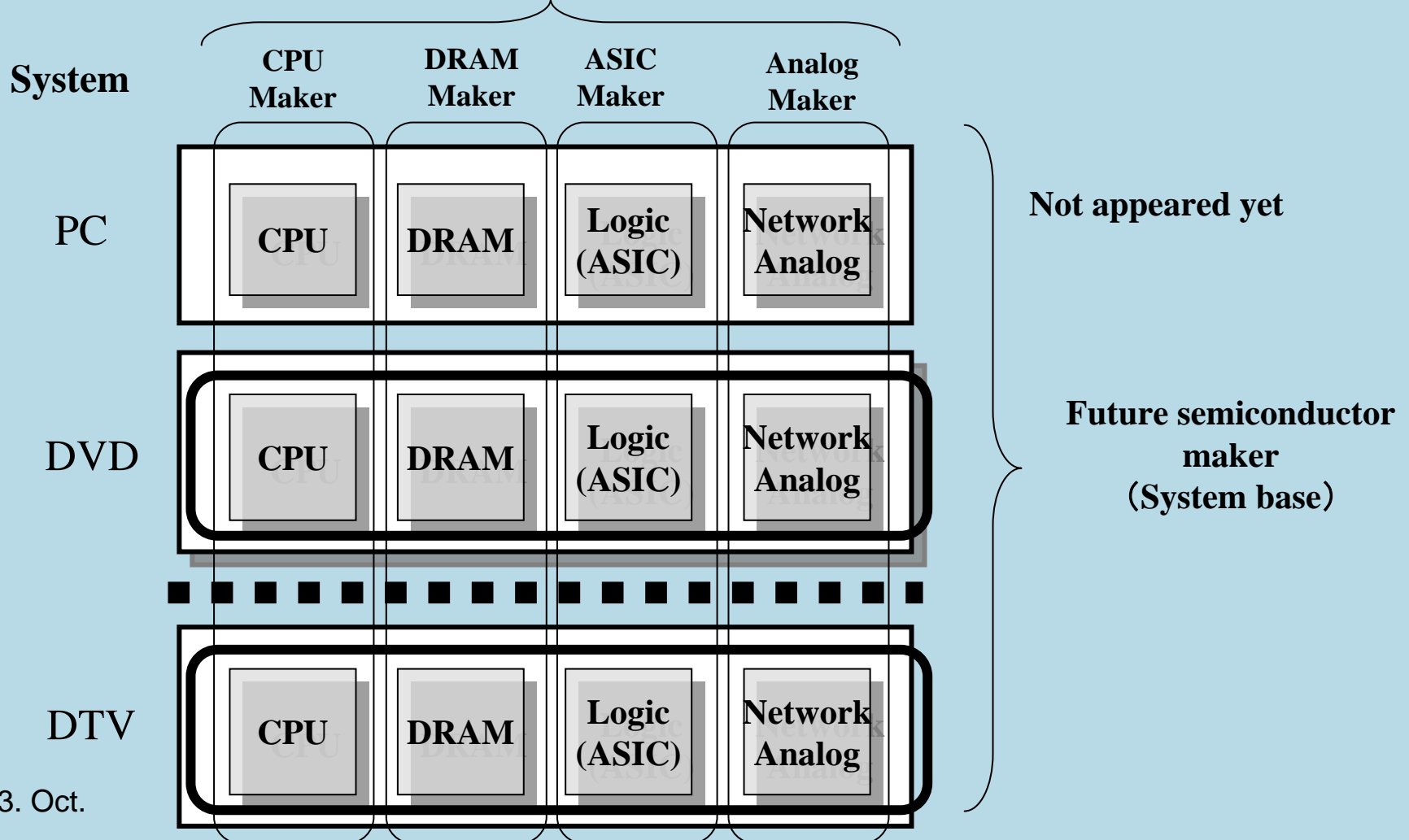
Digital base



# New semiconductor business scheme

SoC will reform the semiconductor business scheme from vertical to horizontal.

Conventional semiconductor maker (semiconductor technology base)

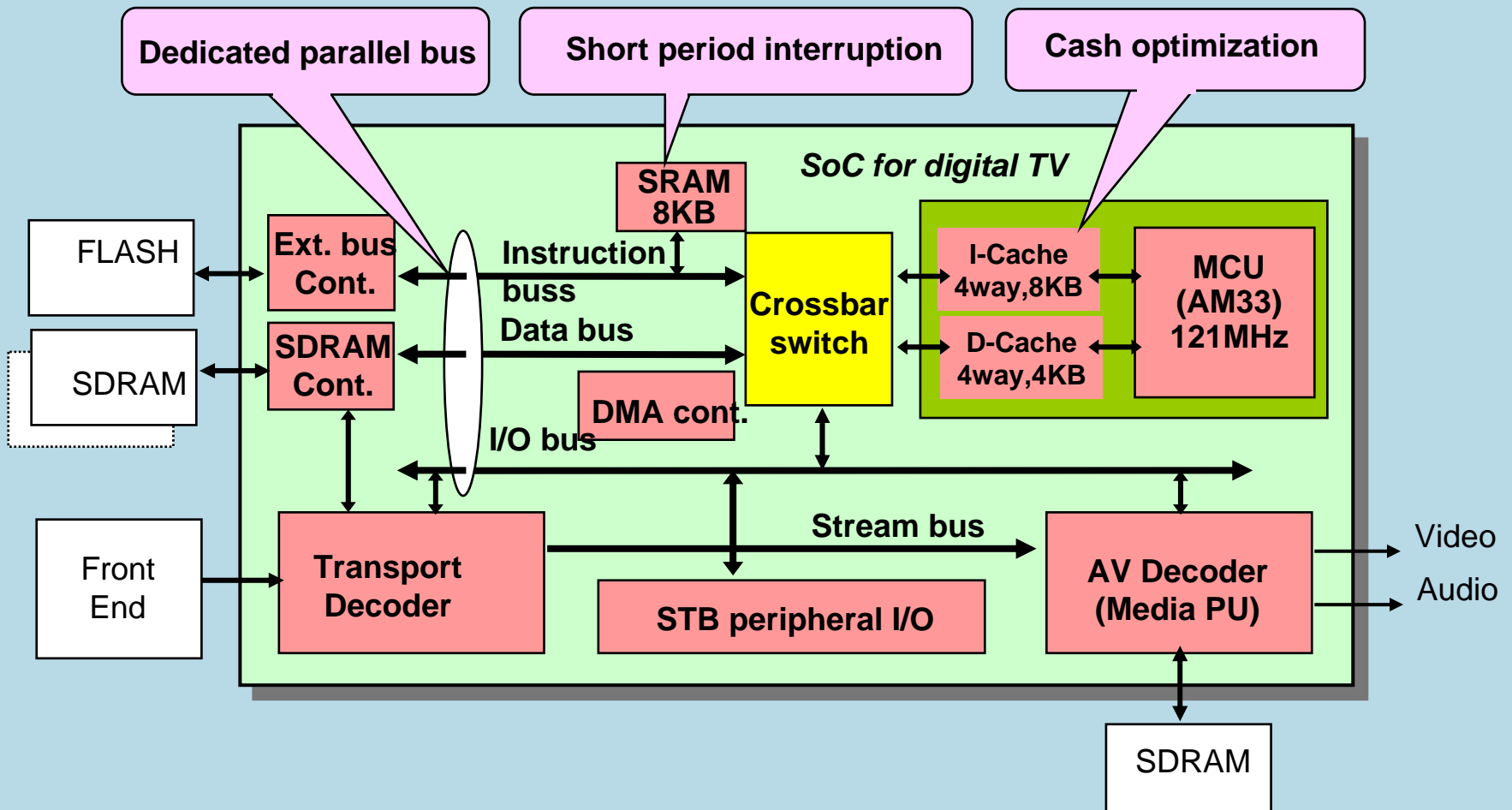


# Architecture design



# Architecture design

The architecture optimization based on a system analysis is a key.

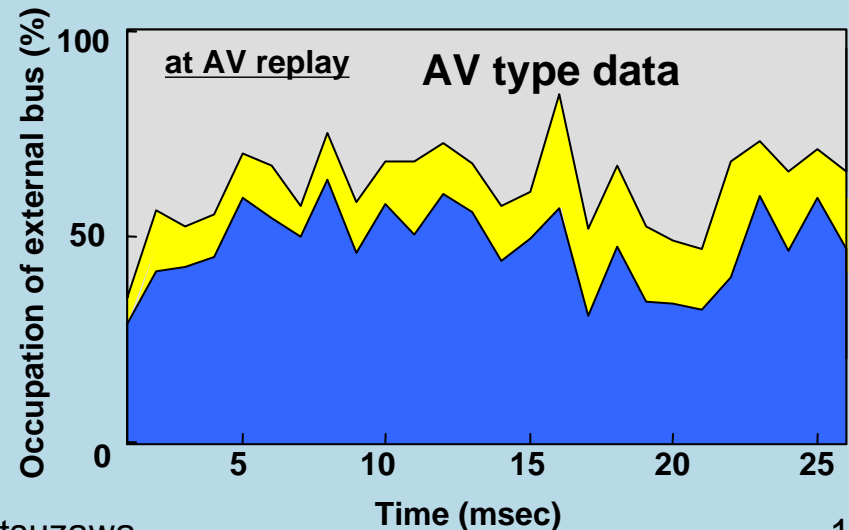
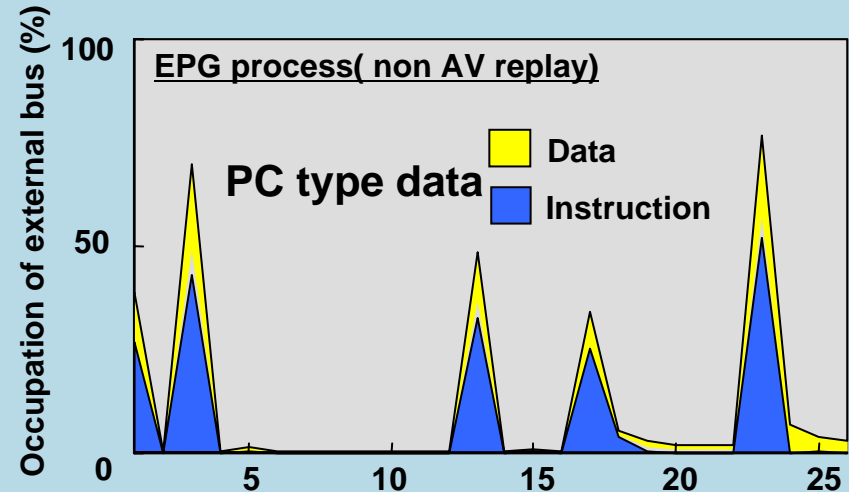
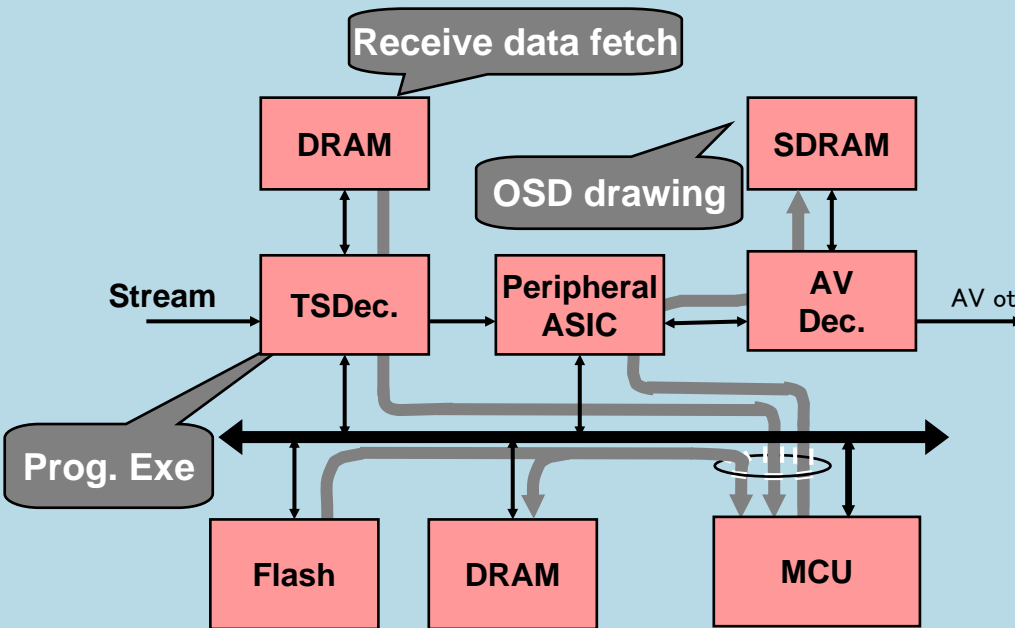


# System analysis 1: External bus

Bus occupation increases at AV replay

Conventional PC bus can't be used

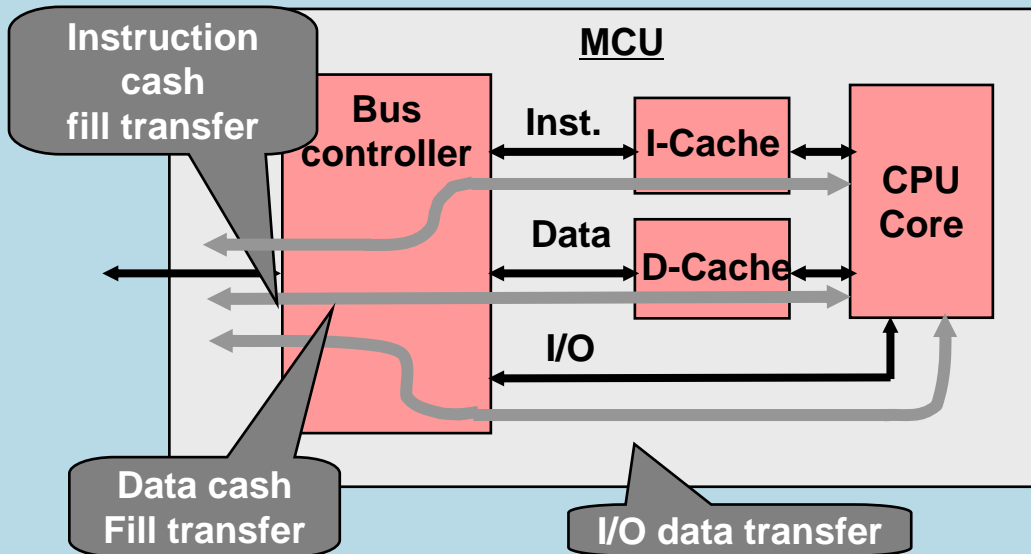
New bus architecture is needed



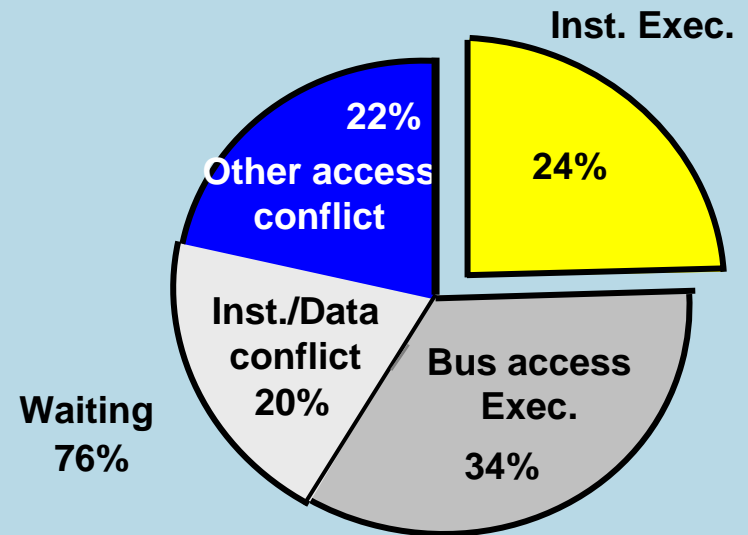
# System analysis 2: Internal bus

Instruction execution is only 1/4

Many conflicts between data and instructions



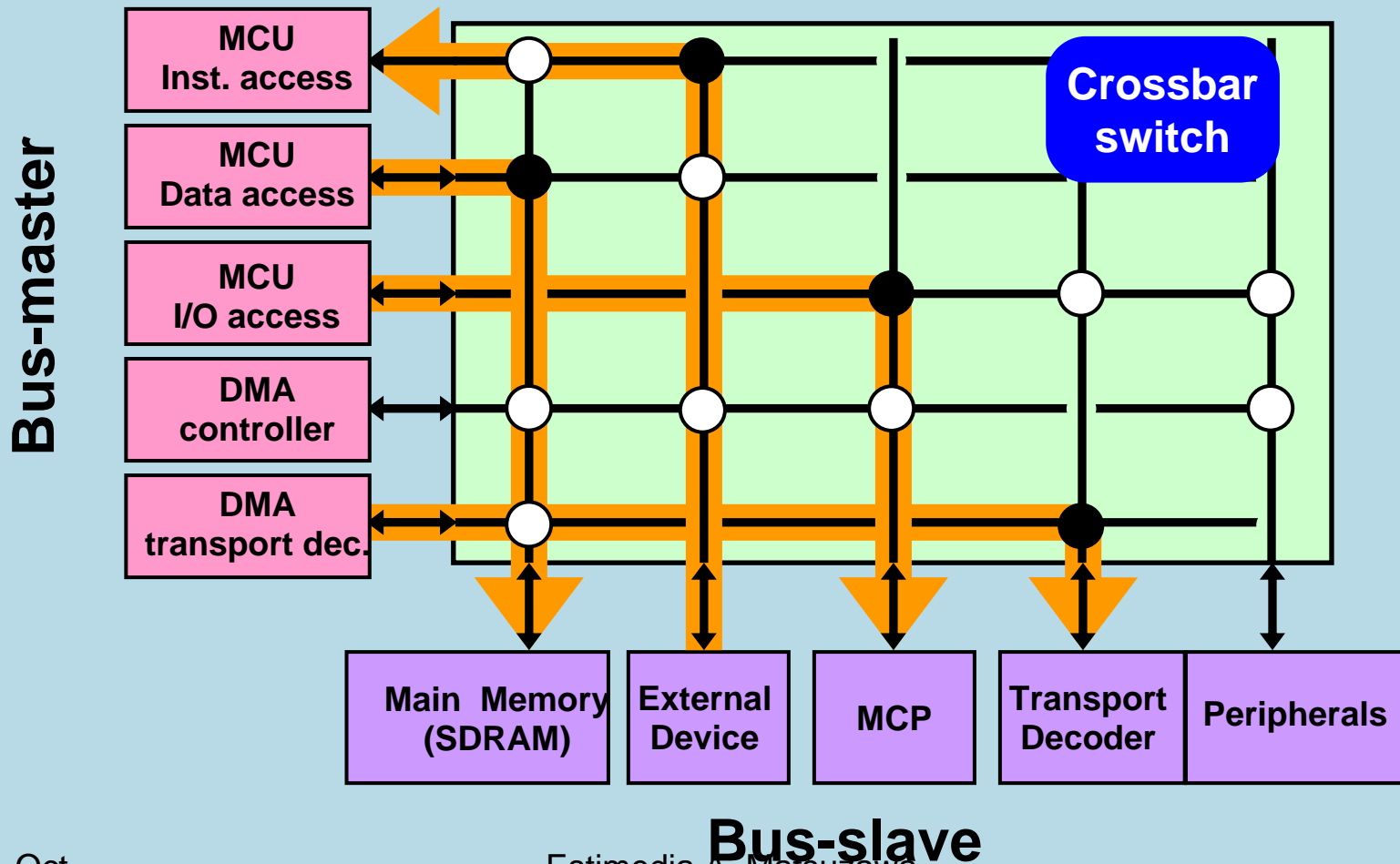
Access conflicts



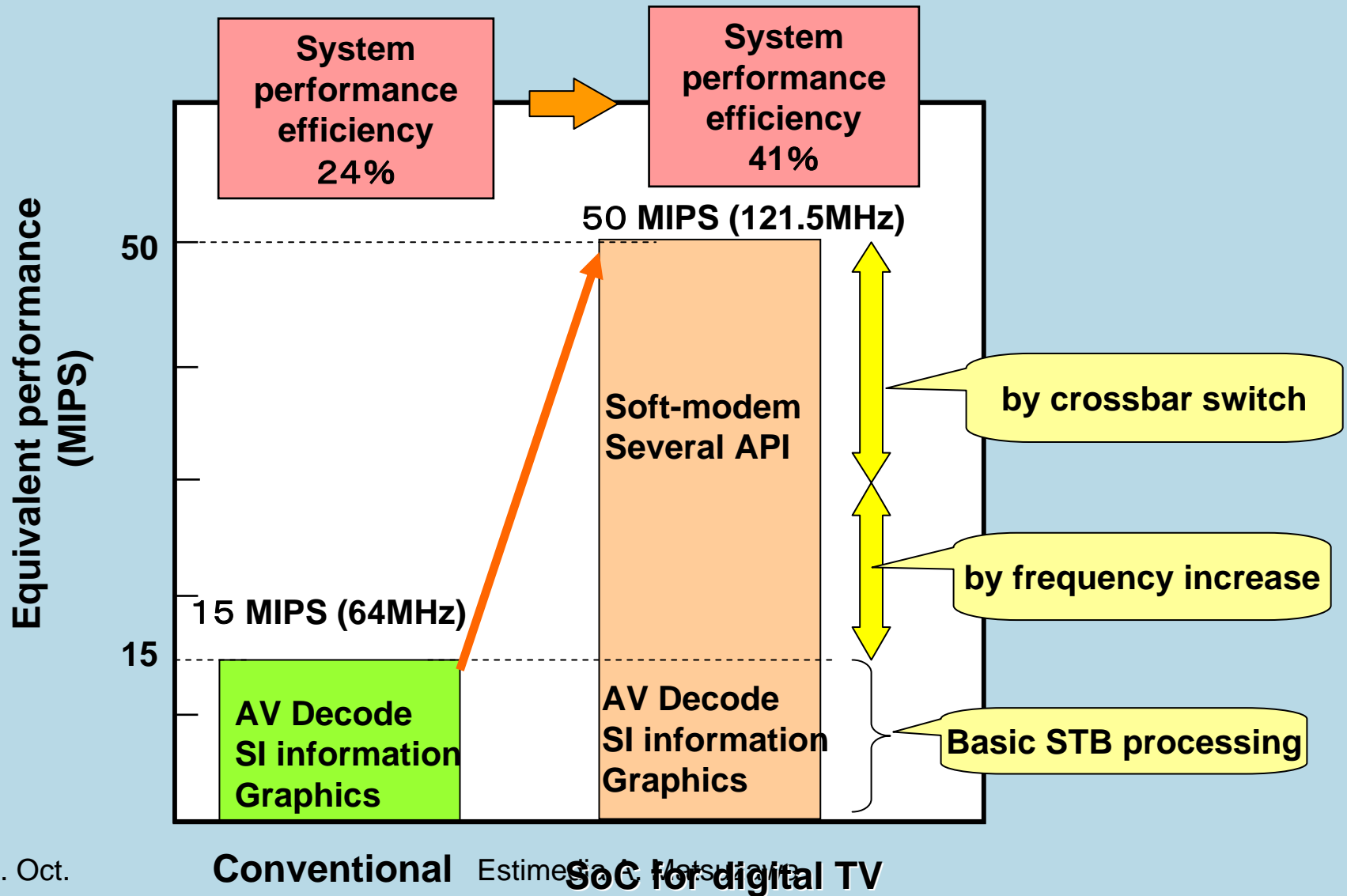
Internal status in MCU

# Solution: Crossbar switch

Bus-master can access to bus slave in each, independently

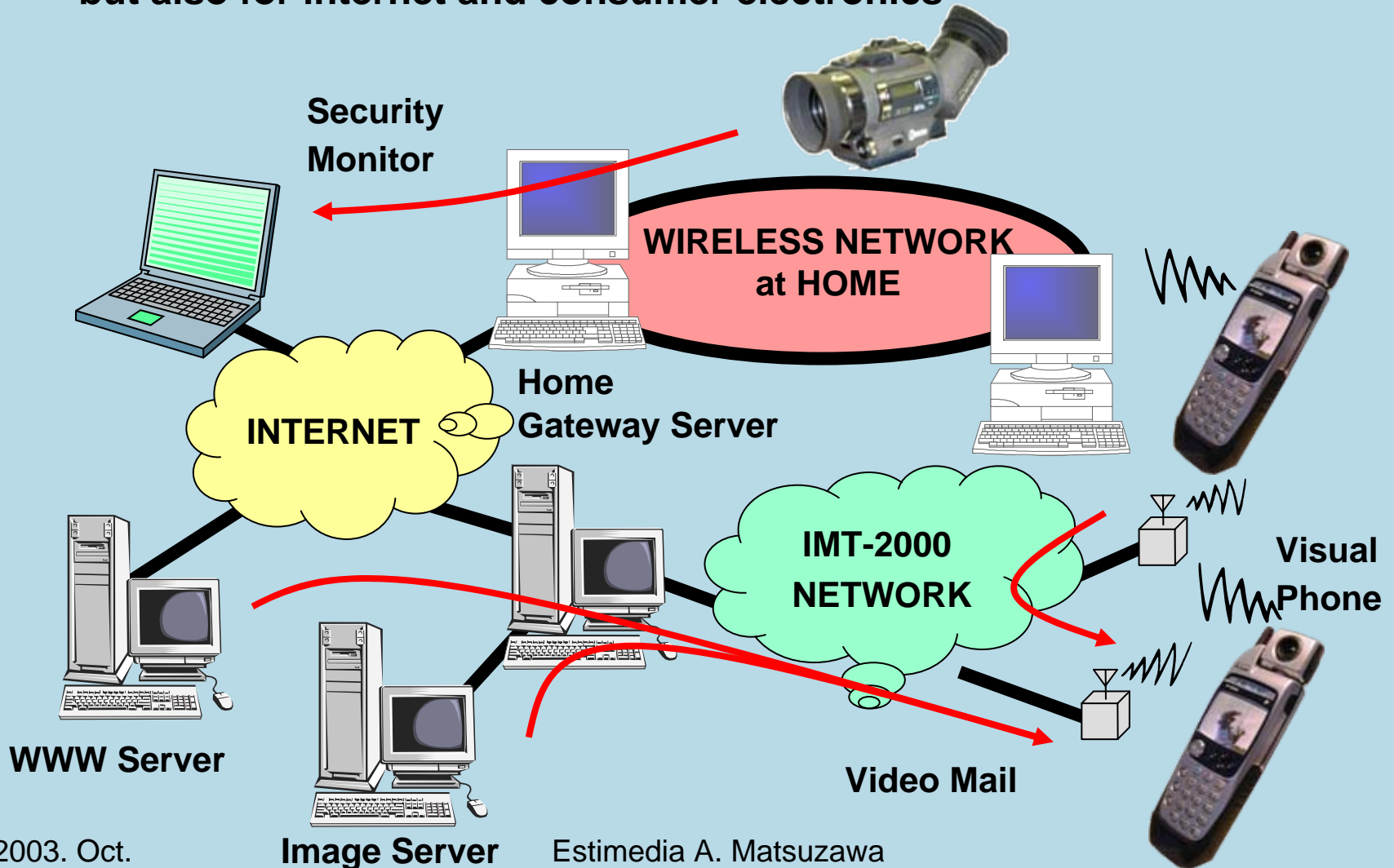


# Performance improvement



# MPEG4 World

The MPEG4 technology are going to be used not only for a cellular phone, but also for internet and consumer electronics

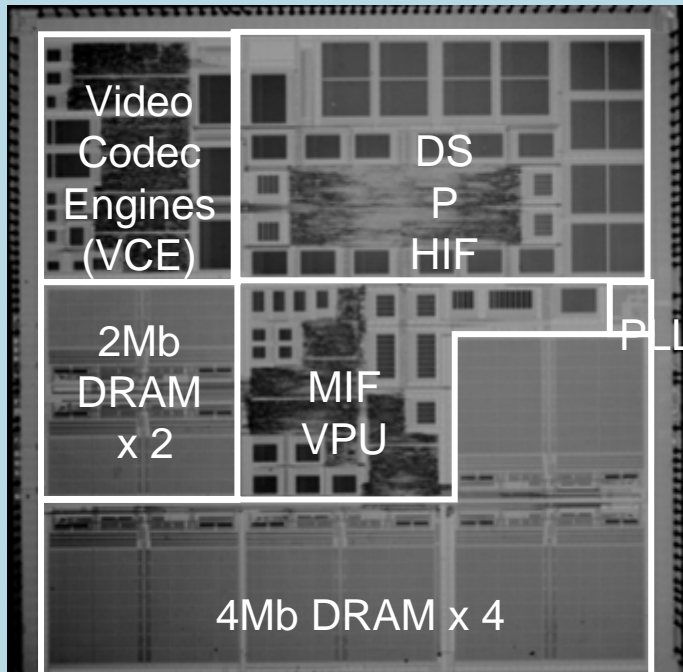


# MPEG4 Codec and decoder

## MPEG4 Codec

0.18um e-DRAM  
31M Tr  
90 mW@54MHz

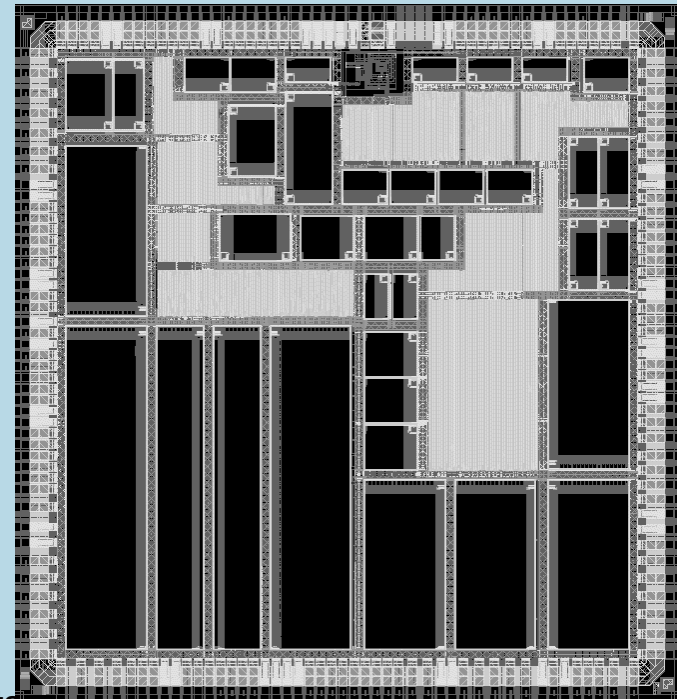
15fps (Core@L1 decode)  
30 fps (Simple@L3 decode)



## MPEG4 Decoder

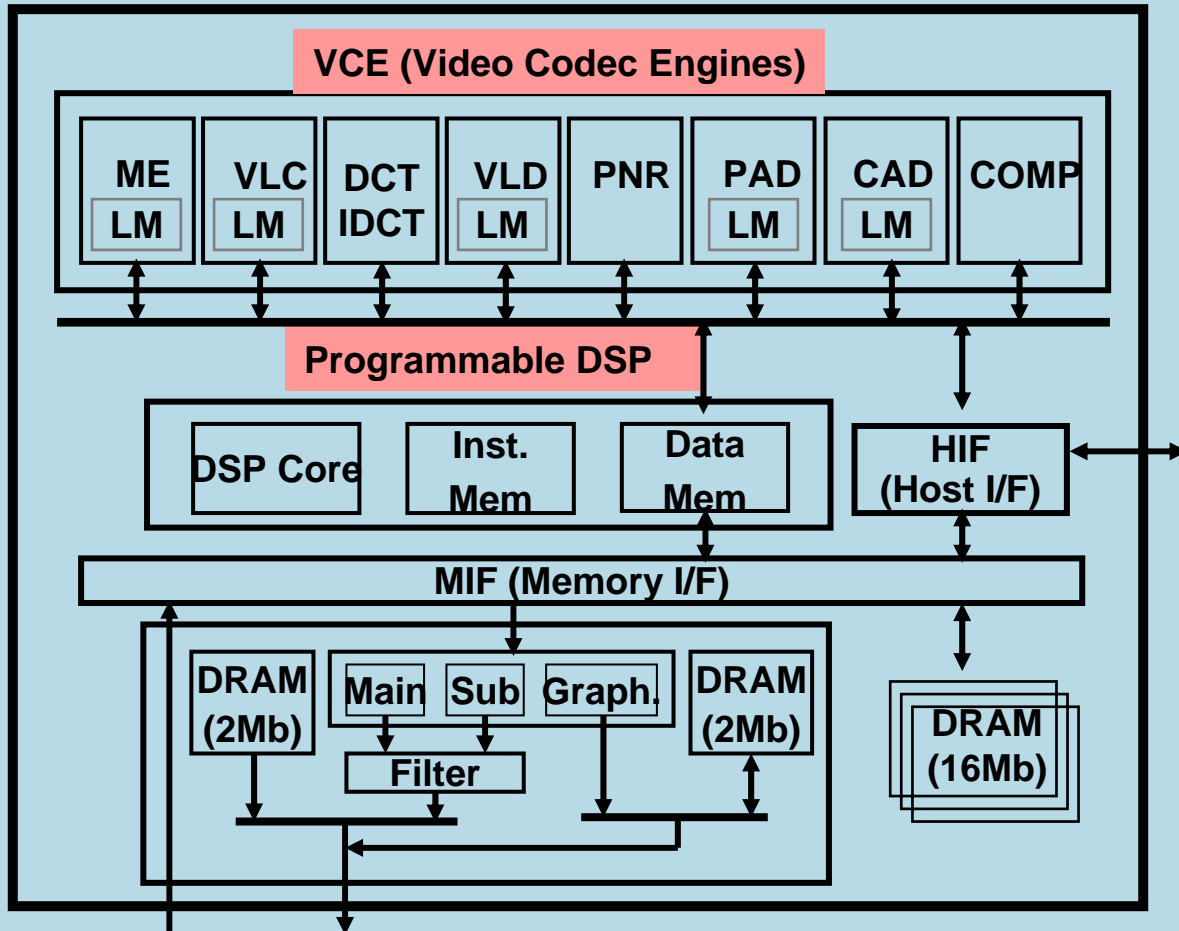
0.18um CMOS  
11M Tr  
11 mW@27/54MHz

15fps (Core@L1 decode)



# MPEG4 Codec

DSP with Vector Pipeline and dedicated HW engines enables high throughput and low power video processing

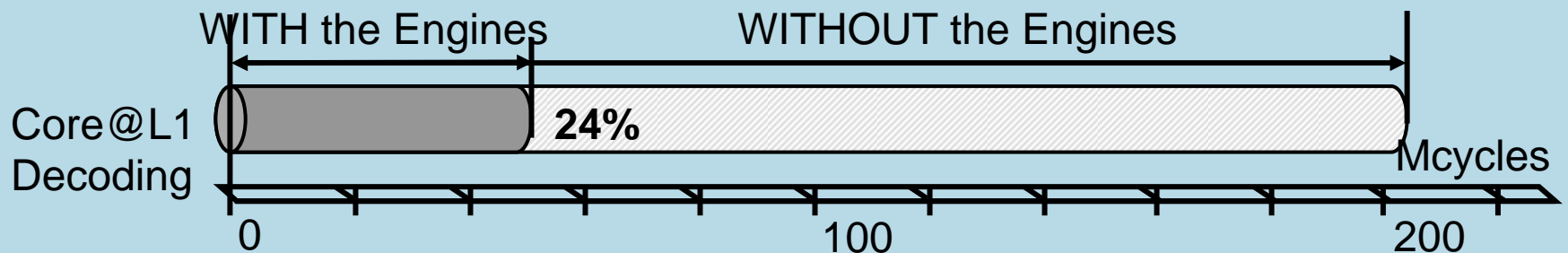
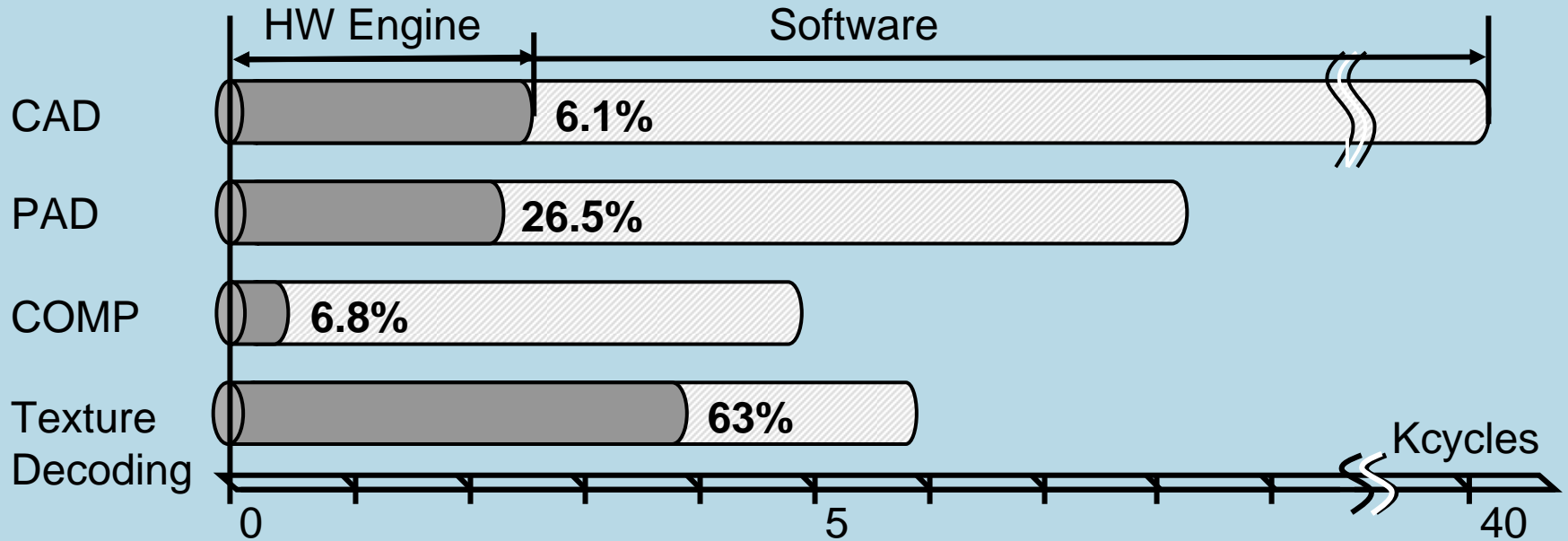


1.5 GOPS: Simple@L1  
12 GOPS: Simple@L3  
6 GOPS: Core@L1



# Performance of core decoding

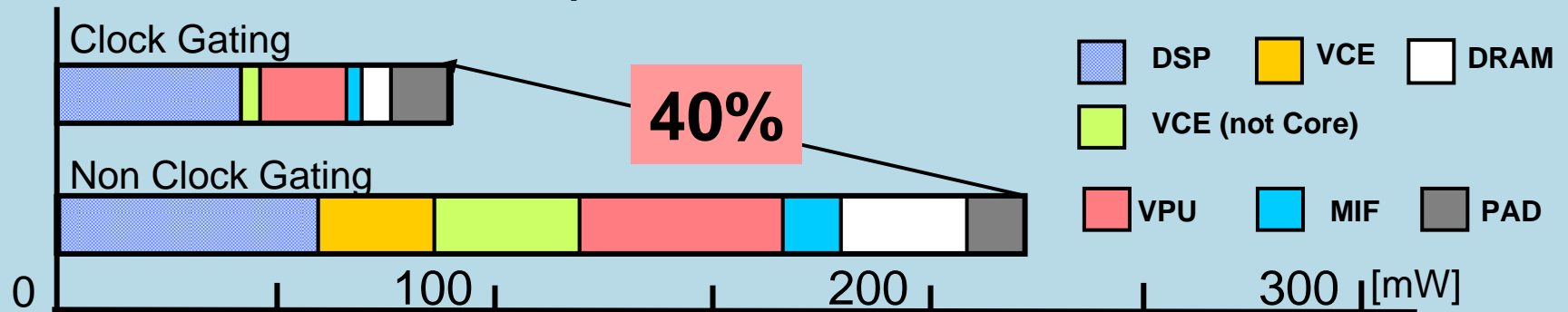
Hardware engines increase the performance 4 times higher



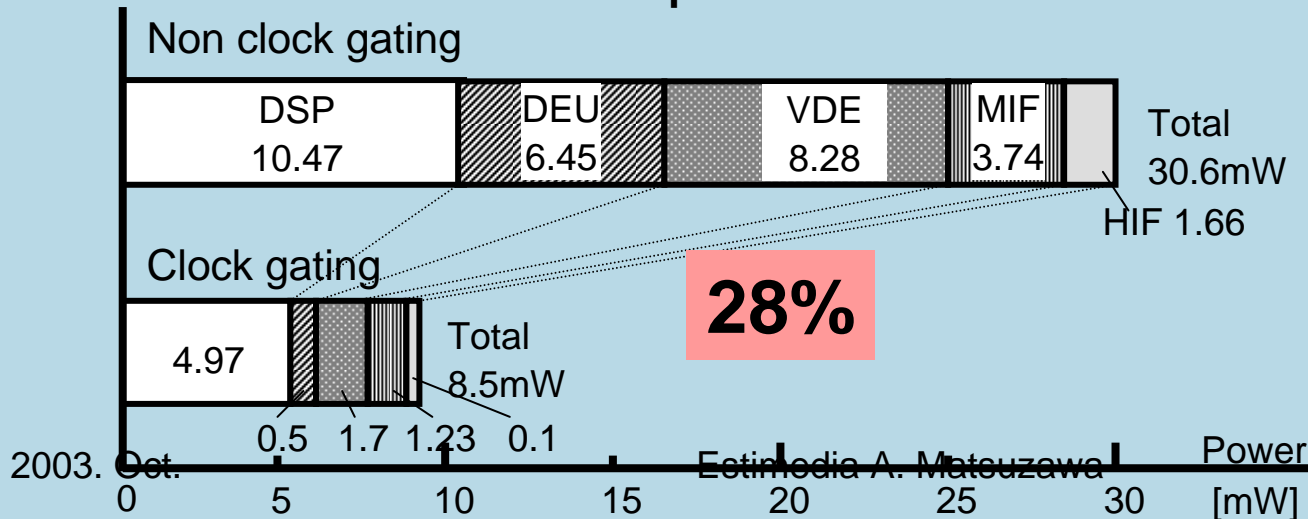
# Clock gating

The sophisticated clock gating is very effective to reduce the power consumption.

### Example 1: MPEG4 Codec



### Example 2: MPEG4 Decoder



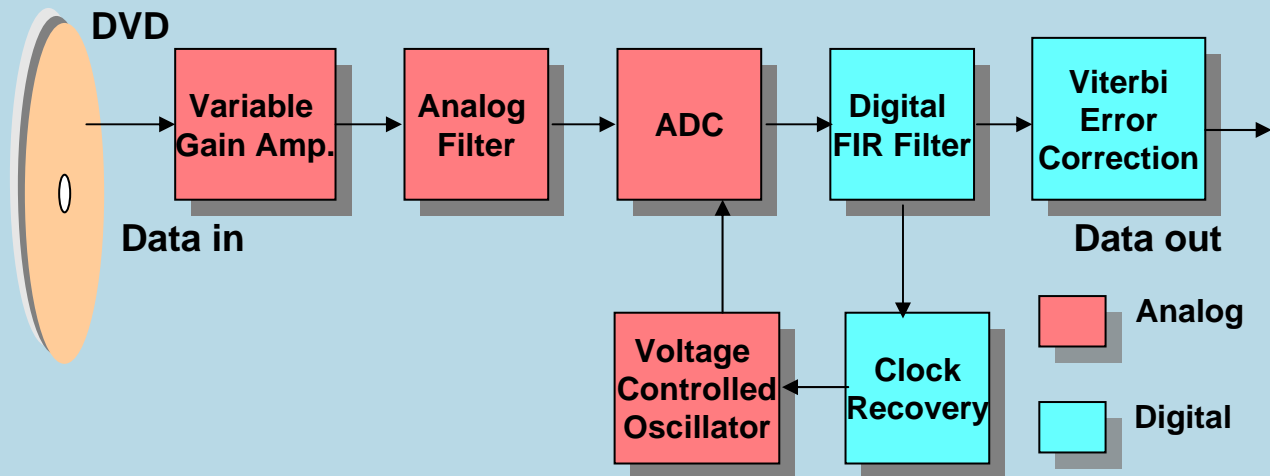
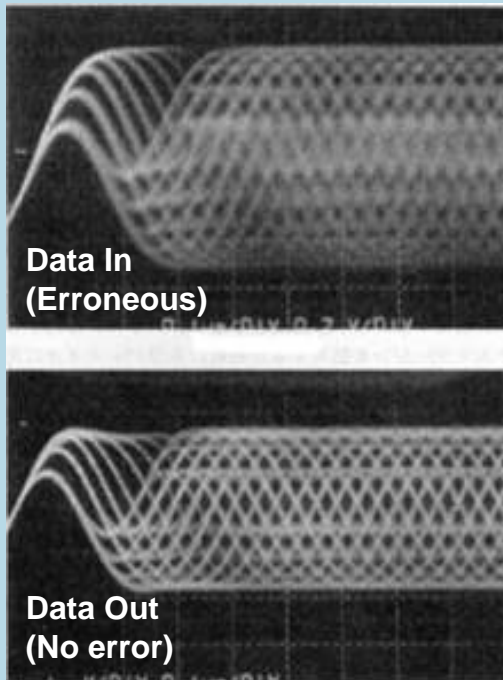
# Mixed signal technology

# Mixed signal technology

The mixed signal is vital to current SoC for the consumer and networking.

However, conventional analog needs 2 or 3 redesigns!

**How to develop it without re-design!**

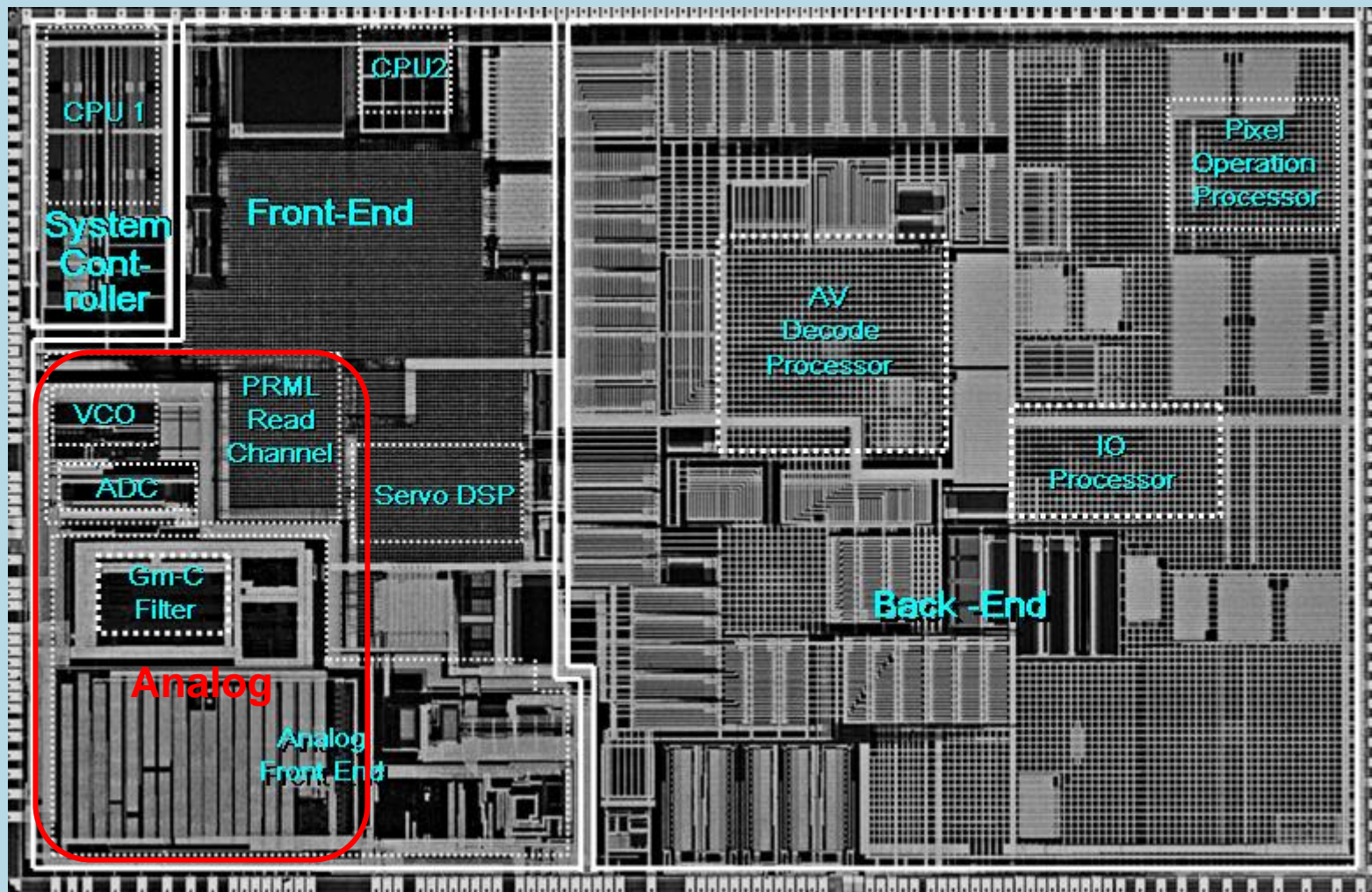


Mixed signal can decrease bit-error rate and can increase stability in DVD recorder systems.

# Mixed signal SoC for DVD systems

The SoC integrates analog FE, front-end, and back-end in 0.13um tech.

ISSCC 2003, K Okamoto et., al. 24M Tr



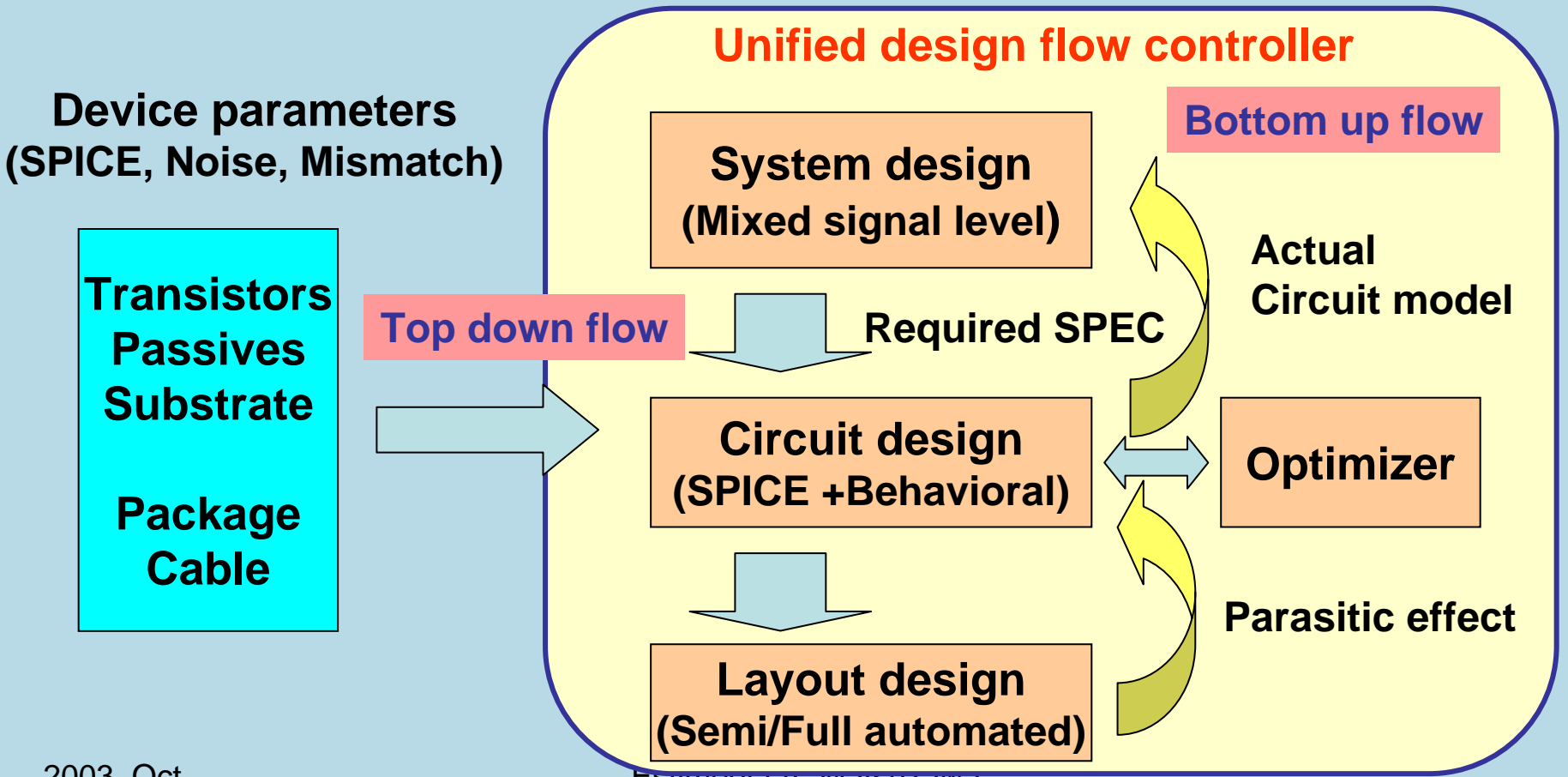
# Strategy for the mixed signal SoC

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- **System design**
  - **Digital calibration** for analog adjustment and unknown parameters.
  - **System optimization** to reduce analog area and increase robustness.
- **System verification**
  - Fast and accurate **mixed signal system simulator** with behavioral model to verify and optimize the mixed signal system.
  - Create the **target performance** for circuit blocks.
- **Circuit design**
  - Ultra fast and accurate circuit simulation for **P.V.T and fluctuation analysis** to verify the performance and robustness.
  - **Circuit optimizer** to find the sweet spot of the circuit.
  - Automated **creation of analog behavioral model** for system simulation.
- **Process and device development**
  - Develop suitable **analog option device**
  - Early **analog parameter extraction** ( mismatch, temp. and voltage chara.)
  - **Monitor and control the analog parameters** in Fab.

# Design flow for mixed signal SoC

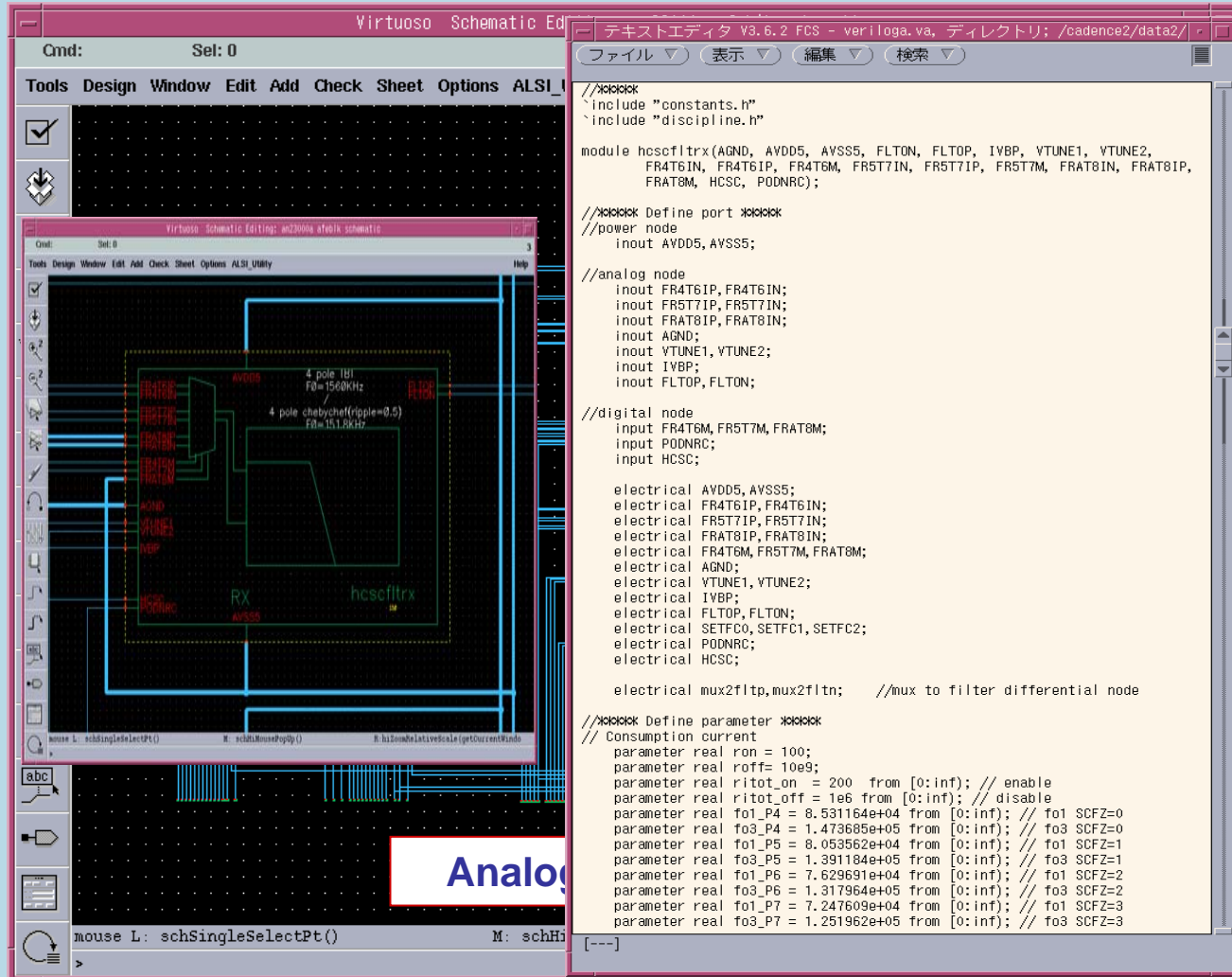
The design flow from a system to a layout with top down and bottom up process should be used for designing the mixed signal SoC.  
The accurate and a variety of device parameters is an another key.





# Hierarchical and behavioral system design

This system should be described in behavioral language, hierarchically.



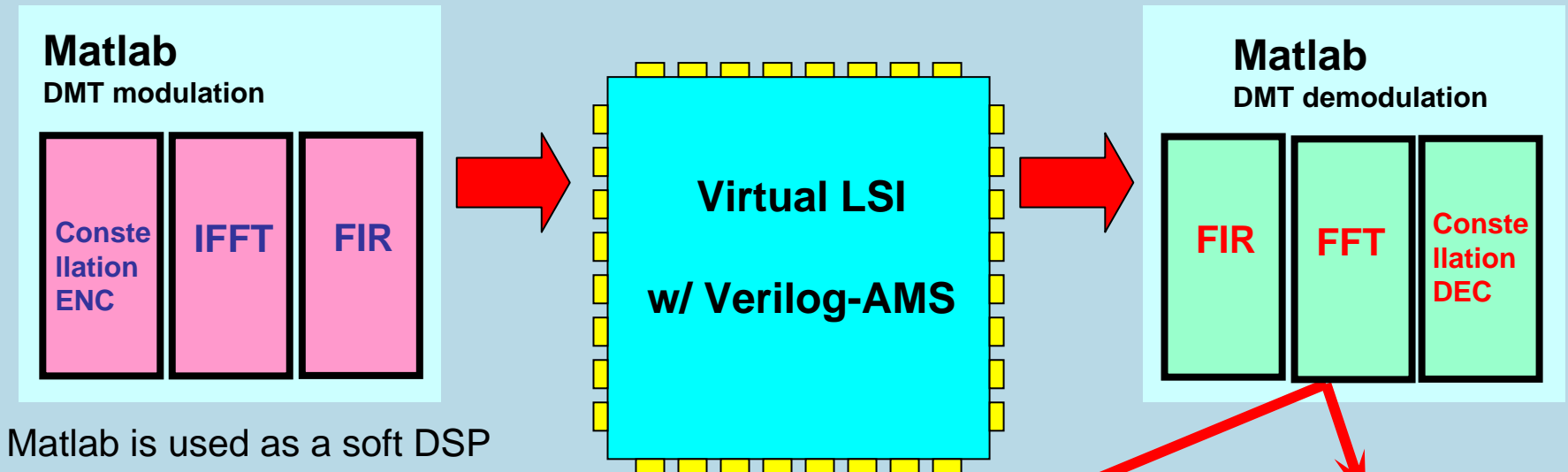
The image displays two windows from the Virtuoso Schematic Editor. The left window shows a hierarchical schematic diagram of a filter system. It features a central block labeled 'hscsfltr' which is connected to various input and output nodes. The schematic includes components like '4 pole IIR' and '4 pole chebycheff(ripple=0.5)'. The right window shows the Verilog code for the 'hscsfltr' module, which is a behavioral description of the filter. The code includes port declarations, electrical node definitions, and parameter settings for the filter's behavior.

```
//*****  
`include "constants.h"  
`include "discipline.h"  
  
module hscsfltrx(AGND, AVDD5, AVSS5, FLTON, FLTOP, IVBP, VTUNE1, VTUNE2,  
FR4T6IN, FR4T6IP, FR4T6M, FR5T7IN, FR5T7IP, FR5T7M, FRAT8IN, FRAT8IP,  
FRAT8M, HCSC, PODNRC);  
  
//***** Define port *****  
//power node  
inout AVDD5, AVSS5;  
  
//analog node  
inout FR4T6IP, FR4T6IN;  
inout FR5T7IP, FR5T7IN;  
inout FRAT8IP, FRAT8IN;  
inout AGND;  
inout VTUNE1, VTUNE2;  
inout IVBP;  
inout FLTOP, FLTON;  
  
//digital node  
input FR4T6M, FR5T7M, FRAT8M;  
input PODNRC;  
input HCSC;  
  
electrical AVDD5, AVSS5;  
electrical FR4T6IP, FR4T6IN;  
electrical FR5T7IP, FR5T7IN;  
electrical FRAT8IP, FRAT8IN;  
electrical FR4T6M, FR5T7M, FRAT8M;  
electrical AGND;  
electrical VTUNE1, VTUNE2;  
electrical IVBP;  
electrical FLTOP, FLTON;  
electrical SETFC0, SETFC1, SETFC2;  
electrical PODNRC;  
electrical HCSC;  
  
electrical mux2fltp, mux2fltn; //mux to filter differential node  
  
//***** Define parameter *****  
// Consumption current  
parameter real ron = 100;  
parameter real roff = 10e9;  
parameter real riotot_on = 200 from [0:inf]; // enable  
parameter real riotot_off = 1e6 from [0:inf]; // disable  
parameter real fo1_P4 = 8.531164e+04 from [0:inf]; // fo1 SCFZ=0  
parameter real fo3_P4 = 1.473685e+05 from [0:inf]; // fo3 SCFZ=0  
parameter real fo1_P5 = 8.053562e+04 from [0:inf]; // fo1 SCFZ=1  
parameter real fo3_P5 = 1.391184e+05 from [0:inf]; // fo3 SCFZ=1  
parameter real fo1_P6 = 7.629691e+04 from [0:inf]; // fo1 SCFZ=2  
parameter real fo3_P6 = 1.317964e+05 from [0:inf]; // fo3 SCFZ=2  
parameter real fo1_P7 = 7.247609e+04 from [0:inf]; // fo1 SCFZ=3  
parameter real fo3_P7 = 1.251962e+05 from [0:inf]; // fo3 SCFZ=3  
  
[---]
```

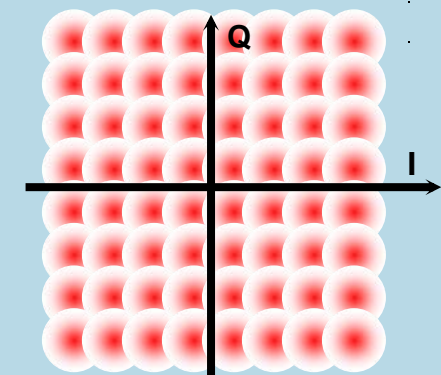
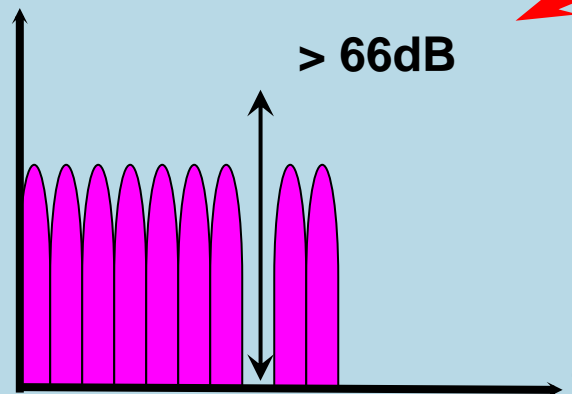
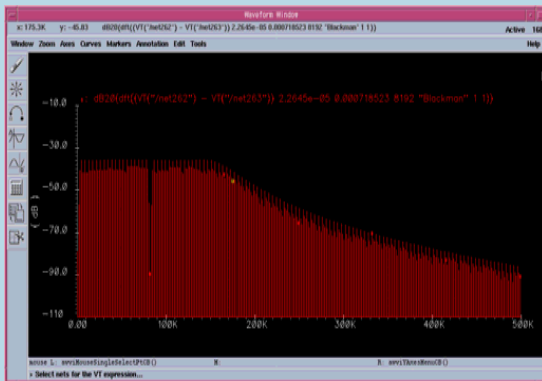


# Virtual System test using verilog AMS and Matlab

We can simulate the performance of mixed signal system, using Verilog AMS and Matlab.



Matlab is used as a soft DSP



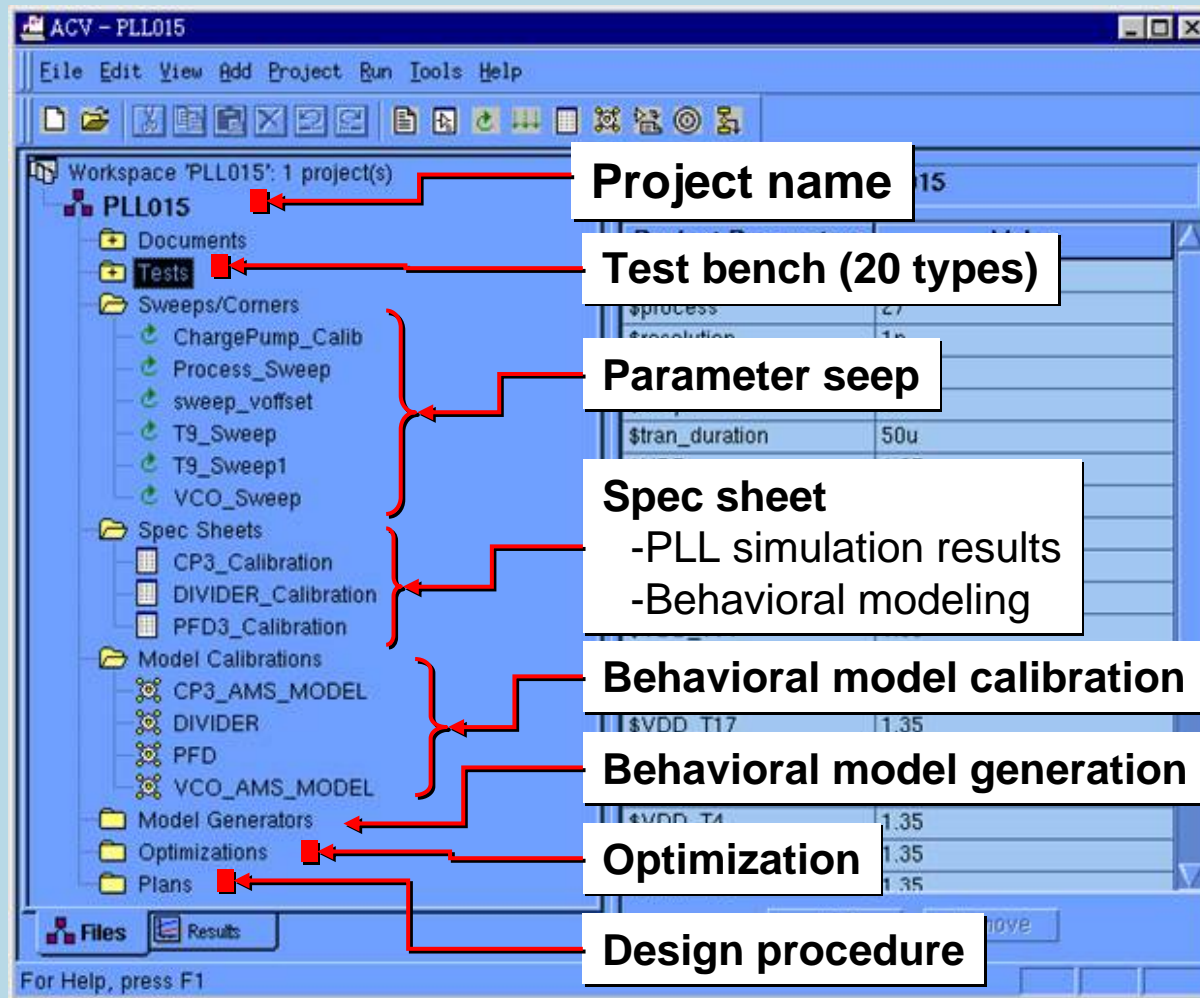
MTPR TEST (DMT Carrier hole)

Estimedia A. Matsuzawa

QAM constellation

# Controller for automated simulation

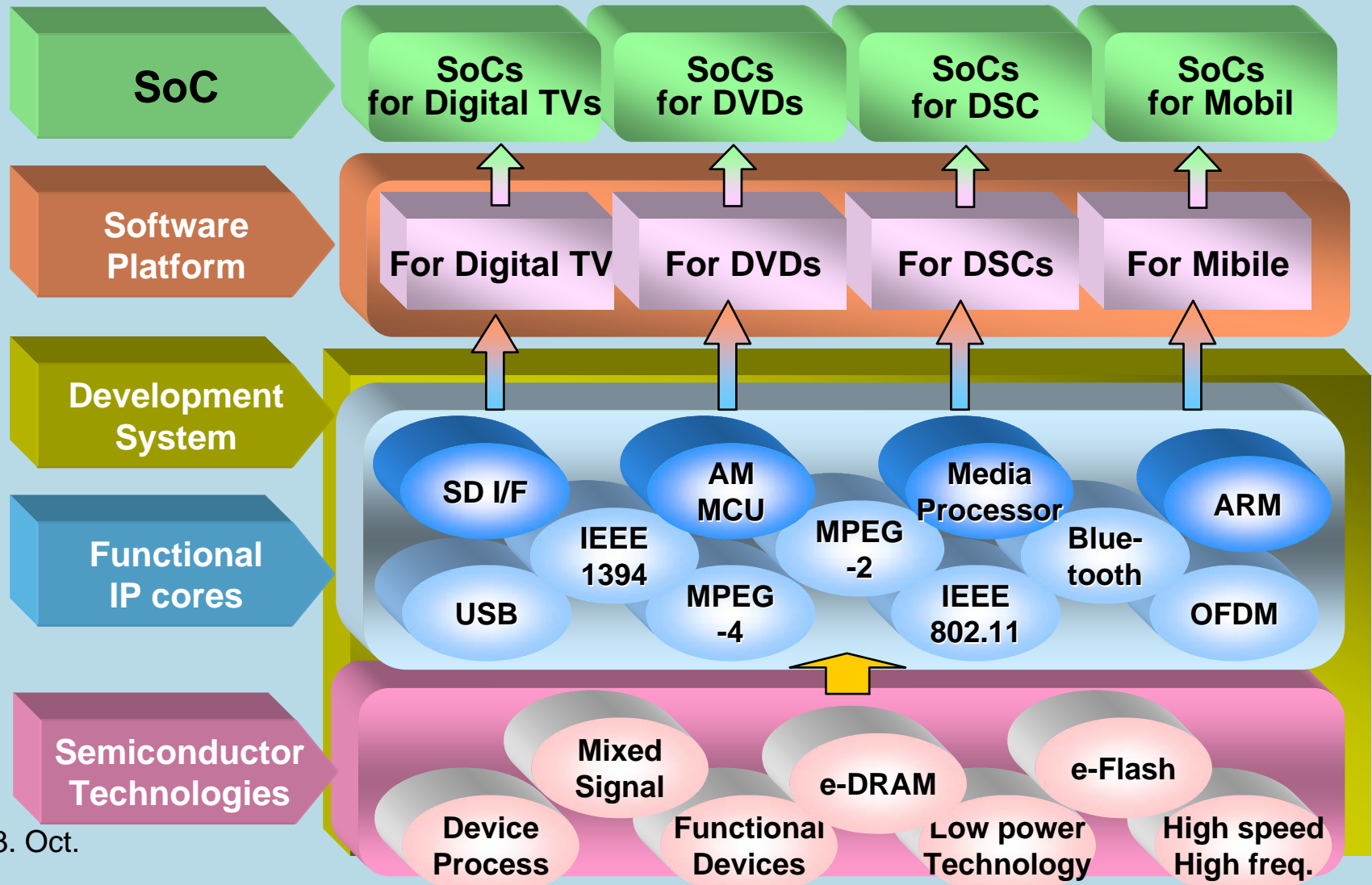
Simulation controller enables fast and automated simulation steps



# Global development management

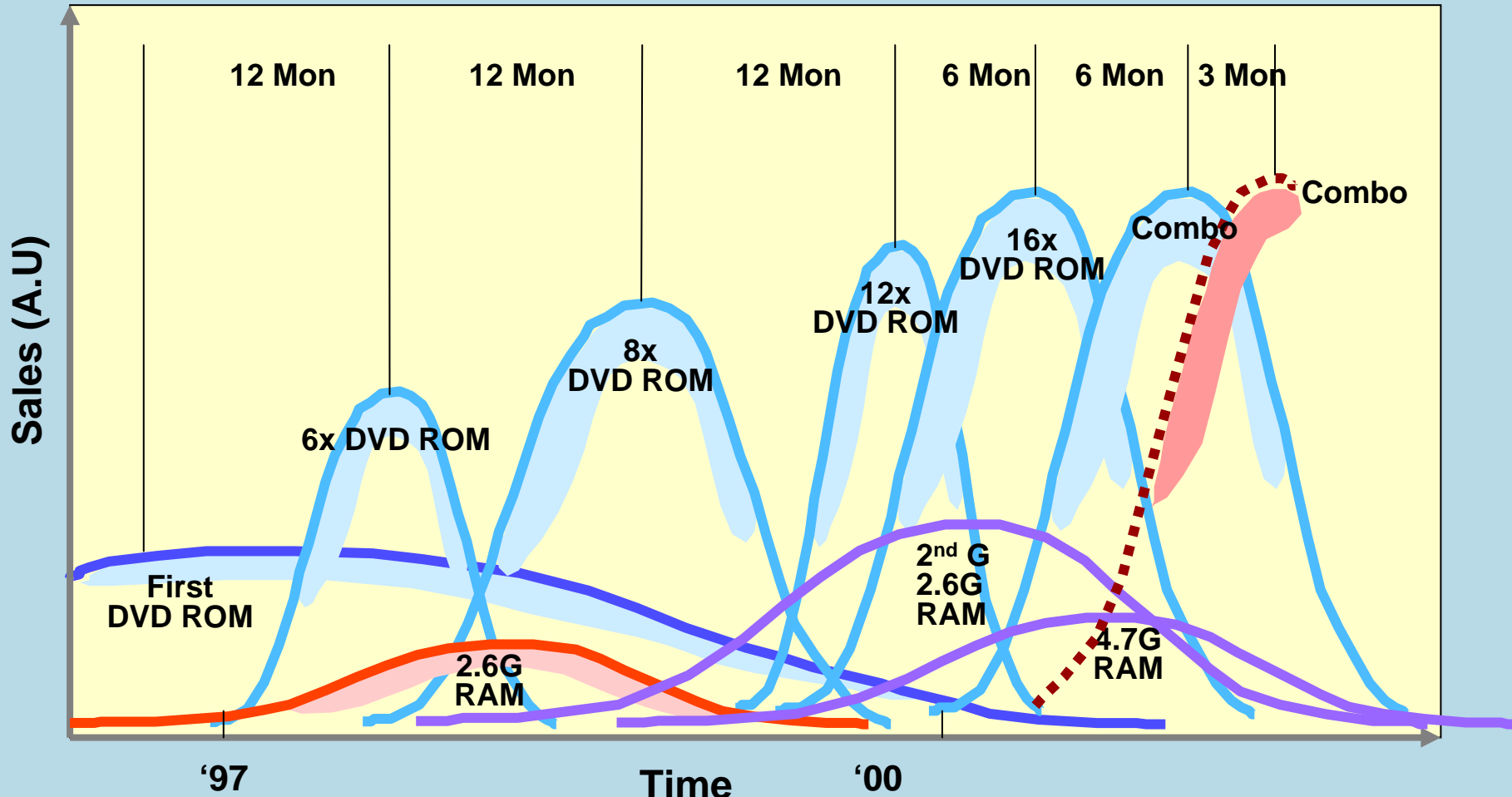
# Development Platforms for SoC

SoC needs several technology layers from system and software to device



# Narrow development time slot

The development time slot is very narrow.  
So “Just in time” develop is required.

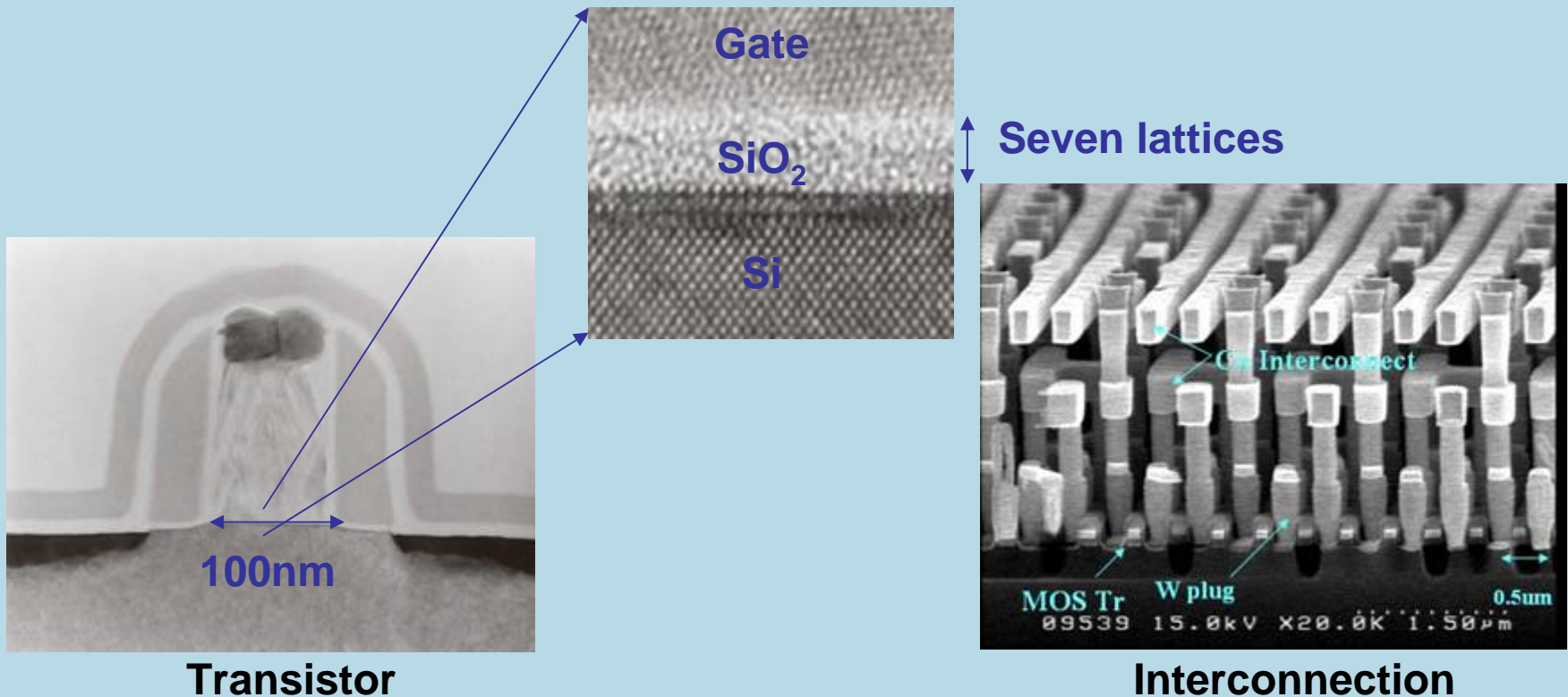


# Scaled CMOS

Current Scaled Si technology is very artistic.

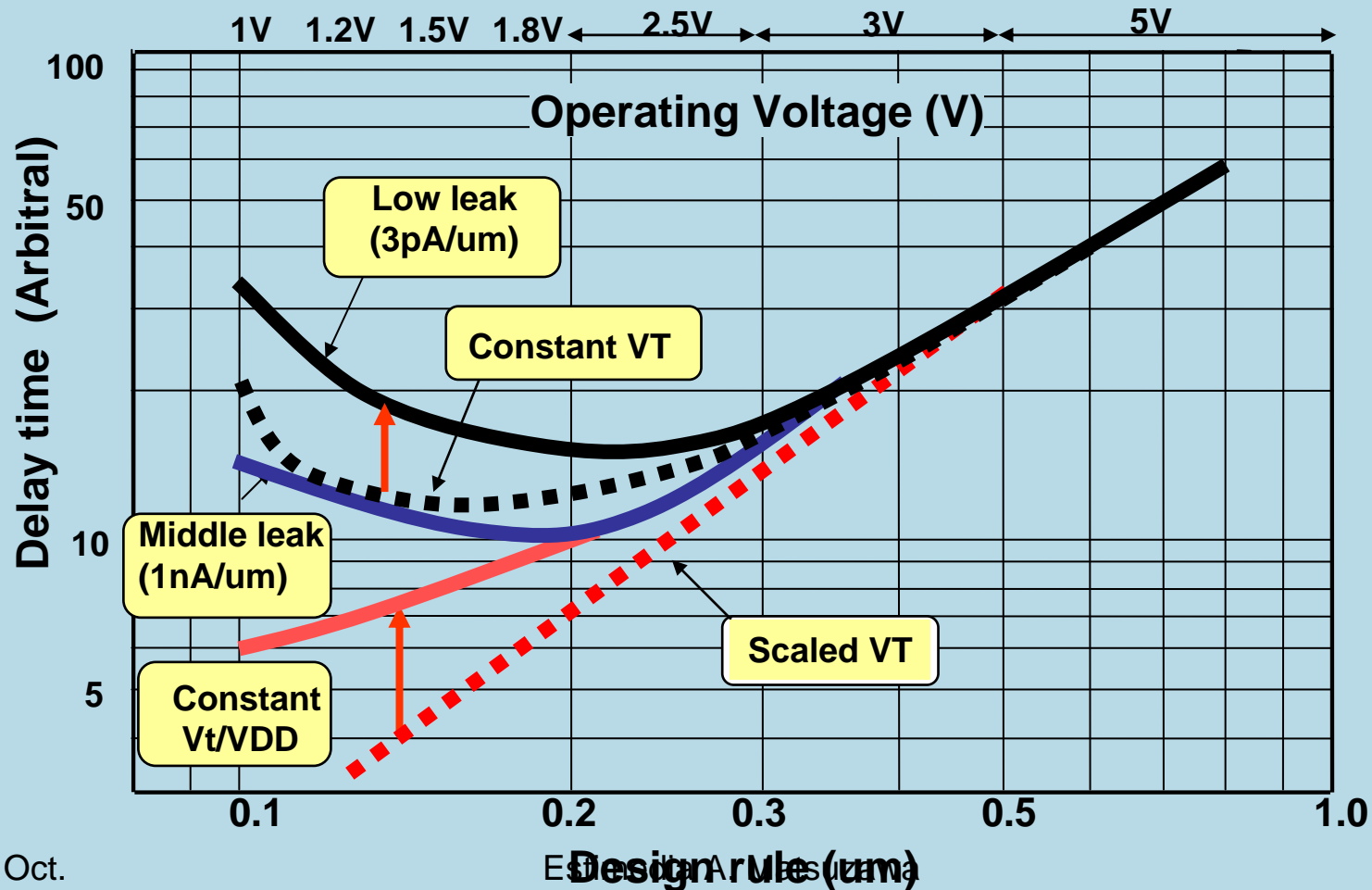
How to control it and how to increase the production yield quickly!

## Matsushita's 0.13um CMOS



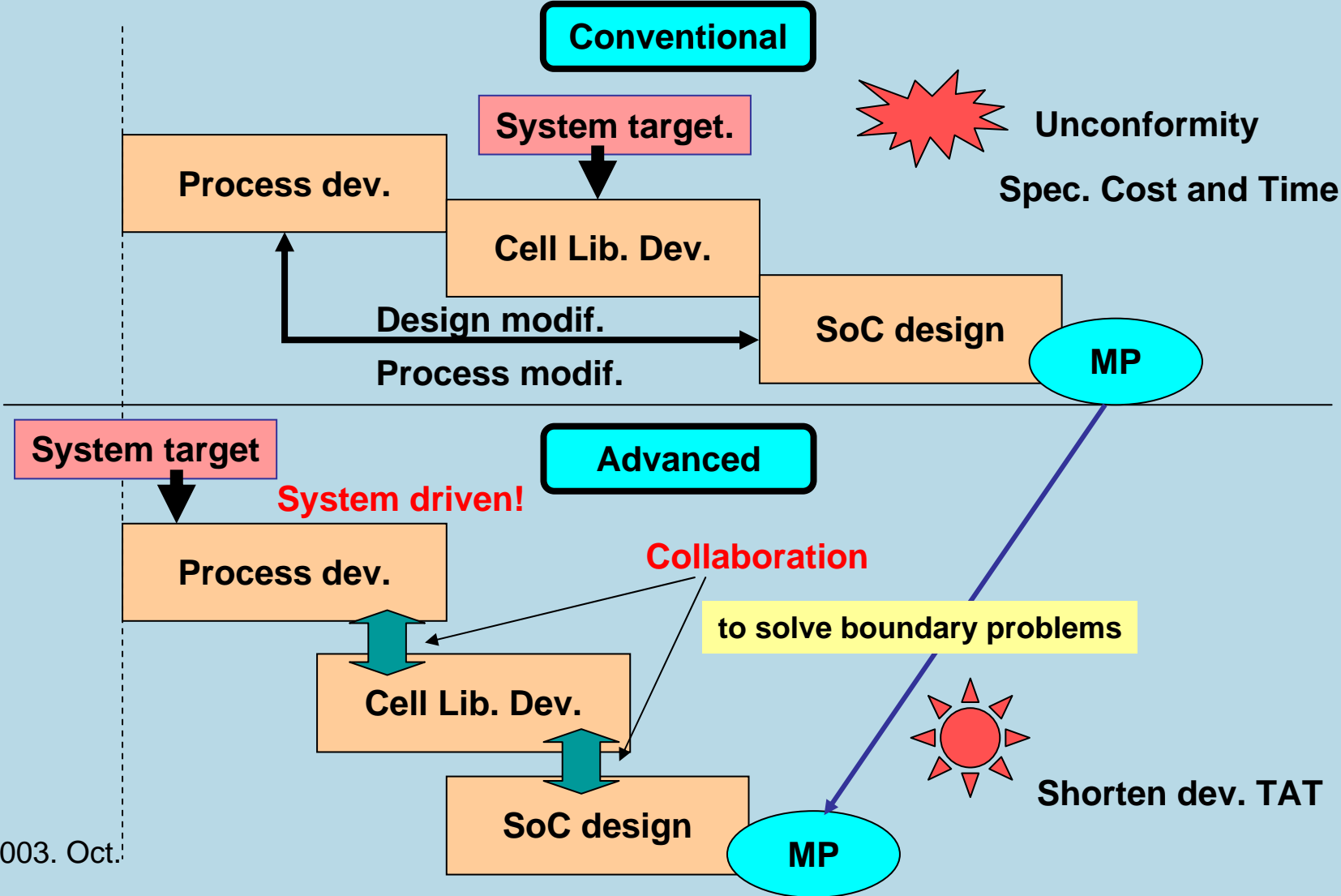
# Choice of transistor

A variety of transistors has increased.  
Choose the proper transistor depending on the systems



# System target driven development

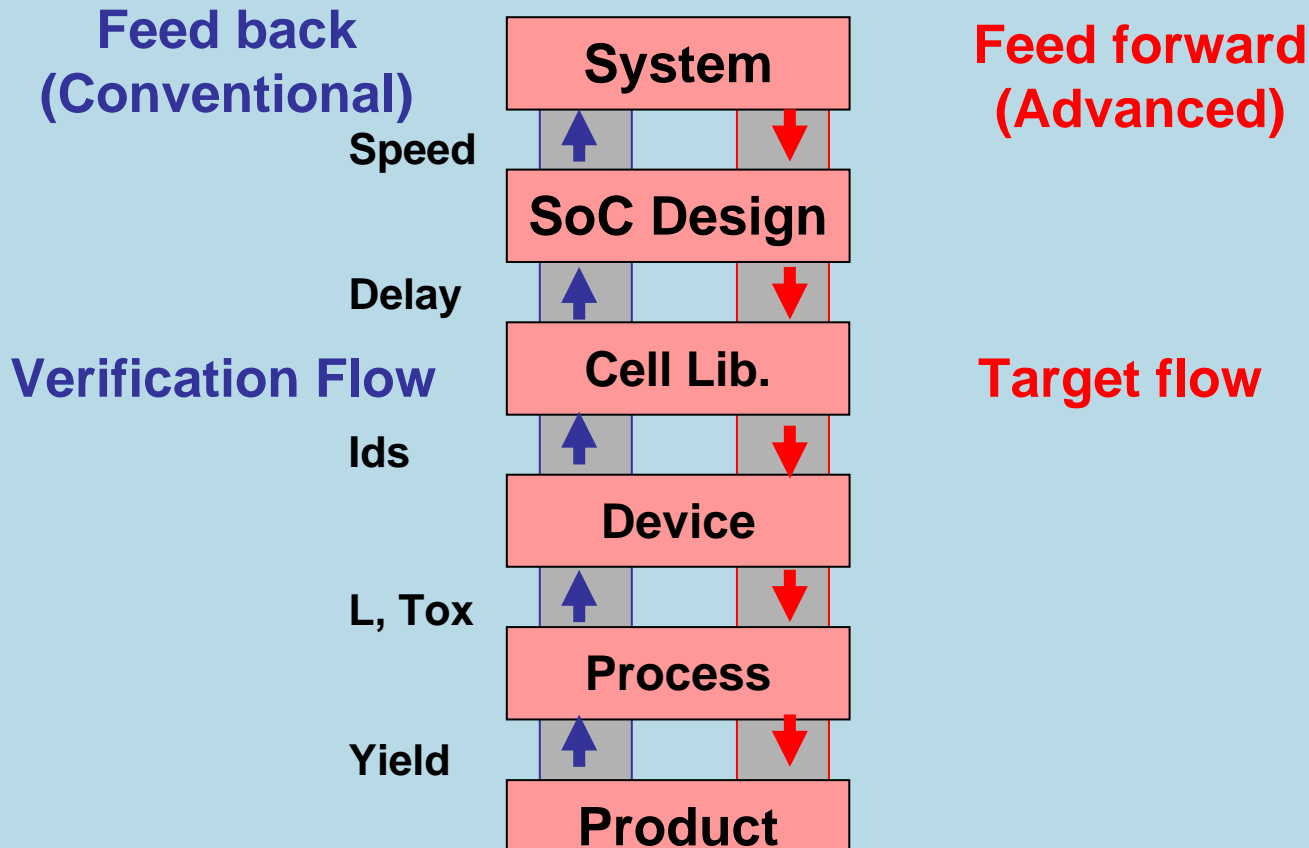
System target driven can reduce unconformities and shorten the TAT.





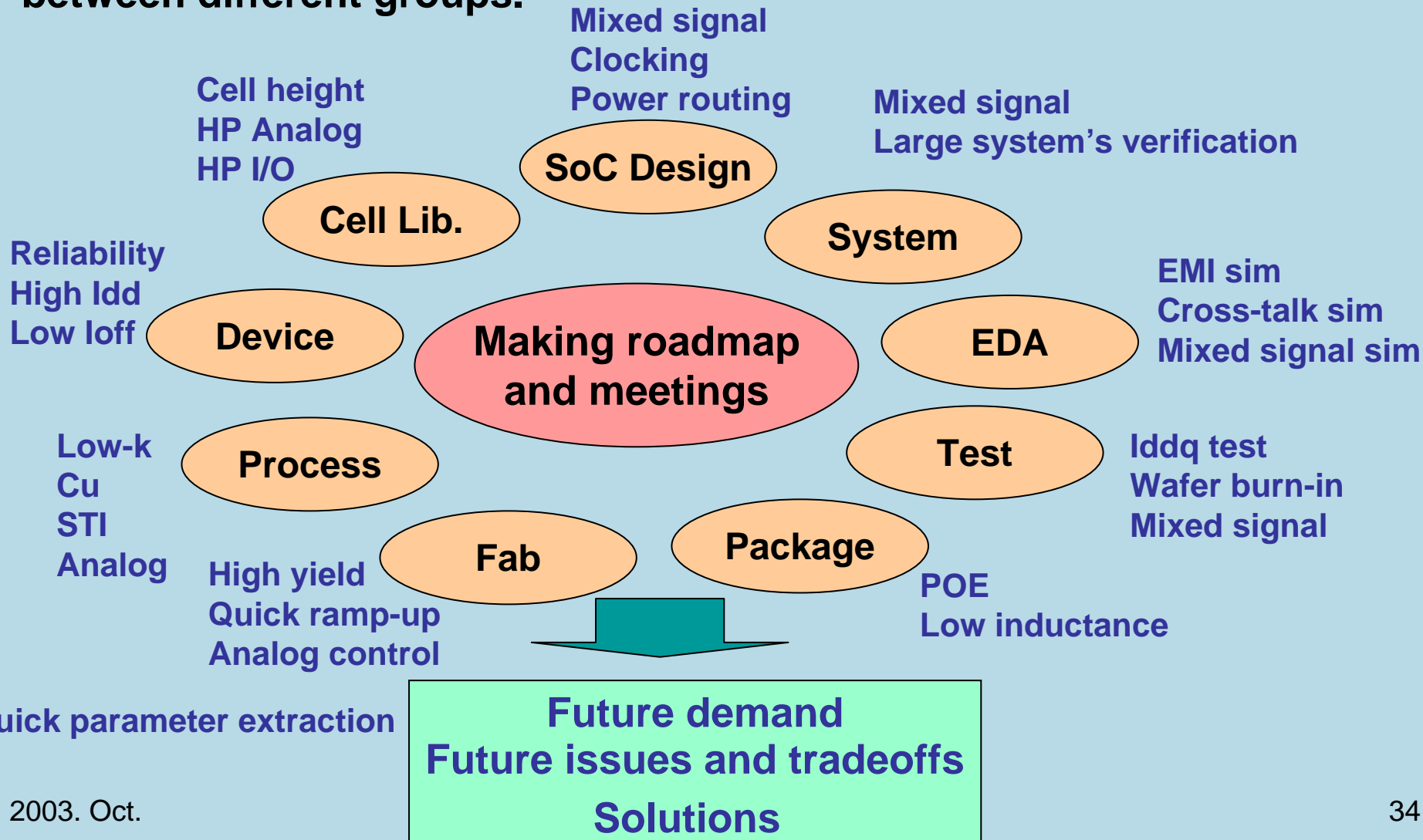
# Bidirectional design flow

**Bidirectional design flow; feed forward flow, as well as feedback flow can pass early targets to different groups. This shorten the TAT and reduce the conflicts.**



# Making roadmap

Making roadmap makes a good communication and a corroboration between different groups.



# Summary

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- Digital consumer electronics based on multimedia technology has emerged and become big market.
- SoC also has become a dominant along with this technology.
- Architecture of SoC should be optimized for the application system.
- The mixed signal technology is vital for SoC.  
Increase the design quality and development speed.
- SoC development needs a variety of technology layers from a system to a device and needs several optimization for the applications.
- A global development managing system is an another key to success.  
Make collaboration and unification over different technology groups to shorten the development time and increase customer satisfaction .