Scalable and Synthesizable Analog IPs

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July 8, 2014.

Background and Motivation

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- **Issues**

  It becomes more difficult to obtain good analog IPs

  - **Insufficient design resources (Designers, Tools)**
  - **Insufficient performance**
  - **Expensive**
  - **Longer development time**

- **Proposed solutions**

  - **Reduce # of analog IPs → One IP for versatile uses**
  - **Scalable IPs**
  - **Reduce the parasitic effect due to layout**
  - **Respect regularity**
  - **Synthesizable IPs**

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Scalable 12bit SAR ADC

for versatile uses

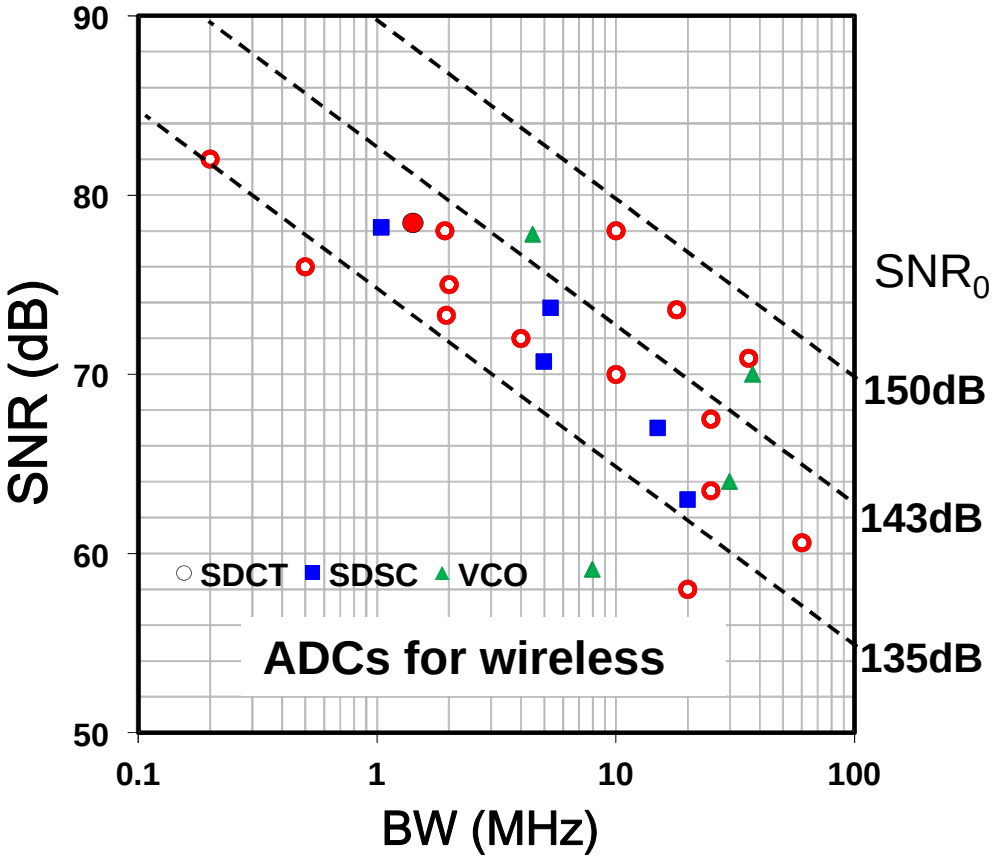
Scalable ADC

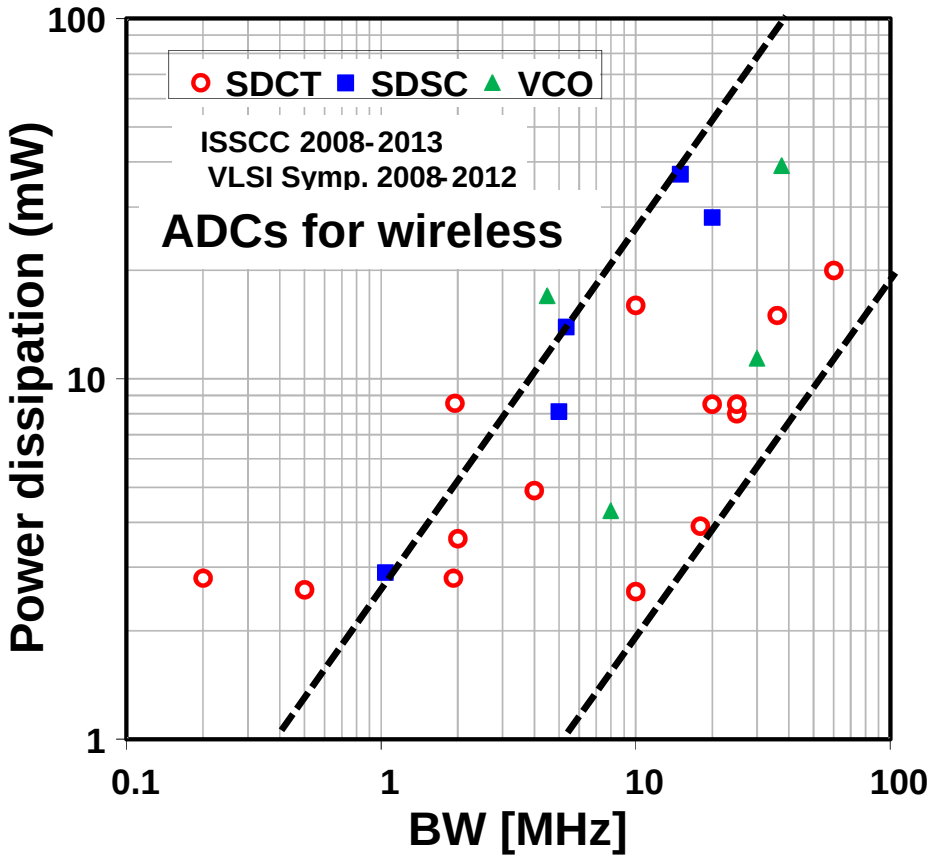
Many ADCs to cover the almost all wireless communications.

SNR can be increased by the reduction of BW, up to 84 dB.
P_d should be minimized and can be reduced by the reduction of BW.

$$SNR \approx SNR_0 - 10\log(BW) \qquad P_d \approx K_1 \cdot BW$$

K_1: 0.2 -- 3 (mW/MHz)





Matsuzawa, A. "Digitally-Assisted Analog and RF CMOS Circuit Design for Software-Defined Radio," Chapter 7, Springer 2011.

SAR ADC : ADC for versatile use

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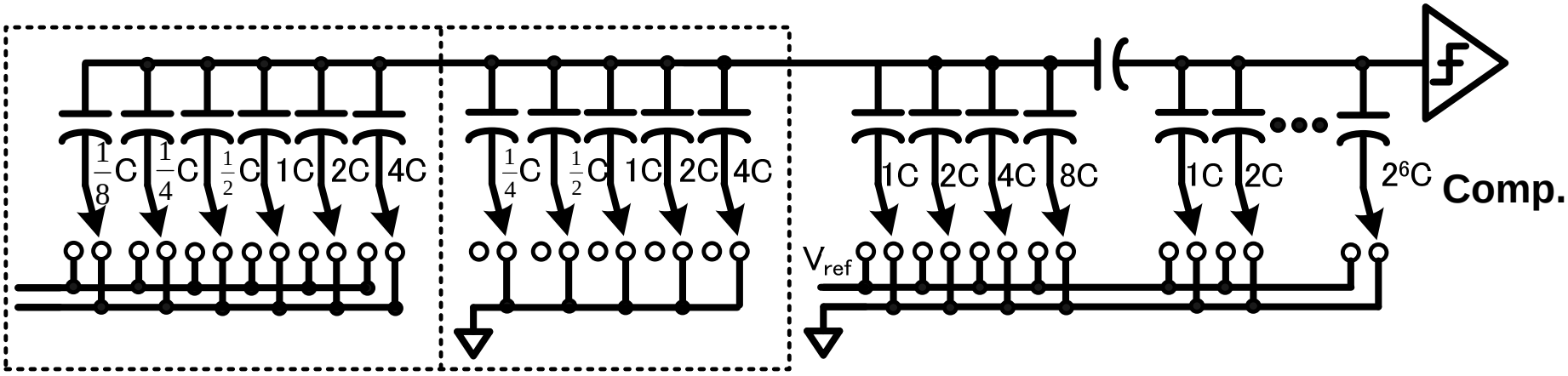
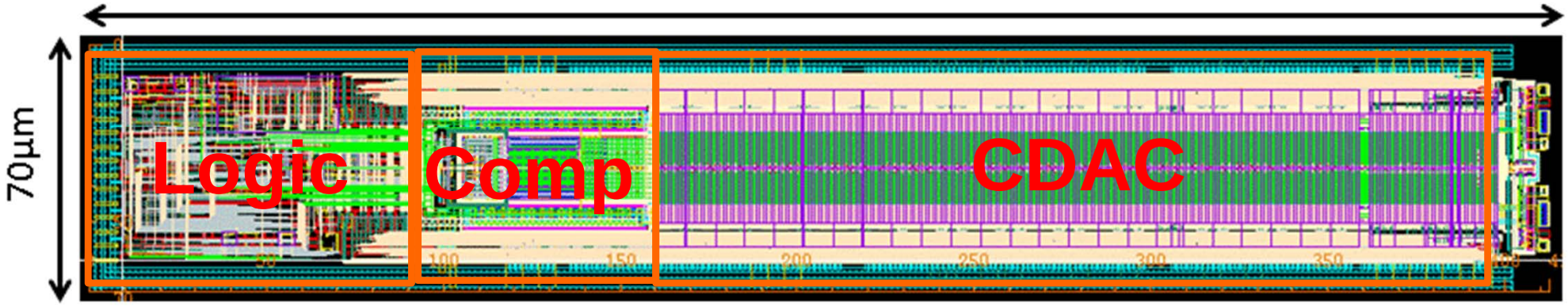
SAR ADC is the most energy efficient ADC.
It can be used for versatile applications.
Conversion errors can be suppressed digitally.



Mismatch CAL. **Parasitic CAL.** **12bit, 65nmCMOS, 0.03mm²**

S. Lee, A. Matsuzawa, SSDM 2013



Dynamic comparator

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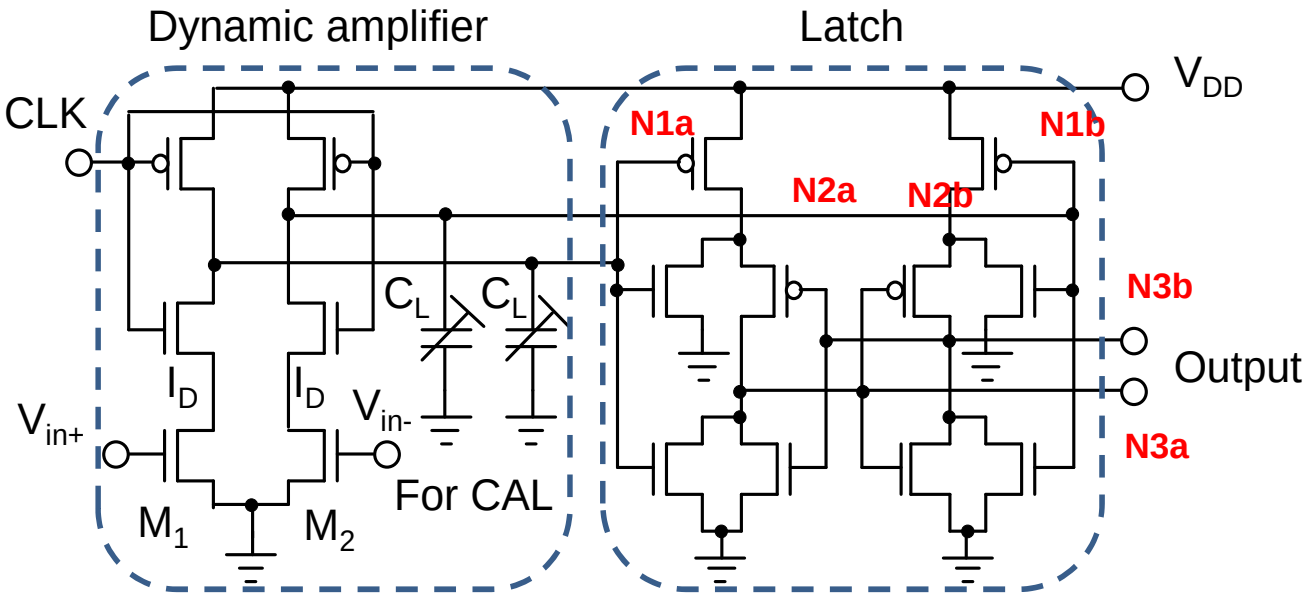
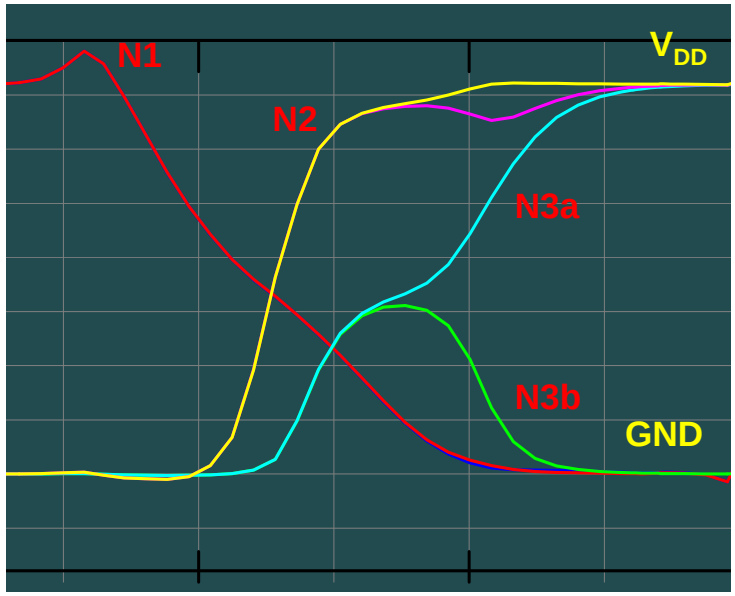
Dynamic comparator doesn't consume any static power. Large noise was an issue, however improved by our proposed circuit using CMOS inter-stage amplifier.





M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

Yusuke Asada, Kei Yoshihara, Tatsuya Urano, Masaya Miyahara, and Akira Matsuzawa, "A 6bit, 7mW, 250fJ, 700MS/s Subranging ADC," A-SSCC, 5-3, pp. 141-144, Taiwan, Taipei, Nov. 2009.

Use of MOM capacitor

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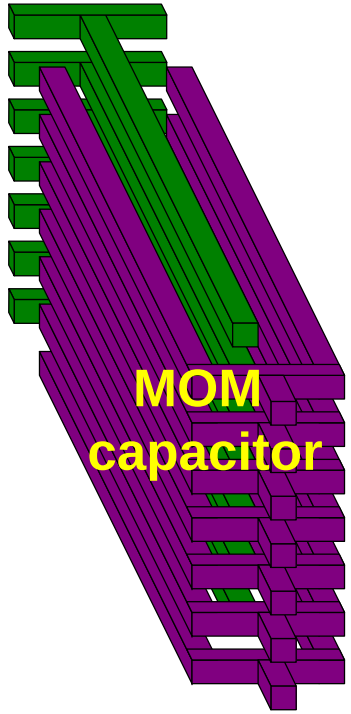
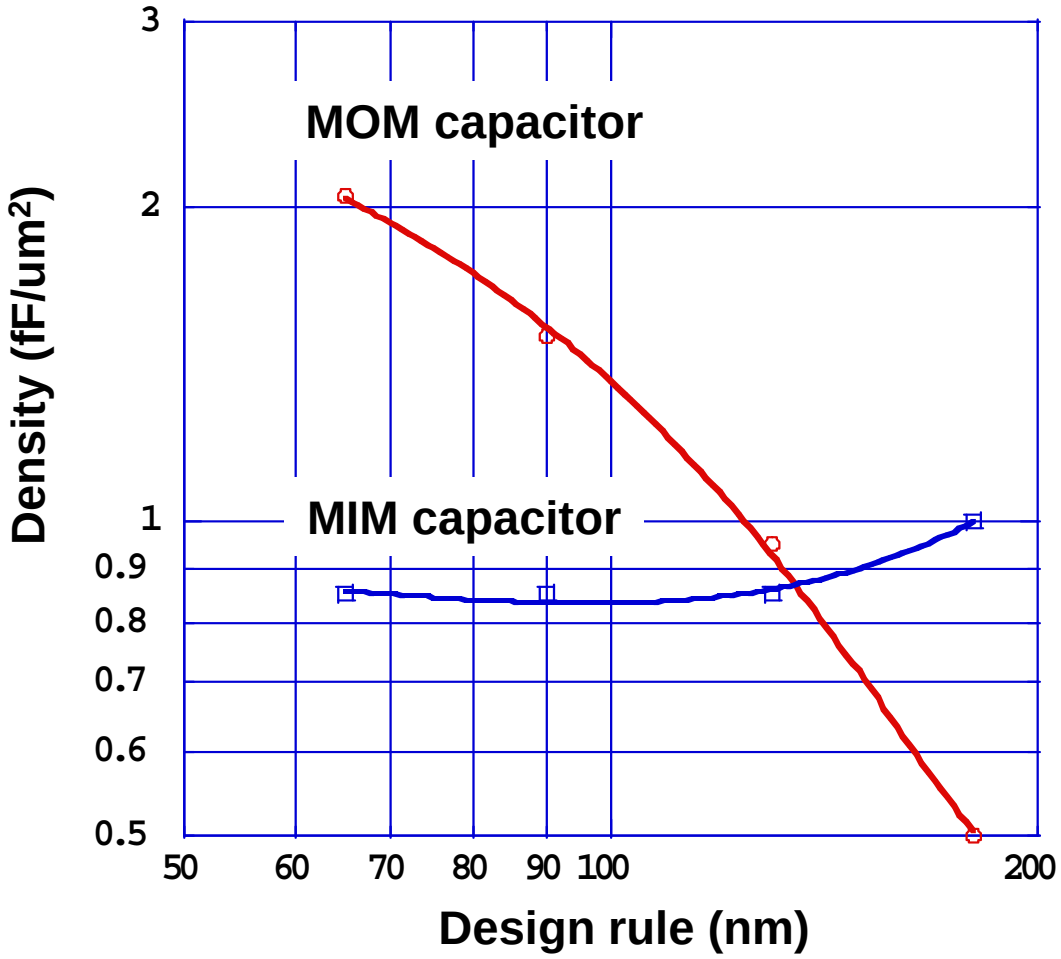
MOM capacitor uses the capacitance between the lateral interconnection.
The capacitor density can be increased by technology scaling.
Smaller occupied area (same C) can be expected by technology scaling.
Furthermore, parasitic capacitance can be controlled.

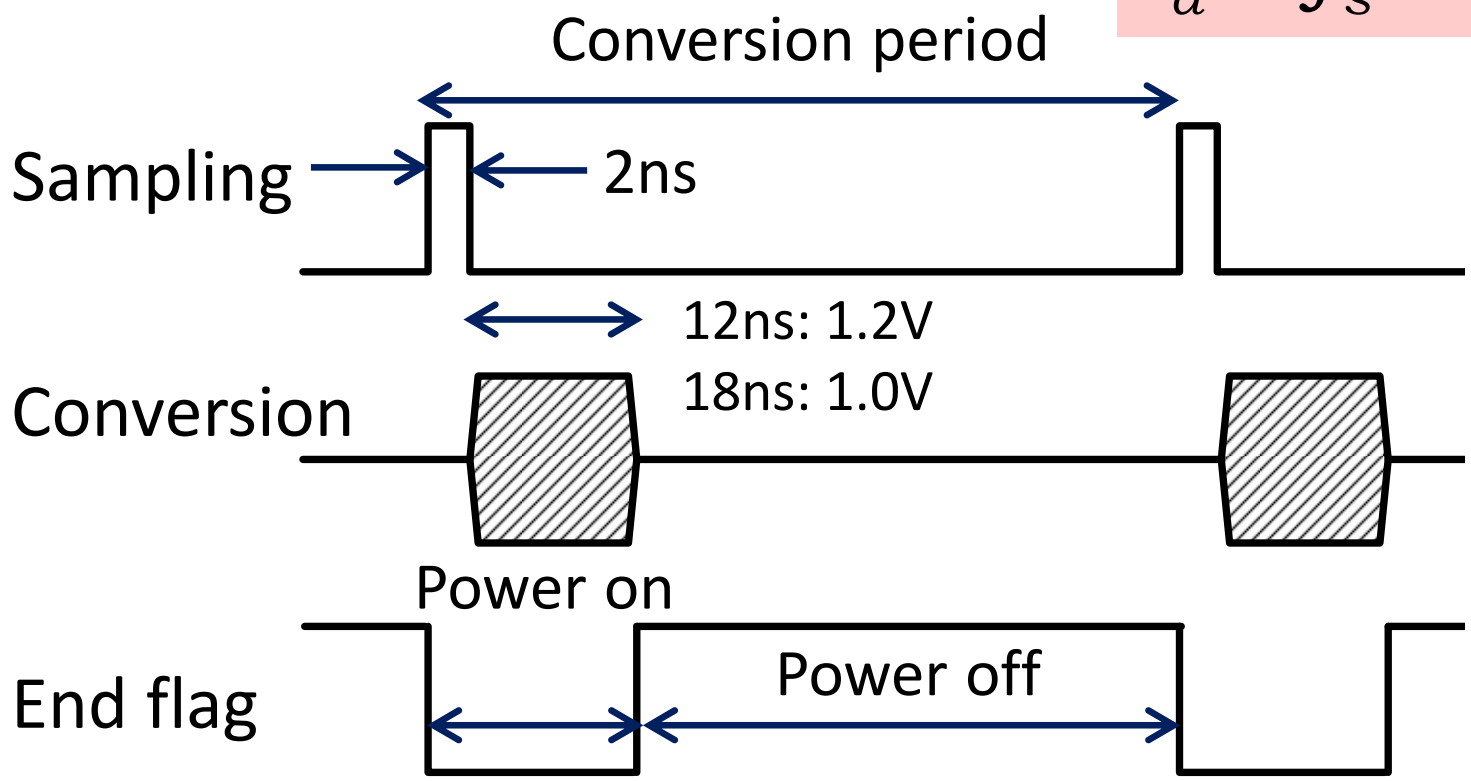




Intermitted operation by self-clocking

Successive comparison is started after the sampling period and ended at 12 conversions.
P_d is proportional to the sampling frequency.
The leakage current can be blocked by using power gating.

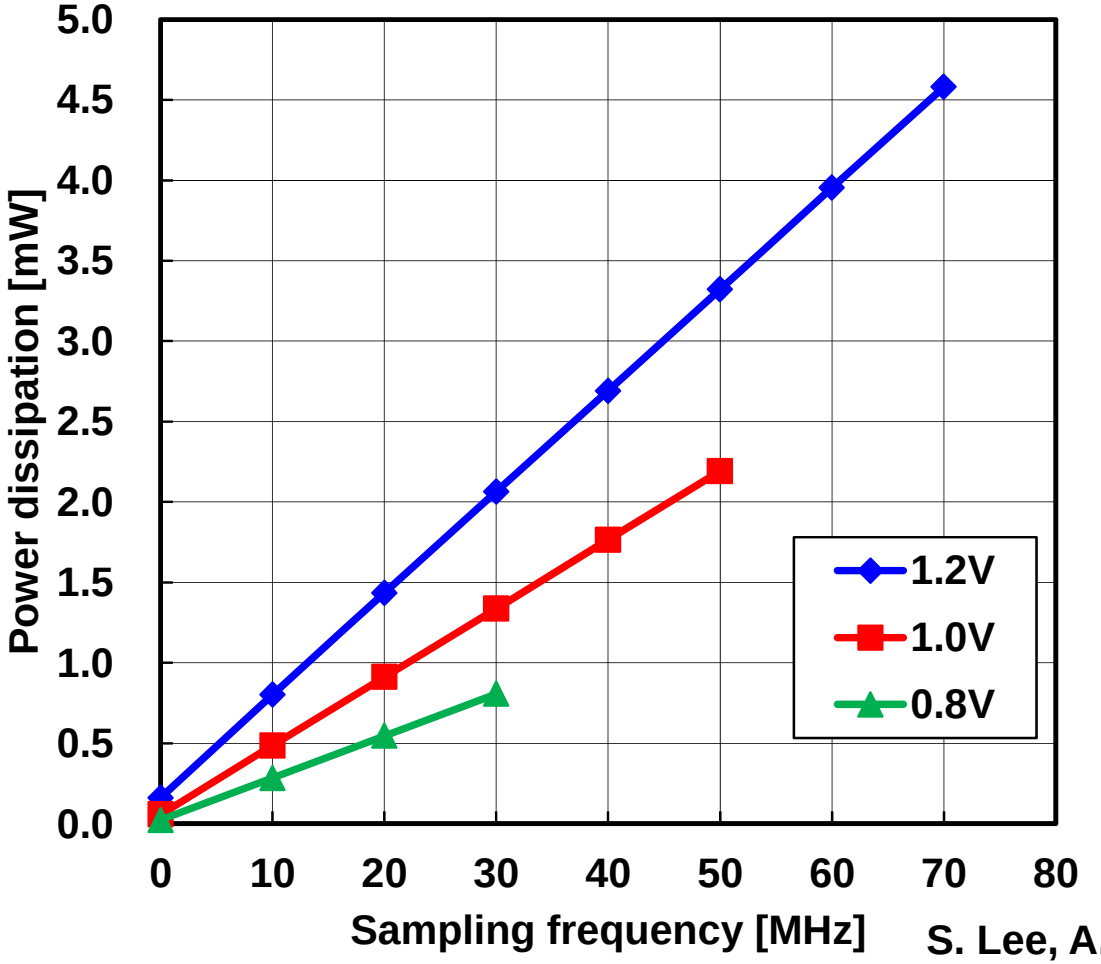
$$P_d = f_s \times E_d$$



Scalable power dissipation

P_d is completely proportional to the sampling frequency.
Therefore an ultra-low power is possible at low speed operation.
Further low power is possible by using low voltage operation.

Suitable for the versatile uses; wireless and sensor



50MSps: 2mW
5MSps: 200uW
500KSps: 20uW
50KSps: 2uW
5kSps: 0.2uW

S. Lee, A. Matsuzawa, et al., SSDM 2013

Performance comparison

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- **Highest conversion rate：70MSps**
- **Lowest voltage：0.8V**
- **Lowest P_d：2.2mW at 50MSps**
- **Smallest FoM：28fJ**
- **Smallest area：0.03mm²**

12bit SAR ADCs

	This work			[3]	[4]
Resolution (bit)	12			12	12
V_{DD} (V)	0.8	1	1.2	1.2	1.2
fsample (MHz)	30	50	70	45	50
Pd (mW)	0.8	2.2	4.6	3	4.2
SNDR (dB)	62	64	65	67	71
FoM (fJ) Nyq/DC	81/28	62/33	100/45	36/31	36/29
Technology (nm)	65			130	90
Occupied area(mm^2)	0.03			0.06	0.1

S. Lee, A. Matsuzawa, et al., SSDM 2013.
[3] W. Liu, P. Huang, Y. Chiu, ISSCC, pp. 380-381, Feb. 2010.
[4] T. Morie, et al., ISSCC, pp.272-273, Feb. 2013.

Performance scalable ADC

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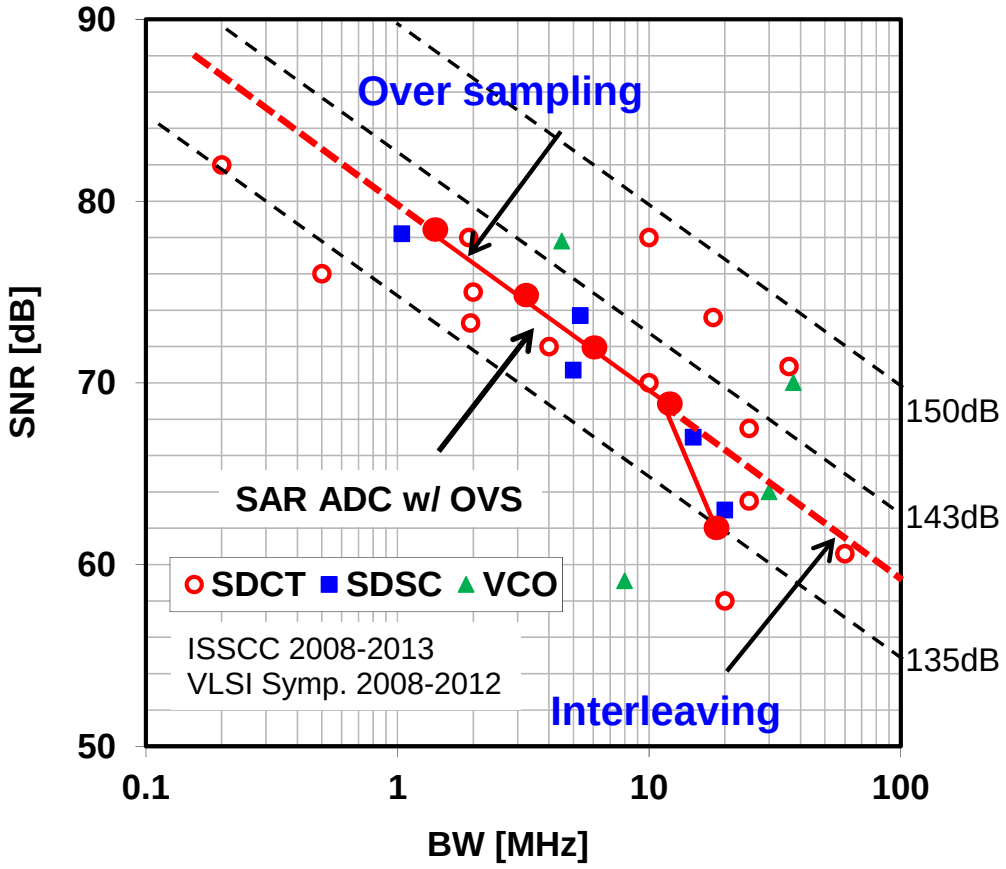
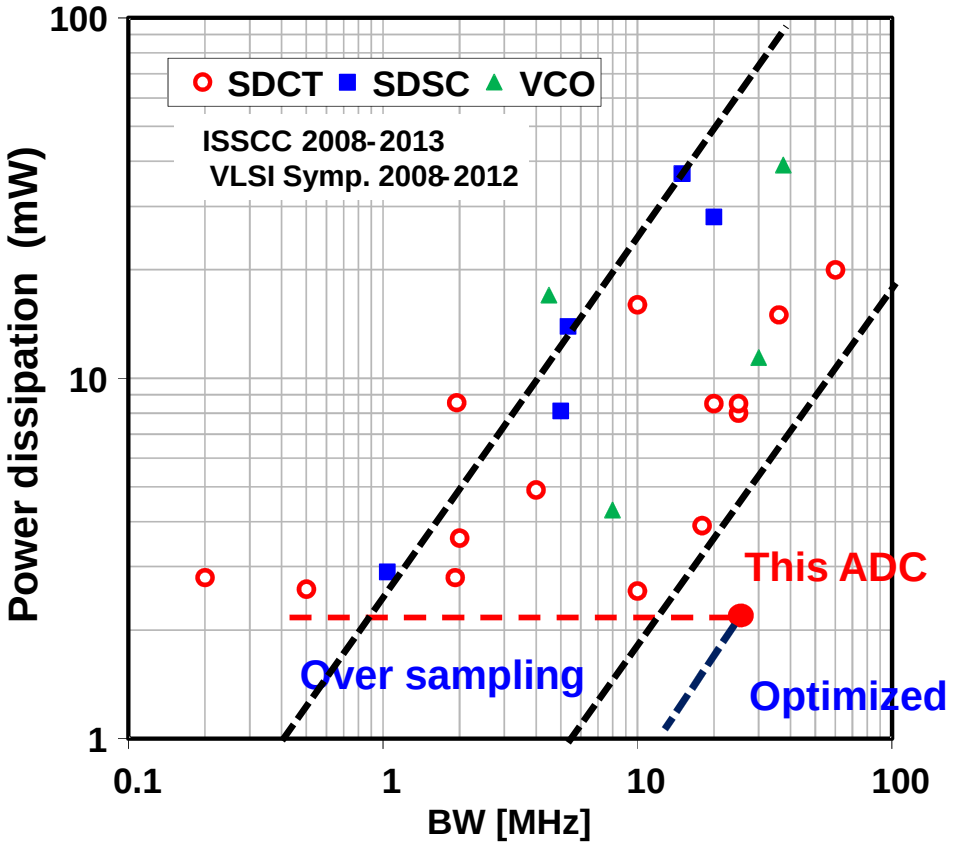
SNR can be increased up to 78 dB by reducing BW.
Smallest P_d among ADCs for wireless communications.

84 dB will be attained by dither and DEM method.
SNR_0 is 140 dB and it can be increased.

S. Lee, A. Matsuzawa, et al., SSDM 2013



1V, 50MSps Operation



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Layout-driven circuit design and synthesizable analog IPs

Conventional idea for analog IP design

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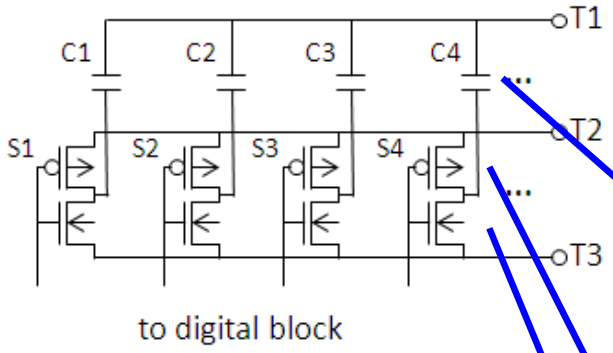
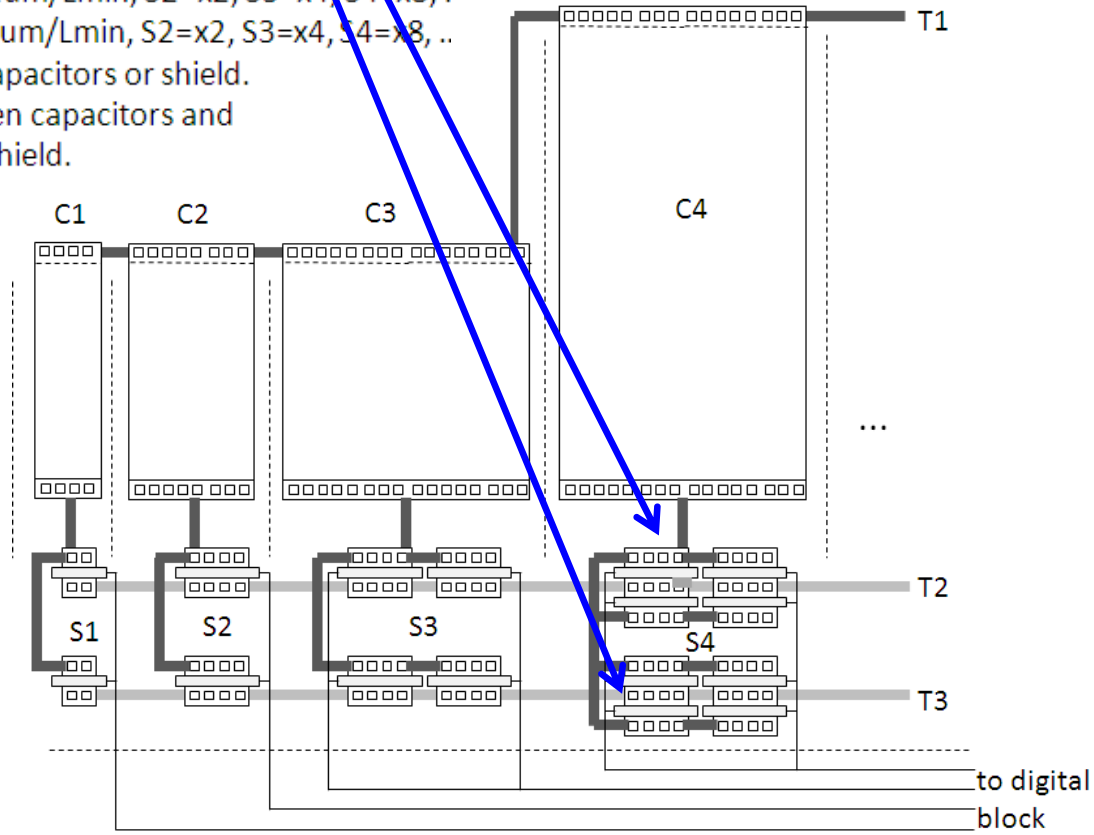


Place the components
Route wires between them

cell generator

1. C1=20fF, C2=40fF, C3=80fF, C4=160fF, ..
2. S1 NMOS W/L=2um/Lmin, S2=x2, S3=x4, S4=x8, .
3. S1 PMOS W/L=2um/Lmin, S2=x2, S3=x4, S4=x8, ..
4. Separate each capacitors or shield.
5. Separate between capacitors and digital block or shield.



Issue of conventional idea for analog design

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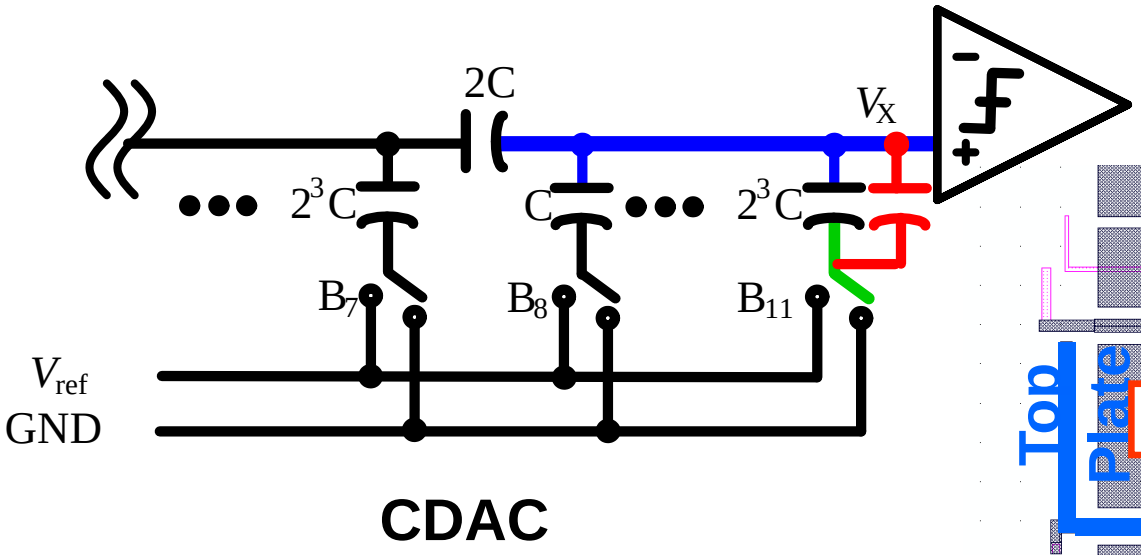
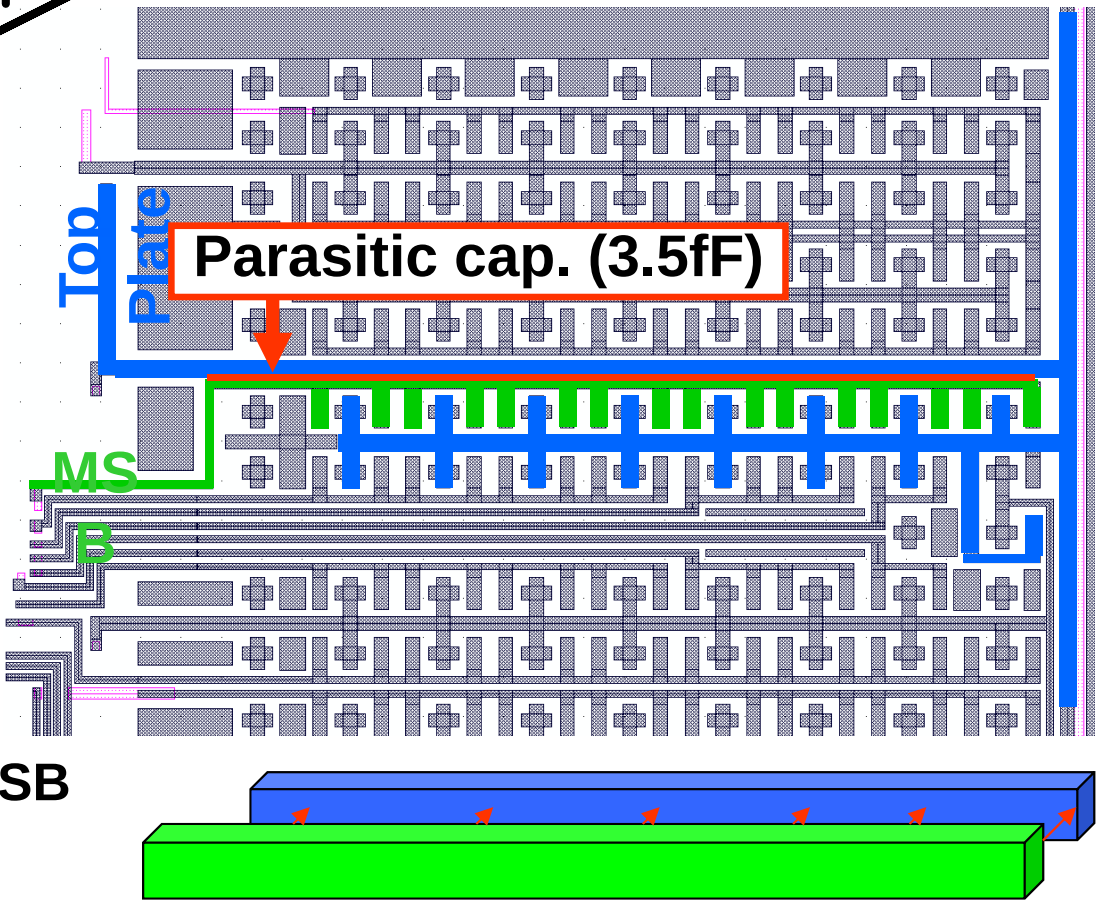
A conventional idea of Place the components and Route them causes parasitic components essentially and it results in performance degradation.



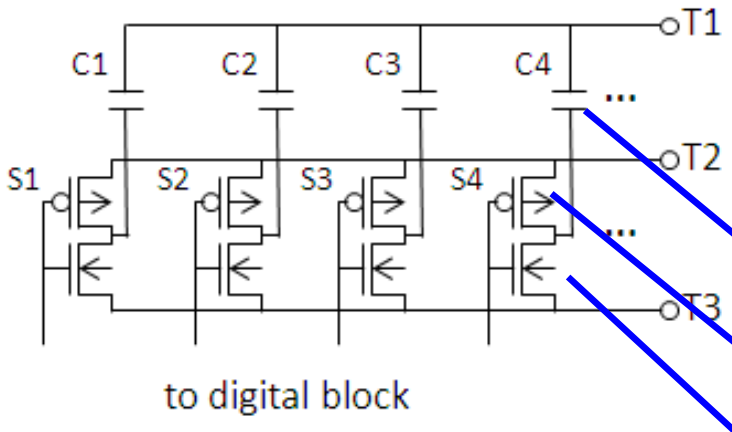
CDAC

Layout of CDAC

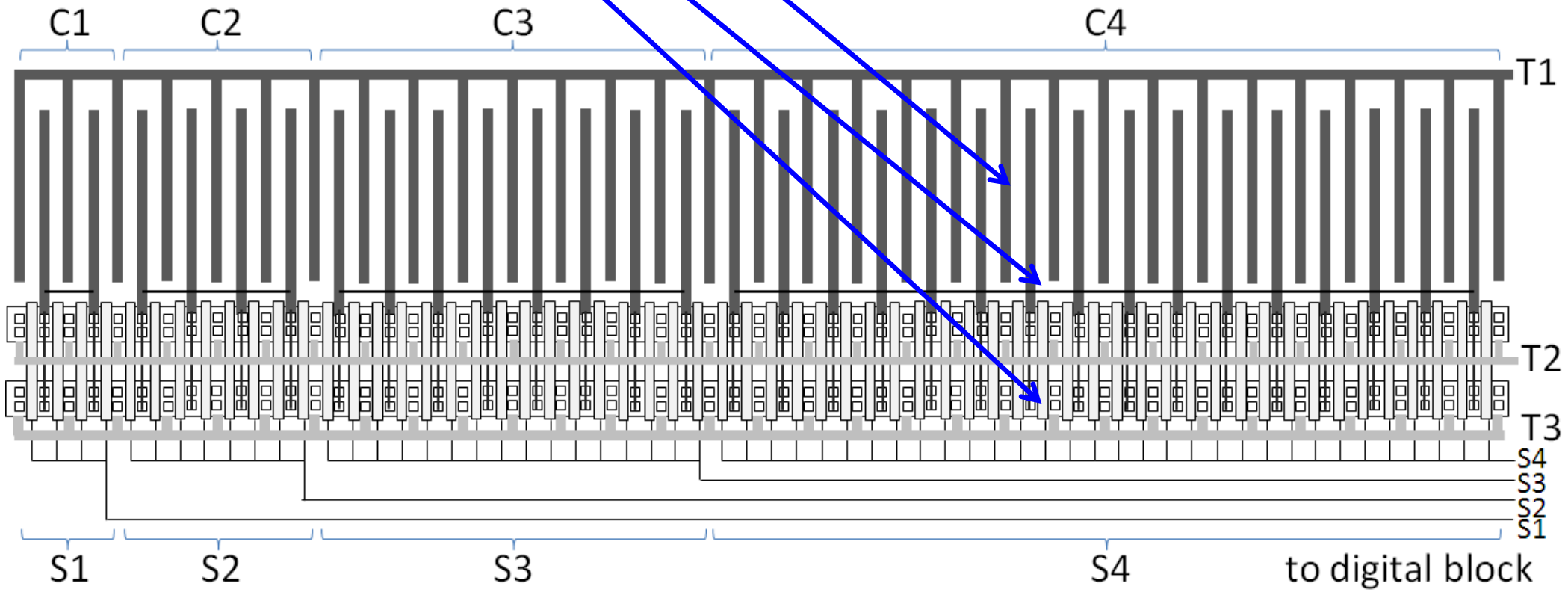


Parasitic capacitance (3.5 fF) Between top prate and bottom plates Causes large conversion error of 50 LSB (12 bit).

Regular layout driven design



Avoid wires between components
Wire itself is the component
Respect the regularity
Pitch should be aligned



Ideal layout design

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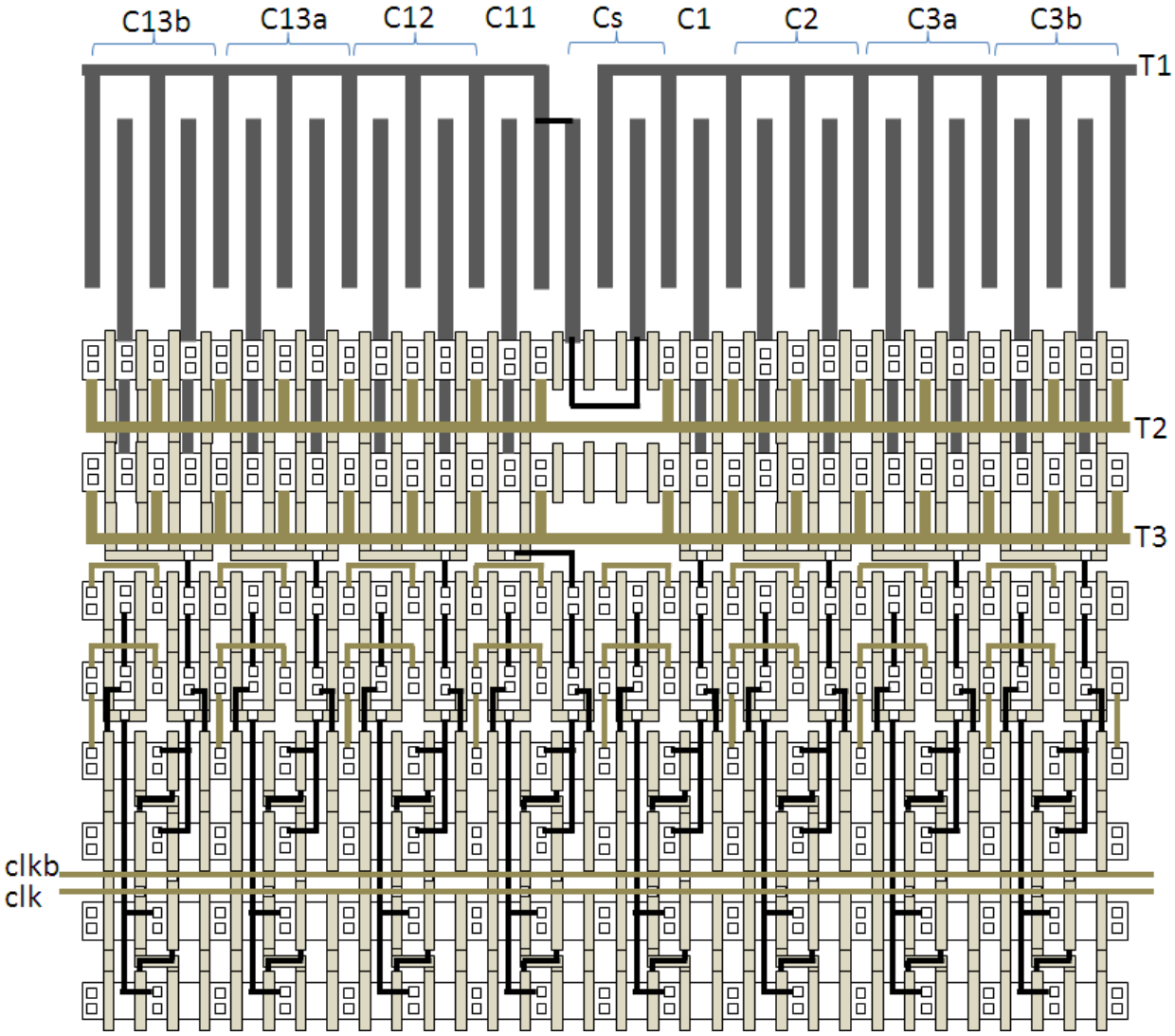
Pitch is aligned.
It minimizes parasitic component , wire length, delay and capacitance.
Low power, high speed, small area, and high robustness can be realized.



SAR ADC

Synthesized layout

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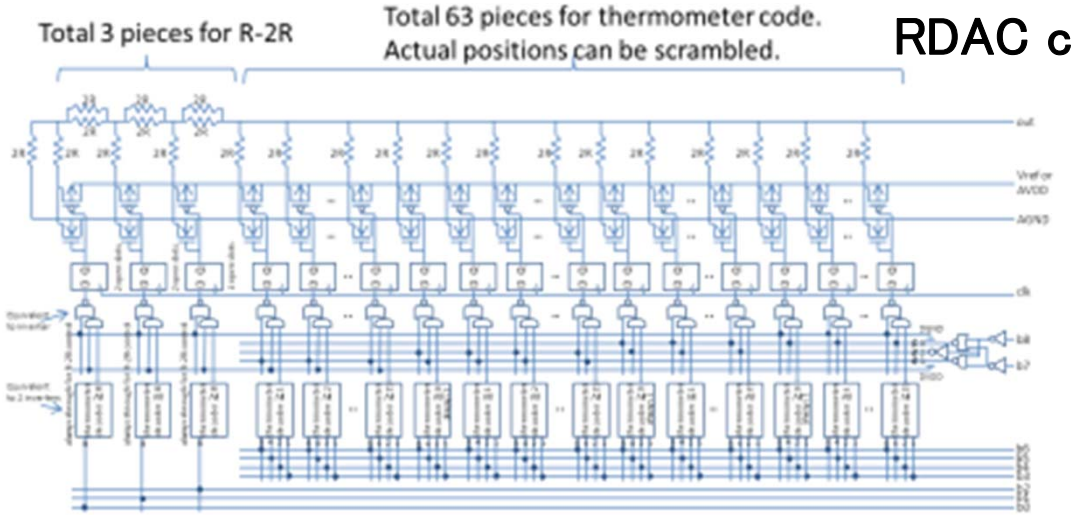
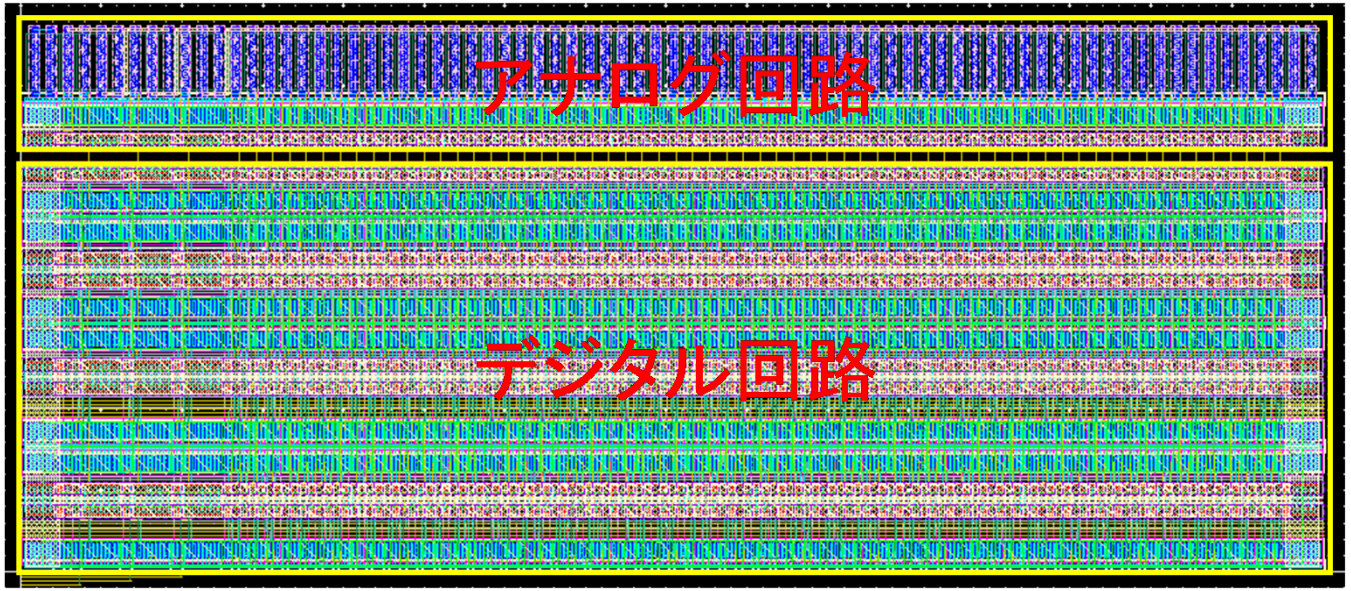
We can synthesize analog layout with SKILL language



RDAC circuit

Automated optimization
Automated layout with SKILL language

RDAC layout composed by skill language



Design flow for analog IP synthesis

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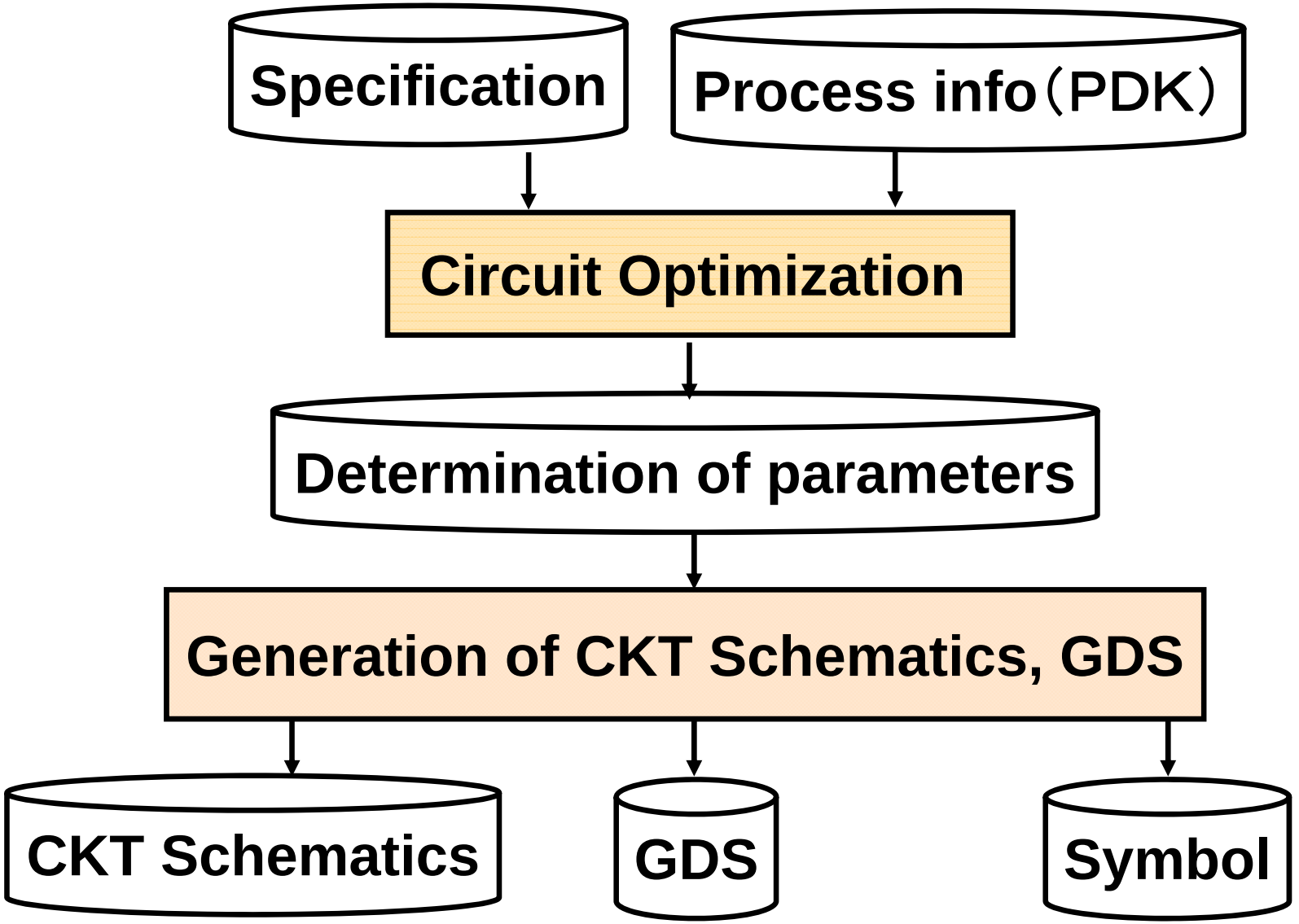
Automated design for circuit and layout



Circuit schematic and layout

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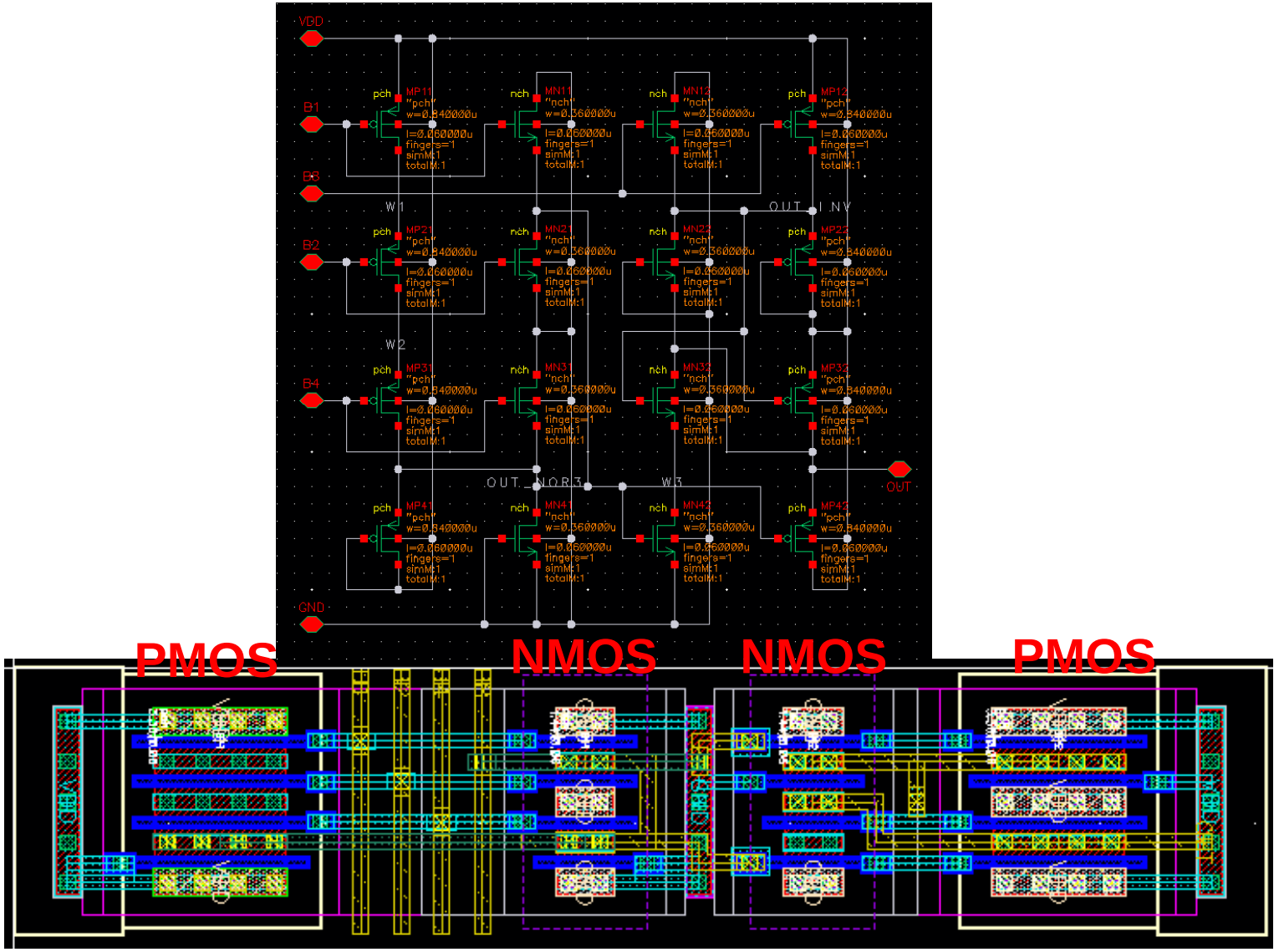
Logic gates should have regularity and launch the automated layout.



Align the layout pitch

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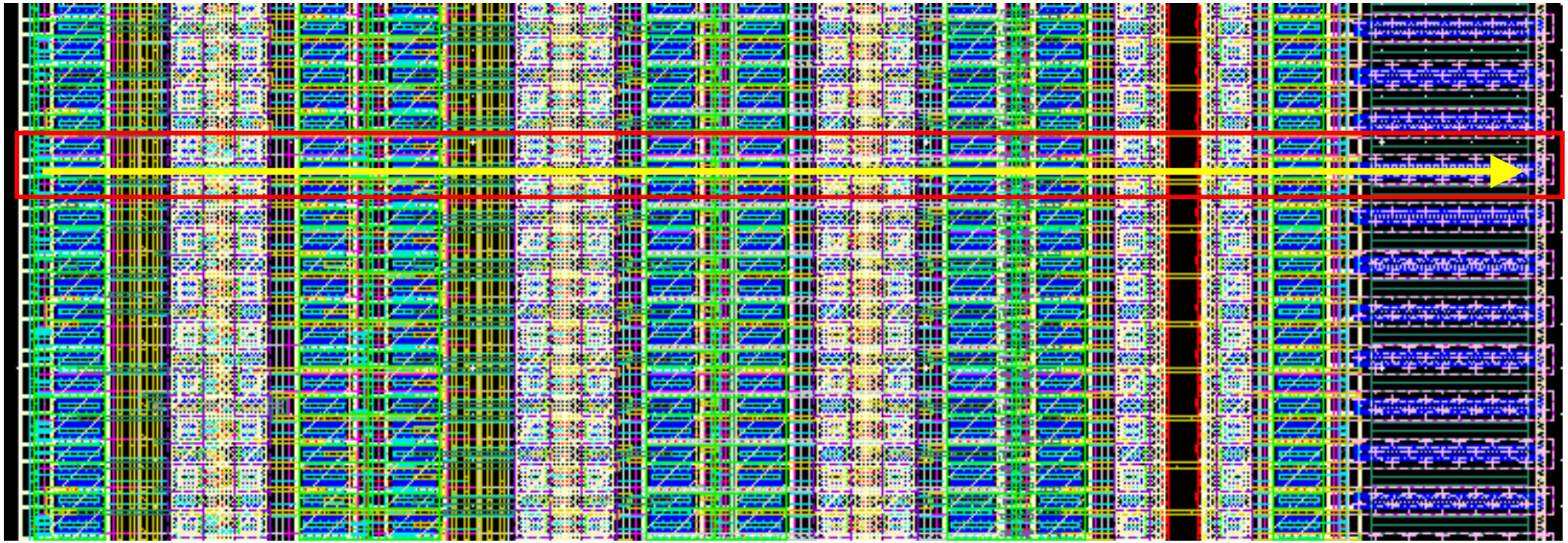
Logic gates, DFFs, switches, and resistors are aligned



Proposed analog IP design and business

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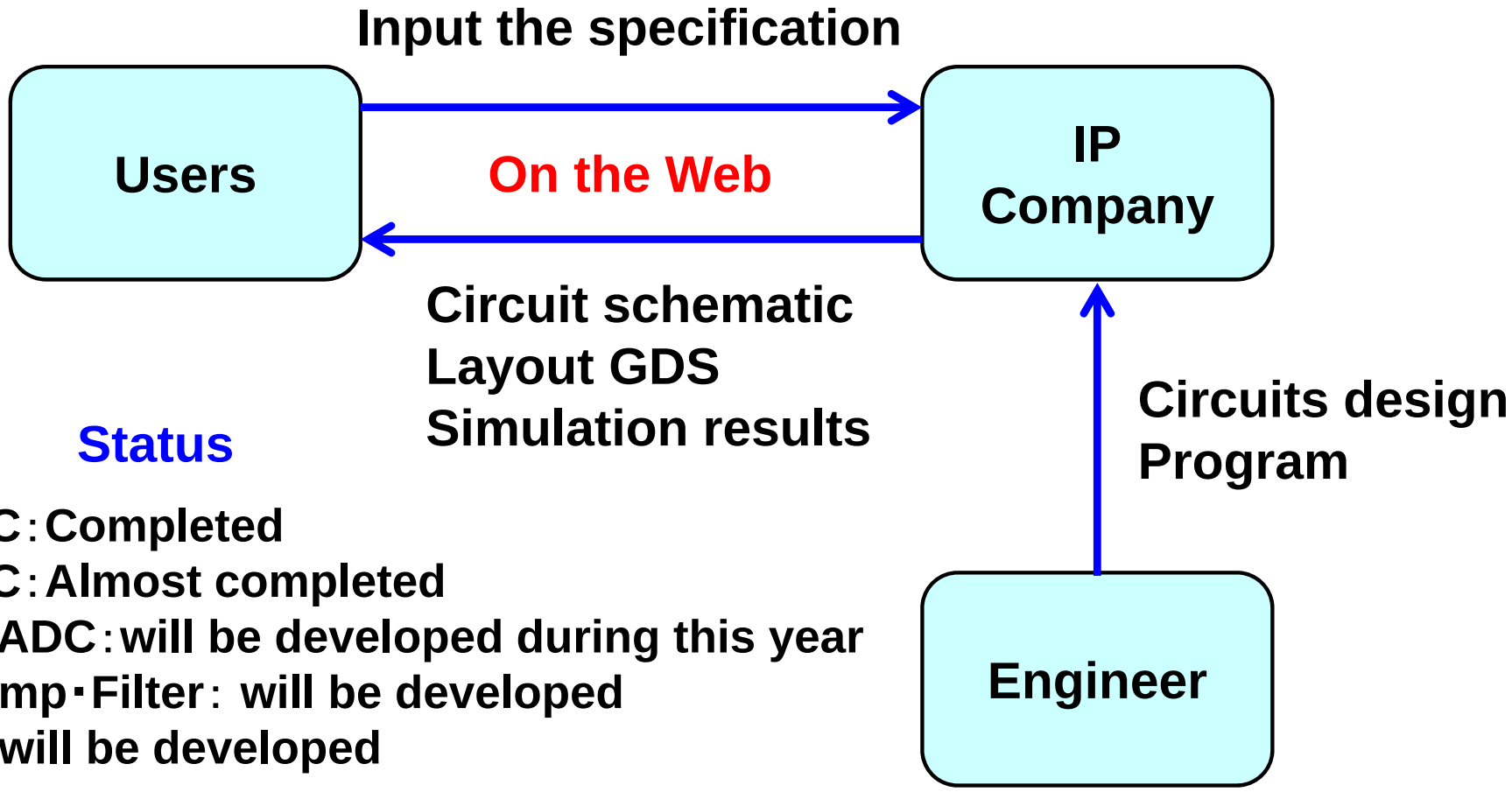
Circuits should be synthesized automatically.
Users can obtain analog IPs immediately with less money.
No limitation for # of design requests



Status

RDAC：Completed
CDAC：Almost completed
SAR ADC：will be developed during this year
OP Amp・Filter： will be developed
PLL：will be developed

Summary

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- **Issues**

  It becomes more difficult to obtain good analog IPs

  – **Insufficient design resources, Insufficient performance Expensive, and Longer development time**

- **Proposed solutions**

  – **One analog IP core for versatile uses**
  Ex: Scalable 12b SAR ADC for versatile use

  – **Regularity driven analog layout**

    - **Avoid wires between components by making wire component**
    - **Respect the regularity and pitch should be aligned**

  – **Synthesize analog IPs with Skill language**

  – **Propose new analog IP design method and business.**