RF circuit design: Basics

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Contents

• Building blocks in RF system and basic performances
• Device characteristics in RF application
• Low noise amplifier design
• Mixer design
• Oscillator design
Basic RF circuit block

RF systems are composed of limited circuits blocks. LNA, Mixer, and Oscillator will be discussed in my talk.
Basic functions of RF building blocks

Amplifier, frequency converter (mixer + oscillator), and filter are basic function blocks in RF system.
RF Amplifier

- **Gain:** Amplify small signal or generate large signal.
- **Noise:** Smaller noise and larger SNR.
- **Linearity:** Smaller non-linearity.

Non-linearity generates undesired frequency components.

\[ v_{out}(t) = \alpha_1 v_{in}(t) + \alpha_2 v_{in}^2(t) + \alpha_3 v_{in}^3(t) + \ldots \]

\[
(\cos(\omega_1 t) + \cos(\omega_2 t))^2 = 2 + \cos(2\omega_1 t) + \cos(2\omega_2 t) + \cos((\omega_1 - \omega_2) t) + \cos((\omega_1 + \omega_2) t)
\]

\[
(\cos(\omega_1 t) + \cos(\omega_2 t))^3 = \frac{1}{2} \cos(2\omega_1 - \omega_2) t + \frac{1}{2} \cos(2\omega_2 - \omega_1) t + \ldots
\]
Distortion and noise are important factors in RF amplifier, as well as power and gain.
\[ \text{Noise Floor} = -174 \text{dBm} + NF + 10 \log BW \]

\[ \text{SFDR: Spurious free dynamic range} \]

The input power range over which third order inter-modulation products are below the minimum detectable signal level.

\[ SFDR = \frac{2}{3} (IIP_3 - \text{Noise Floor}) - SNR_{\text{min}} \]

\[ \text{BDR: Blocking dynamic range} \]

\[ BDR = P_{1dB} - \text{Noise Floor} - SNR_{\text{min}} \]

\[ \text{MDS: Minimum detectable signal level} = \text{Noise Floor} + SNR_{\text{min}} \]
Non-linearity

$CP_{1dB}$: The input level at which the small signal gain has dropped by 1dB.

$$CP_{1dB} = \sqrt{0.145 \left| \frac{\alpha_1}{\alpha_3} \right|}$$

IMD3: The third order inter modulation term

IP3: The metric third order intercept point. It is the point where the amplitude of third order inter modulation is equal to the that of fundamental.

$$A_{IP3} = \sqrt{\frac{4}{3} \left| \frac{\alpha_1}{\alpha_3} \right|}$$

IIP3: Input referred intercept point

OIP3: Output referred intercept point

$$P_{out} - IMD_3 = 2 \cdot (IIP_3 - P_{in})$$
MOS transistor

Intrinsic gate voltage and gm are the most important factors in RF CMOS.
Cutoff frequency: $f_T$

For higher $f_T$, increase $gm$ and decrease $Cin$.

$$f_T: \text{Frequency at which the current gain is unity.}$$

$$I_i = I_{io} \sin(\omega t) \quad \text{Input current}$$

$$V_i = \frac{I_{io}}{\omega C_{in}} \cos(\omega t) \quad \text{Gate voltage}$$

$$I_o = gmV_i = \frac{gmI_{io} \cos(\omega t)}{\omega C_{in}} \quad \text{Output current}$$

$$\therefore f_T = \frac{gm}{2\pi Cin} \quad \text{Proportional to gm} \quad \text{Inversely proportional to Cin}$$
Amplifier gain

For higher voltage gain, increase $g_m$, $f_T$, $r_o$ ($Q$), and decrease input and gate resistance.

For the larger gain

Fundamentally larger $g_m r_0$

Higher $f_T$ and lower $r_s$

$V_{eff}$ is difficult to reduce

$\Rightarrow$ Distortion and $C_{in}$ increase

\[ G \approx g_m r_0 \approx \frac{I_{ds}}{\frac{V_{eff}}{2}} \cdot r_o \]

Larger $I_{ds}$ or $r_o$

Larger $Q$

$\omega_0 = \frac{g_m r_o}{r_s C_{in}} = \omega_T \frac{r_0}{r_s}$

\[ \omega_s = \frac{1}{r_s C_{in}} \]

\[ \omega_T = \frac{g_m}{C_{in}} \]
Characteristics of gm (Basic)

Gm is proportional to the Ids and inversely proportional to the $V_{\text{eff}}$.

$V_{\text{eff}}$ is proportional to square root of $I_{\text{ds}}$ and inversely proportional to square root of $(W/L)$ ratio.

**Square law region**

\[
I_{\text{ds}} = \frac{\mu C_{\text{OX}}}{2n} \left( \frac{W}{L} \right) (V_{\text{gs}} - V_{T})^2 = \frac{\mu C_{\text{OX}}}{2n} \left( \frac{W}{L} \right) V_{\text{eff}}^2
\]

\[
gm = \frac{dI_{\text{ds}}}{dV_{\text{gs}}} = \frac{\mu C_{\text{OX}}}{n} \left( \frac{W}{L} \right) V_{\text{eff}}
\]

\[
gm = \sqrt{\frac{2\mu C_{\text{OX}}}{n} \left( \frac{W}{L} \right)} I_{\text{ds}}
\]

\[
V_{\text{eff}} \propto \sqrt{L \frac{I_{\text{ds}}}{W}} = \sqrt{L \cdot J_{\text{ds}}}
\]

$V_{\text{eff}}$ is proportional to square root of drain current density.

\[
gm = \frac{I_{\text{ds}}}{V_{\text{eff}}} \implies \frac{gm}{I_{\text{ds}}} = \frac{1}{\left( \frac{V_{\text{eff}}}{2} \right)}
\]
Non-ideal effects to square low region

At larger $V_{\text{eff}}$ and lower $V_{\text{eff}}$, two non-ideal effects are not negligible.

Low $V_{\text{eff}}$  Sub-threshold region

$$I_{ds} = I_{so} \exp \left( \frac{V_{gs}}{nU_T} \right)$$

$$g_m = \frac{I_{ds}}{nU_T}$$

(Weak inversion)

High $V_{\text{eff}}$  Mobility degradation

$$\mu \approx \frac{\mu_0}{1 + \theta V_{\text{eff}}}$$

$$\theta \approx \theta_0 + \frac{\mu_0}{v_c L}$$

This effect becomes larger at large $V_{\text{eff}}$ and short channel length.
Distortion

Lower \( V_{\text{eff}} \) gives higher gm, but results in higher distortion. To obtain lower distortion (higher IIP3), we must increase \( V_{\text{eff}} \).

Higher gm and lower distortion means higher \( I_{ds} \).

\[
I_{ds} = a_1 V_{\text{eff}} + a_2 V_{\text{eff}}^2 + a_3 V_{\text{eff}}^3 + \cdots
\]

\[
a_3 \equiv \frac{1}{6} \frac{d^3 I_{ds}}{d V_{\text{eff}}^3}
\]

\[
I_{IP3} = \sqrt{\frac{4}{3} \left| a_1 \right|}
\]
LC resonator can be regarded as resistance at the resonance frequency.

\[ \omega_0 = \frac{1}{\sqrt{LC}} \quad r_0 = Q \omega_0 L = \frac{Q}{\omega_0 C} \]
Substrate effect

Substrate should be treated as resistive network.

This substrate resistance causes RF power loss and noise generation.

Shielding can reduce this effect.
Power loss in substrate

Very low resistance or high resistance realizes low power loss.

\[ G_p = \frac{1}{R_p} \cdot \left( \frac{\omega}{\sigma_p} \right)^2 \]

\[ C_p = C \cdot \frac{1}{1 + \left( \frac{\omega}{\sigma_p} \right)^2} \]

\[ \sigma_p = \frac{1}{R_p C} \]

MOS: 10 Ω cm
GaAs: 1G Ω cm

Higher C and moderate \( R_{sub} \) results in higher power loss.
The cutoff frequency of MOS becomes higher than that of Bipolar. Over several GHz operations have attained in CMOS technology.
Effect of parasitic capacitance to $f_T$

$f_T$ of actual circuit is reduced by a parasitic capacitance.
There is an optimum gate width to obtain highest $f_T$.

\[ f_T \equiv \frac{gm}{2\pi (C_{gs} + C_{gd} + C_p)} \]

Region (1); Increased by increasing gm
Region (2); Decreased by increasing Cin

Region (1); Increased by increasing gm
Region (2); Decreased by increasing Cin
f_T: MOS vs. Bipolar

Even if f_T of MOS is the same as that of Bipolar, f_T of MOS is easily lowered by a parasitic capacitance. Because, gm of MOS is \( \frac{1}{2} \) to \( \frac{1}{4} \) of that of Bipolar at the same current. Small parasitic capacitance is a key for RF CMOS design.

MOS

\[
\begin{align*}
gm &= \frac{I_{ds}}{\left(\frac{V_{eff}}{2}\right)} \\
V_{eff, min} &= 2nU_T \\
V_{eff/2} &\approx 50\text{-}100\text{mV} \text{ (actual ckt.)}
\end{align*}
\]

Bipolar

\[
\begin{align*}
f_T &= \frac{gm}{2\pi C_{in}} \\
gm &= \frac{I_c}{U_T} \\
U_T &= \frac{kT}{q} \approx 26mV \\
\text{(Same operating current)}
\end{align*}
\]

\[
\begin{align*}
gm_{CMOS} &< \frac{1}{2}, \frac{1}{4}gm_{Bip} \\
C_{in, CMOS} &< \frac{1}{2}, \frac{1}{4}C_{in, Bip} \\
\text{(Same f_T)}
\end{align*}
\]
$\Delta V_T$ mismatch degrades accuracy; ADC, OP amp, and Mixer. Larger gate area is needed for small $V_T$ mismatch. Scaling and proper channel structure improves mismatch.

\[ \Delta V_T \propto \frac{T_{ox}}{\sqrt{LW}} \]

*Larger gate area*

0.4um Nch

Tox Scaling

0.13um Nch Boron w. Halo*

0.4um Pch

Channel engineering

0.13um Nch In w/o Halo*

* Morifuji, et al., IEDM 2000.*
$\Delta V_T = \frac{\Delta Q_{\text{depl}}}{C_{\text{ox}}} = A t_{\text{ox}} \frac{\sqrt{L W d_{\text{depl}} N_A}}{L W} = A' t_{\text{ox}} \frac{4 \sqrt{N_A}}{\sqrt{L W}} \approx A_{VT} \frac{t_{\text{ox}}}{\sqrt{L W}}$

$\therefore d_{\text{depl}} \propto \frac{1}{\sqrt{N_A}}$

$A_{VT} = 1V$

$L = W = 0.25 \mu m, \quad t_{\text{ox}} = 5nm$

$\Delta V_T = 20mV$

1/f noise

1/f noise of MOS is larger than that of bipolar. For the lower 1/f noise, the larger gate area is needed.

\[ V_{nf}^2 = \frac{S_v f}{L W} \frac{\Delta f}{f}, \quad S_v \propto T_{ox}^2 \]

Nch/Pch 0.4\,\mu m

Nch 0.4\,\mu m/1.0\,\mu m

\( W/L=800/0.4 \), \( Vdd=3\,V \), \( I_d=1\,mA \)
The lower $R_{nv}$ and $G_{ni}$ realizes the better for a lower noise figure.

\[ Z_s = R_s + jX_s \]

\[ V_{ng}^2 = 4kTR_{nv}, \quad I_{ng}^2 = 4kTG_{ni} \]

\[ F = \frac{V_{n,rs}^2 + (V_{ng} + Z_sI_{ng})^2}{V_{n,rs}^2} = 1 + \frac{R_{nv}}{R_s} + \frac{|Z_s|^2 G_{ni}}{R_s} \approx 1 + \frac{R_{nv}}{R_s} + R_sG_{ni} \]

\[ R_{sopt} = \frac{V_{ng}}{I_{ng}} = \sqrt{\frac{R_{nv}}{G_{ni}}} \]

\[ F_{\min} \approx 1 + 2\sqrt{R_{nv}G_{ni}} \]
Noise figure: MOS transistor

\[ F \approx 1 + \frac{R_{nv}}{R_s} + R_s G_{ni} \]

\[ R_{nv} = R_g + R_{gs} \quad R_g = R_{sr} \frac{W_{tot}}{L} \frac{1}{3N^2} \quad R_{gs} \approx \frac{1}{5gm} \quad G_{ni} \approx \frac{gm}{5} \left( \frac{\omega_0}{\omega_T} \right)^2 \]

\[ F \approx 1 + \frac{1}{R_s 5gm} + R_s \frac{gm}{5} \left( \frac{\omega_0}{\omega_T} \right)^2 \]

\[ R_{s\text{opt}} \approx \frac{1}{gm} \left( \frac{\omega_T}{\omega_0} \right) = \frac{1}{C_{gs} \omega_0} \]

\[ F_{\text{min}} \approx 1 + 2 \frac{\omega_0}{\omega_T} \]
Low noise amplifier design

Narrowband LNA uses inductor degeneration for impedance matching.

Impedance matching

\[ Z_{in} \approx s(L_s + L_g) + \frac{1}{sC_{gs}} + \left( \frac{g_m}{C_{gs}} \right) L_s \approx \omega_T L_s \]

\[ \omega_0 = \frac{1}{\sqrt{C_{gs}(L_s + L_g)}} \]
Low NF design

\[ F \approx 1 + \frac{r_{gs} + r_g}{Z_0} + 4\gamma gmZ_0 \left( \frac{\omega_0}{\omega_r} \right)^2 \approx 1 + \frac{r_{gs} + r_g}{Z_0} \]

Low noise figure

1) Lower the gate resistance

Dived the gate, or lower the gate sheet resistance

2) Reduce substrate loss

Reduce parasitic capacitance

Use shield technique to the input bonding PAD.

Use high resistive substrate, if possible.

3) Increase drain current

\[ r_{gs} \approx \frac{1}{5gm} \approx \frac{V_{eff}}{10I_{ds}} \]

4) Increase \(Z_0\), if possible.
Id_s and V_eff optimization

Adjust the Id_s and V_eff for optimization of gain, noise and distortion. Dynamic range of LNA is proportional to Id_s.

\[ DR_{LNA} \propto \frac{IIP^3_{LNA}}{F - 1} \propto gmZ_0V_{eff} \approx I_{ds}Z_0 \quad IIP^3 \propto V_{eff} \]

\[ V_{eff} \propto \sqrt[3]{\frac{I_{ds}}{W}} \]

![Graph showing dynamic range, noise figure, gain, and 3rd distortion against V_eff and Id_s. Increase in Id_s is indicated with dotted line, decrease with solid line. Each curve shows the relationship at different levels of V_eff.]
NF progress in MOS LNA

NF of MOS LNA is reaching 1dB.
Mixer

Mixer converts frequency, but image signal is converted to the same frequency.

\[ V_s = A_s \cos(\omega_s t) \]

\[ V_o = \frac{2}{\pi} A_s \cos((\omega_s \pm \omega_{LO})t) \]

If \( V_{LO} \gg 4V_{eff} \) (Full swing)

\[ V_{LO} = A_{LO} \cos(\omega_{LO}t) \]

RF spectrum

IF spectrum

dB

Freq

\( F_{LO} \)

\( F_{image} \)

\( F_{des} \)

\( F_{IF} \)

\( F_{IF} \)

Freq
Image-reject mixers

The quadrature mixing realizes image-suppression. Gain and phase matching is needed.

\[ V_{\text{in}}(t) = A_{\text{des}} \cos(\omega_{\text{det}}) + A_{\text{im}} \cos(\omega_{\text{im}}t) \]

\[ V_{\text{out}}(t) = A_{\text{des}}A_{c} \cos(\omega_{\text{IF}}t) + A_{\text{im}}A_{c}I_{R} \cos(\omega_{\text{IF}}t) \]

\( A_{c} \): Conversion gain, \( I_{R} \): Image rejection

\( I_{R} = 0 \) if I/Q phase difference is 90° and Channel conversion gains are equal.
Gain mismatch and phase error

\[ \frac{P_{spur}}{P_{desired}} = \frac{1 + \gamma^2 - 2\gamma \cos \phi}{1 + \gamma^2 + 2\gamma \cos \phi} \]

\[ \gamma : \text{Gain ratio} \]

\[ \phi : \text{Phase error} \]

Passive FET mixer

MOS can realize a passive mixer easily.

Ultimately low power, but take care of isolation.

Low power
High linearity
No 1/F noise

No conversion gain
No isolation, Bi-directional
Active mixers

Single balanced mixer

Double balanced mixer

Very small direct feed through and even order distortion
Active mixer design

The larger $I_{ds}$ is needed for high dynamic range and shorter switching time for low 1/f noise.

Mixer gain

$$G_{mix} = \frac{2}{\pi} g_m Z_L, \text{ or } = \frac{2}{\pi} \frac{Z_L}{Z_S}$$

when $Z_S$ is used

Thermal noise

$$v_{on}^2 = 8kT R_L \left( 1 + \frac{2\gamma R_L}{\pi A_{LO}} + \gamma g_m R_L \right) \approx 8kT R_L^2 \gamma g_m$$

$$SSBv_{in}^2 = \left( \frac{2}{\pi} g_m R_L \right)^2 \approx 2\pi^2 kT \gamma \frac{\gamma}{g_m} \pi^2 kT \gamma \frac{V_{eff}}{I_{ds}}$$

A larger dynamic range needs larger current

1/F noise

1) Switch transistor (M2, M3)

$$\nu_{n, o} = \frac{4T_S}{T_{LO}} \nu_{n, sw}$$

$$\nu_{n, sw}^2 \approx \frac{1}{wL} \propto \frac{1}{C_{gs}}$$

Shorter switching time or larger $T_s/T_{LO}$ ratio

2) Load transistors

Directly produces

Phase modulation

R_L: Resistive component in ZL

Ts: 1/F noise
There is an optimum $I_{ds}$ for low phase noise.

1) Amplitude condition

\[ V_{osc} = \frac{4I_{ro}}{\pi} \]

Headroom limit

\[ I_{opt} = \frac{\pi V_{dd}}{2r_o} = \frac{\pi V_{dd} \omega_0 C}{Q} \]

2) Oscillation condition

\[ gm_{2,3} > \frac{2}{r_o} \quad I > \frac{\omega_0 CV_{eff,2,3}}{Q} \]
Phase noise of oscillator

Phase-frequency relation and resonator characteristics determine phase noise.

\[
\frac{1}{B_W} = \frac{2Q_L}{\omega_0}
\]

\[
v(t) = A \cos[\omega_0 t + \phi(t)]
\]

\[
\omega_m = \frac{d\phi}{dt} = j \omega \phi
\]

\[
S_\omega(\omega_m) = \omega_m^2 S_\phi(\omega_m)
\]

\[
\Delta \theta = \frac{\omega_m}{B_W} = \frac{2Q_L}{\omega_0} \omega_m
\]

\[
S_\phi(\omega_m) = \left(\frac{\omega_0}{2Q_L}\right)^2 S_{\Delta \theta}(\omega_m) \quad \omega_m < B_W
\]

\[
S_{\Delta \theta}(\omega_m) = \left(\frac{\omega_0}{2Q_L}\right)^2 \frac{1}{\omega_m^2} S_{\Delta \theta}(\omega_m) = \left(\frac{\omega_0}{2Q_L \omega_m}\right)^2 S_{\Delta \theta}(\omega_m)
\]
Phase noise of oscillator

\[ Z(\omega_0 + \omega_m) \approx j \frac{\omega_0 L}{\omega_m} \quad \omega_m << \omega_0 \]

(Filter action)

\[ Q = \frac{r_0}{\omega_0 L} \]

\[ |Z(\omega_0 + \omega_m)| \approx \frac{r_0 \omega_0}{2Q \omega_m} \]

\[ \frac{v_n^2}{\Delta f} = \frac{i_n^2}{\Delta f} \cdot |Z|^2 = 4kT r_0 \left( \frac{\omega_0}{2Q \omega_m} \right)^2 \]

Noise spectrum density

\[ L\{\omega_m\} = 10 \log \left[ \frac{2kT}{P_{\text{sig}}} \cdot \left( \frac{\omega_0}{2Q \omega_m} \right)^2 \right] \]

Phase noise
Frequency characteristics of Phase noise in oscillator

1/f noise and thermal noise is converted to 1/f^3 and 1/f^2, respectively.

\[
S_{\phi}(\omega_m) = \left( \frac{1}{2Q_L} \right)^2 \frac{2FkT}{P_S} \frac{1}{\omega_m^2}
\]

where \( \omega_m \) is the angular frequency, \( P_S \) is the input power, \( FkT \) is the thermal noise power, and \( 1/Q_L \) is the load quality factor.

The phase noise spectrum shows two slopes:
- -9dB/oct (Slope = -3)
- -6dB/oct (Slope = -2)

The figure illustrates the conversion of 1/f noise and thermal noise to 1/f^3 and 1/f^2, respectively, with specific equations and graphical representations.
Up and down converted noise

Noises around $N \times f_0$ are up and down converted to $f_0$. 

$$V_{noise} \left( V / \sqrt{Hz} \right)$$

$V_{noise}$ is shown as a function of frequency $\omega$. The diagram illustrates noise shaping with peaks at $\omega_0$, $2\omega_0$, and $3\omega_0$. The power $P$ is given in dBm.
FoM and minimum phase noise

FoM is basically proportional to $Q^2$.

$$FoM = \left( \frac{f_0}{f_m} \right)^2 \frac{1}{L(f_m)V_{dd}I}$$

$F_m$: Offset frequency

$L(f_m)$: Phase noise at offset freq.

$$L(f_m) = \frac{1}{2} \cdot \frac{1}{Q^2} \cdot \left( \frac{f_o}{f_m} \right)^2 \cdot \frac{FkT}{P_{RF}} = \frac{1}{2} \cdot \frac{1}{Q^2} \cdot \left( \frac{f_o}{f_m} \right)^2 \cdot \frac{FkT}{\left( \frac{V_o^2}{2r_o} \right)}$$

$F$: Noise factor

$$F = 2 + \frac{8\gamma r_o I}{\pi V_o} + \gamma \frac{8}{9} r_o \cdot g_{m1}$$

$I_{opt} = \frac{\pi V_{dd}}{2r_o} = \frac{\pi V_{dd} \omega_o C}{Q} = \frac{\pi V_{dd}}{2Q \omega_o L_{ind}}$

$$FoM = \frac{4Q^2}{\pi kT} \frac{1}{2 + 4\gamma + \frac{32}{9} \gamma \frac{V_{dd}}{V_{eff,1}}} \propto Q^2$$

at $I_{opt}$
Oscillator design

Careful optimization reduces the oscillator phase noise.

\[ L_{\text{min}}(f_m) = kT \cdot \frac{\gamma}{V_{dd}} \cdot \frac{\omega_0 L_{\text{ind}}}{2Q} \left( \frac{1}{V_{dd}} + \frac{2}{V_{\text{eff},1}} \right) \left( \frac{f_o}{f_m} \right)^2 \]

\[ L_{\text{min}}(f_m) = kT \cdot \frac{\gamma}{2I_{\text{opt}}} \cdot \frac{1}{2Q^2} \left( \frac{1}{V_{dd}} + \frac{2}{V_{\text{eff},1}} \right) \left( \frac{f_o}{f_m} \right)^2 \]

\[ I_{\text{opt}} = \frac{\pi V_{dd}}{2r_o} = \frac{\pi V_{dd} \omega_0 C}{Q} = \frac{\pi V_{dd}}{2Q \omega_0 L_{\text{ind}}} \]

**Larger** \( V_{dd} \)

**Large** \( V_{\text{eff},1} \), but take care of \( V_o \) reduction

**Large** \( L_1, W_1 \) to reduce 1/f noise

**Enough** \( W/L \) for \( M2, M3 \)

**Higher** \( Q \)

**Larger** \( QL_{\text{ind}} \) for Lower \( I_{\text{opt}} \)
CMOS oscillator circuits

(a) Basic

(b) Low power (gm is higher)

(c) Low noise by filtering

E. Hegazi, ISSCC 2001

CMOS oscillator circuits

Basic
Low power (gm is higher)
Low noise by filtering

E. Hegazi, ISSCC 2001
Filtering of $2f_0$ component in OSC.

Noise filtering of $2f_0$ component reduces the OSC phase noise to -10dB.

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Oscillator phase noise progress

Phase noise in CMOS oscillator becomes lower than that of bipolar.

![Graph showing phase noise progress over years for CMOS, Si-bipolar/BiCMOS, and SiGe-BiCMOS technologies.](image-url)
Acknowledgment and references

• Acknowledgment

I would like to thank Prof. Asad Abidi in UCLA for his advices.

• References