Mixed signal SoC:
A new technology driver in LSI industry

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• Current electronics and mixed signal technology
• CMOS as an analog device
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• Summary
Current electronics and mixed signal technology
Image of current electronics

Digital consumer electronics and networking drive current electronics.

- DAB
- CS/BS
- ITS
- ADSL, FTTH
- Network
- IEEE 1394, USB, Blue tooth, Wireless LAN
- Ethenet
- Home network
- HII Station
- Digital TV
- DVC
- DVD
Mixed signal technology enables high speed digital networking.

Data conversion
Data and clock recovery
Equalization
Noise cancellation
Encryption
Error correction

Analog circuit
Digital circuit
Digital storage also needs high speed mixed signal technologies.
Mixed signal SoC for DVD RAM system

This enables high readability for weak signal from DVD RAM pickup.

World fastest and highly integrated mixed signal CMOS SoC

Goto, et al., ISSCC 2001
Recent developed mixed signal CMOS LSIs

5G RF LAN
- 12b 50MHz ADC 2ch
- 12b 50MHz DAC 2ch

AFE for ADLS
- 12b 20MHz ADC+DAC

Digital network
- 1394b (1GHz)

AFE (Analog Front End)
- AFE for Digital Camera
  - 12b 20MHz ADC+AGC

2GHz RF CMOS
Application area in mixed signal CMOS tech.

Almost all the products need mixed signal CMOS LSI tech.

- **Wireless**
  - Cellular phone: PDC, W-CDMA
  - RR-Net: Bluetooth, IEEE802.11
  - Broadcast: STB, DTV, DAB
  - Optical: FTTH, OC-xx
  - Metal: ADSL, VDSL, Power line modem
    - Serial: IEEE1394, USB, Ethernet
    - Parallel: DVI, LVDS

- **Wired**
  - DVD, VDC, HDD
  - LCD, PDP, EL, Audio drive
  - Camera, Others
  - Switching supply, Every LSIs (On-chip)
Digital technology in real world

Digital signal suffers heavy damage in real world.
But, digital can address this issue by own advantages,
but needs the help of analog tech.

Advantages of Digital Tech.

• High robustness
• Programmability
• Time shift (memory)
• Error correction
• High Scalability

Mixed signal technology
(Analog+Digital)

Not only digital, but also analog;
ADC, DAC, Filter, and PLL are needed

Pure digital

Noise
Distortion
Interference
Limited bandwidth

Real world

Damaged
digital

Reconstruction

Recovered digital
Progress in A/D converter; video-rate 10b ADC

ADC is a key for mixed signal technology.
We have reduced the cost and power of ADC drastically;
1/2,000 for Power and 1/200,000 for the cost!
CMOS technology attained it. dulling past 20 years

<table>
<thead>
<tr>
<th>Year</th>
<th>Technology</th>
<th>Power (W)</th>
<th>Cost ($K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1980</td>
<td>Conventional</td>
<td>20</td>
<td>8,000</td>
</tr>
<tr>
<td>1982</td>
<td>World 1st Monolithic Bipolar (3um)</td>
<td>2</td>
<td>800</td>
</tr>
<tr>
<td>1993</td>
<td>World lowest power CMOS (1.2um)</td>
<td>30</td>
<td>2.00</td>
</tr>
<tr>
<td>Now</td>
<td>SoC Core CMOS (0.15um)</td>
<td>10</td>
<td>0.04</td>
</tr>
</tbody>
</table>

Analog Devices Inc.

Our developed. Our developed. Our developed.
Progress in high-speed ADC

High speed ADC has reduced its power and area down to be embedded.

**World fastest 6b ADC**

6b, 1GHz ADC
2W,
1.5um Bipolar

ISSCC 1991

**World fastest CMOS ADC**

6b, 800MHz ADC
400mW, 2mm²
0.25umCMOS

ISSCC 2000

**World lowest Pd HS ADC**

7b, 400MHz ADC
50mW, 0.3mm²
0.18umCMOS

ISSCC 2002

Reported Pd of CMOS ADCs

Conversion rate [x100Msps]

10mW/Gsps

1mW/Gsps

1 order down

This Work

ISCAS A. Matsuzawa
Early stage mixed signal CMOS LSI for CE

Success of CMOS ADC and DAC enabled low cost mixed signal CMOS LSI. This also enabled low cost and low power digital portable AV products.

1993 Model: Portable VCR with digital image stabilizing

System block diagram
CMOS as analog device
# CMOS as analog device

CMOS has many issues as analog device, but also has a variety of circuit techniques.

<table>
<thead>
<tr>
<th></th>
<th>CMOS</th>
<th>Bipolar</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch action</td>
<td>++</td>
<td>--</td>
<td>Only CMOS can realize switched capacitor circuits</td>
</tr>
<tr>
<td>Low Input current</td>
<td>++</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>High gm</td>
<td>-</td>
<td>+</td>
<td>CMOS is $\frac{1}{4}$ of Bip.</td>
</tr>
<tr>
<td>Low Capacitance</td>
<td>+</td>
<td>-</td>
<td>This results in $C_p$ issue</td>
</tr>
<tr>
<td>$f_T$</td>
<td>+</td>
<td>+</td>
<td>Almost same</td>
</tr>
<tr>
<td>Voltage mismatch</td>
<td>--</td>
<td>++</td>
<td>CMOS is 10x of Bip.</td>
</tr>
<tr>
<td>1/f noise</td>
<td>--</td>
<td>++</td>
<td>CMOS is 10x to 100x of Bip.</td>
</tr>
<tr>
<td>Low Sub. effect</td>
<td>-</td>
<td>+</td>
<td></td>
</tr>
<tr>
<td>Offset cancel</td>
<td>++</td>
<td>--</td>
<td>CMOS has a variety of techniques to address the self issues</td>
</tr>
<tr>
<td>Analog calibration</td>
<td>++</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>Digital calibration</td>
<td>++</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>Embed in CMOS</td>
<td>++</td>
<td>--</td>
<td></td>
</tr>
</tbody>
</table>
GHz operation by CMOS

Cutoff frequency of MOS becomes higher than that of Bipolar. Over several GHz operations have attained in CMOS technology.

\[ f_T \equiv \frac{g_m}{2\pi C_{in}} \]

\[ f_{Tpeak} \approx \frac{v_{sat}}{2\pi L_{eff}} \]
CMOS technology for over GHz networking

Digital consumer needs over GHz wire line networking. CMOS has attained 5Gbps data transfer.

World first 1394b transceiver
For 1Gbps networking

Test chip for 5Gbps wire line

0.25μm 3AL_CMOS

0.18μm 4AL_CMOS

5Gbps Eye pattern
Even if $f_T$ of MOS is same as that of Bipolar, $f_T$ of MOS is easily lowered by parasitic capacitance. Because, $gm$ of MOS is $\frac{1}{2}$ to $\frac{1}{4}$ of that of Bipolar at the same current.

**MOS**

$$gm \equiv \frac{Ids}{\left(\frac{V_{eff}}{2}\right)}$$

$$V_{eff\ min} = 2nU_T \quad n: 1.4$$

**Bipolar**

$$f_T \equiv \frac{gm}{2\pi Cin}$$

$$gm \equiv \frac{Ic}{U_T}$$

$$U_T \equiv \frac{kT}{q} \approx 26mV$$

**Veff/2: 50-100mV**  
(actual ckt.)

$$gm_{CMOS} < \frac{1}{2}, \frac{1}{4} gm_{Bip}$$

$$Cin_{CMOS} < \frac{1}{2}, \frac{1}{4} Cin_{Bip}$$

(Same operating current)

(Same $f_T$)
Parasitic effect: CMOS CT filter

High frequency ckt. with scaled device is strongly affected from parasitic. Circuit optimization with layout and parasitic effect is needed.

SIM w/o parasitic C

SIM with parasitic C

Optimized with parasitic C
Transistor issue: $V_T$ mismatch

Larger gate area is needed for small $V_T$ mismatch. Scaling and proper channel structure can improve this.

$$\Delta V_T \propto \frac{T_{ox}}{\sqrt{LW}}$$

Development strategy and design system for mixed signal SoC
Full DVD system integration in 0.13um tech.

Advanced mixed signal SoC has been successfully developed.

Okamoto, et al., ISSCC 2003

0.13um, Cu 6Layer, 24MTr

0.13um, Cu 6Layer, 24MTr
Current electrical system is complicated and needs analog and memory.
Scaled CMOS technology

Current Scaled CMOS technology is very artistic.

Matsushita’s 0.13um CMOS technology

Transistor

100nm

Cu Interconnection

Gate

SiO₂

Si

Seven lattices

Cu Interconnect

MOS Tr

W plug

W plug
Development strategy and system

Product time slot is narrow and development cost is huge.

Conventional analog LSI needs 2 or 3 re-designs. This can not be accepted to mixed signal SoC

Advanced development strategy and design system must be established.
Strategy for the mixed signal SoC

• System design
  – Digital calibration for analog adjustment and unknown parameters.
  – System optimization to reduce analog area and increase robustness.

• System verification
  – Fast and accurate mixed signal system simulator with behavioral model to verify and optimize the mixed signal system.
  – Create the target performance for circuit blocks.

• Circuit design
  – Ultra fast and accurate circuit simulation for P.V.T and fluctuation analysis to verify the performance and robustness.
  – Circuit optimizer to find the sweet spot of the circuit.
  – Automated creation of analog behavioral model for system sim.

• Process and device development
  – Develop suitable analog option device
  – Early analog parameter extraction (mismatch, temp. and voltage chara.)
  – Monitor and control the analog parameters in Fab.
Design flow for mixed signal SoC

Design flow from System to layout with top down and bottom up process should be used for designing mixed signal SoC. Accurate and a variety of device parameters is an another key.
Multi-language simulation

Multi-language simulation is 56x faster than SPICE with same accuracy. This will contribute to shorter design TAT and higher design quality.

<table>
<thead>
<tr>
<th>Description</th>
<th>Option</th>
<th>Time</th>
<th>CPU Time (s)</th>
<th>Speed Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL Behavioral Lev (Verilog-A+SPICE)</td>
<td></td>
<td>9 min</td>
<td>545</td>
<td>56</td>
</tr>
<tr>
<td>PLL Circuit Level (Spice)</td>
<td>Model Opt.</td>
<td>2 hr</td>
<td>7939</td>
<td>3.8</td>
</tr>
<tr>
<td>PLL Circuit Level (Spice)</td>
<td></td>
<td>8 hr</td>
<td>30414</td>
<td>1</td>
</tr>
</tbody>
</table>

Red line: SPICE  
Blue line: Verilog-A
Mixed signal system design

Needs mixed signal Simulation for total signal processing. Many parameters and processing methods should be optimized.

Finally, system is checked by real disc signals.
System simulation

Perfection of the mixed signal system should be verified and optimized by system simulation.

ADC resolution effect

![Graph showing BER vs SNR for different ADC resolutions (4b, 5b, 6b, 7b). The graph illustrates the improvement in BER with increasing SNR for each resolution, indicating the impact of ADC resolution on system performance.](image)

- RLL (2, 10) recorded data
- PR(3,4,4,3) waveform
- Viterbi decoded result
- System verification
LSI design using behavioral language

Example: Analog Front End chip for ADSL system.
Hierarchical and behavioral system design

System should be described in behavioral language, hierarchically.
Virtual System test using Verilog AMS and Matlab

We can test the designed mixed signal system virtually, by using Verilog AMS and Matlab.

Matlab is used as a soft DSP

Matlab
DMT modulation

Constitution ENC
IFFT
FIR

Target LSI
Verilog-AMS

Matlab
DMT demodulation

FIR
FFT
Constellation DEC

MTPR TEST (DMT Carrier hole)

> 66dB

QAM constellation

ISCAS A. Matsuzawa 33
Fitting between behavioral and Spice

The combination of Verilog AMS and SPICE assures system perfection.
Unified mixed signal circuit simulator

New design system can increase design speed, 10x to 50x.

System level Specification Optimization Simulation Results Design flow controller

Verilog-AMS +SPICE

Documentation
Test bench
PVT analysis
Spec sheet
Behavioral model
Optimization
Simulation flow
Controller for automated simulation

Simulation controller enables fast and automated simulation steps
Issues of mixed signal SoC
\[ V_{dd} \text{ and CMOS scaling limits in analog} \]

Lowest analog operating voltage must be 1.2V - 1.8V. Thus 0.18um – 0.13um must be a scaling limit for analog. This results in salutation of \( f_T \) and area reduction.
Optimization in channel parameters

Larger gate length is needed for small mismatch and small noise circuit. However, this results in increase of cost and decrease of performance.
Cost up issue by analog & I/O

Cost of mixed A/D LSI will increase when using deep sub-micron device, due to the increase of cost of non-scalable analog and I/O parts.

Large analog on SoC must be unacceptable in near future.

Wafer cost increases 1.3x for one generation

Chip area

Chip cost
Solution 1: Scaled CMOS and use of digital

Use scaled CMOS and not accurate passives. Address the issues by M/S compensation and system optimization.

<table>
<thead>
<tr>
<th>0.35um Tr</th>
<th>0.18um_0.13um Tr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Accurate passive</td>
<td>Not accurate passive</td>
</tr>
</tbody>
</table>

(Solution)

- Analog compensation
- Digital calibration
- System optimization

Pros
- Small area (low cost)
- High speed
- Low power

Cons
- Low accuracy
- Sensitive to Process
- Large 1/f noise

(If low Vdd is acceptable)
Example: Analog+ digital calibration tech.

Area and power are reduced drastically, by scaled CMOS and digital tech.

Y. Cong and R. L. Geiger, Iowa state university, ISSCC 2003

14b 100MS/s DAC

1.5V, 17mW, 0.1mm², 0.13um

0.5 LSB INL,

SFDR=82dB at 0.9MHz, 62dB at 42.5MHz

Area: 1/50

Pd: 1/20
Solution 2: Advanced packaging technology

Some advanced packaging technologies will give the solution.

Analog: using not so much scaled technology.
Digital: using scaled technology
Connect with low parasitic cap. and inductance.

Chip On Chip technology
Same capacitance as on-chip interconnection. No interconnection inductance.
Future step: Mixed signal egg.

Analog helps digital (digital network and storage...). Next step is digital must help analog.

Mixed signal egg (Analog yolk and white with digital shell)

Digital shell

Sustain the analog egg. Calibration and adjustment.

Analog yolk and white

Ultra-low power signal processing (Weak inversion)
Ultra-high speed signal processing

But, very delicate and fancy
Summary

• The mixed signal (Analog+Digital) is essential for almost all the systems. Not analog only, not digital only.

• Effective modeling of analog parts and high speed concurrent simulation with digital is vital for design.

• CMOS is very powerful technology for analog, as well as digital, but scaling limitation is reaching.

• The collaboration between analog and digital, and advanced packaging technology will bring us effective solutions.