Driving the SoC development for digital consumer electronics

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Digital consumer electronics and SoC
Exciting Multimedia world with SoC!

The new consumer electronics era has been emerged. The key technologies are digital multimedia and System on a Chip.
One chip SoC realizes almost whole electric systems

0.13um CMOS, 6Cu
3.5M Trs.
CLK: 400MHz

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SD Memory card
Impact of digital tech. on consumer business

LSI = System !, technically and in business

Analog base

Digital base

Cost occupation (%)

WideTV

Internet TV

Digital TV

PC

Semiconductor

Components

Labor cost

Software & patent

Almost same as PC

Analog base

Digital base


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New semiconductor business scheme

SoC will reform the semiconductor business scheme from vertical to horizontal.

Conventional semiconductor maker  (semiconductor technology base)

System

CPU Maker  DRAM Maker  ASIC Maker  Analog Maker

PC

CPU  DRAM  Logic (ASIC)  Network Analog

DVD

CPU  DRAM  Logic (ASIC)  Network Analog

DTV

CPU  DRAM  Logic (ASIC)  Network Analog


Future semiconductor maker (System base)

Not appeared yet

SoC will reform the semiconductor business scheme from vertical to horizontal.
Architecture design
The architecture optimization based on a system analysis is a key.
System analysis 1: External bus

Bus occupation increases at AV replay

Conventional PC bus can’t be used

New bus architecture is needed

Occupation of external bus (%)

PC type data

AV type data

at AV replay

EPG process (non AV replay)

Receive data fetch

Occupation of external bus (%)

Stream

Prog. Exe

TSDec.

Peripheral ASIC

AV Dec.

DRAM

SDRAM

OSD drawing

Flash

DRAM

MCU


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System analysis 2: Internal bus

Instruction execution is only 1/4

Many conflicts between data and instructions
Solution: Crossbar switch

Bus-master can access to bus slave in each, independently
Performance improvement

Equivalent performance (MIPS)

- Conventional
  - AV Decode
  - SI information
  - Graphics
  - 15 MIPS (64MHz)

- SoC for digital TV
  - AV Decode
  - SI information
  - Graphics
  - 50 MIPS (121.5MHz)

System performance efficiency
- Conventional: 24%
- SoC for digital TV: 41%

Improvement methods:
- By frequency increase
- By crossbar switch
- Basic STB processing
The MPEG4 technology are going to be used not only for a cellular phone, but also for internet and consumer electronics.
MPEG4 Codec and decoder

MPEG4 Codec

- 0.18um e-DRAM
- 31M Tr
- 90 mW@54MHz

15fps (Core@L1 decode)
30 fps (Simple@L3 decode)

MPEG4 Decoder

- 0.18um CMOS
- 11M Tr
- 11 mW@27/54MHz

15fps (Core@L1 decode)
DSP with Vector Pipeline and dedicated HW engines enables high throughput and low power video processing.

1.5 GOPS: Simple@L1
12 GOPS: Simple@L3
6 GOPS: Core@L1
Performance of core decoding

Hardware engines increase the performance 4 times higher

- **CAD**: 6.1%
- **PAD**: 26.5%
- **COMP**: 6.8%
- **Texture Decoding**: 63%
- **Core@L1 Decoding**: WITH the Engines 24%

Mcycles: 0-200
Kcycles: 0-40

Clock gating

The sophisticated clock gating is very effective to reduce the power consumption.

Example 1: MPEG4 Codec

Example 2: MPEG4 Decoder
Mixed signal technology
Mixed signal technology

The mixed signal is vital to current SoC for the consumer and networking. However, conventional analog needs 2 or 3 redesigns!

How to develop it without re-design!

Mixed signal can decrease bit-error rate and can increase stability in DVD recorder systems.
Mixed signal SoC for DVD systems

The SoC integrates analog FE, font-end, and back-end in 0.13um tech.

ISSCC 2003, K Okamoto et., al.  24M Tr
Strategy for the mixed signal SoC

• System design
  – Digital calibration for analog adjustment and unknown parameters.
  – System optimization to reduce analog area and increase robustness.
• System verification
  – Fast and accurate mixed signal system simulator with behavioral model to verify and optimize the mixed signal system.
  – Create the target performance for circuit blocks.
• Circuit design
  – Ultra fast and accurate circuit simulation for P.V.T and fluctuation analysis to verify the performance and robustness.
  – Circuit optimizer to find the sweet spot of the circuit.
  – Automated creation of analog behavioral model for system simulation.
• Process and device development
  – Develop suitable analog option device
  – Early analog parameter extraction (mismatch, temp. and voltage chara.)
  – Monitor and control the analog parameters in Fab.
Design flow for mixed signal SoC

The design flow from a system to a layout with top down and bottom up process should be used for designing the mixed signal SoC. The accurate and a variety of device parameters is an another key.
Hierarchical and behavioral system design

This system should be described in behavioral language, hierarchically.
Virtual System test using verilog AMS and Matlab

We can simulate the performance of mixed signal system, using Verilog AMS and Matlab.

Matlab is used as a soft DSP

QAM constellation

> 66dB

Matlab
DMT modulation

Constellation ENC
IFFT
FIR

Virtual LSI
w/ Verilog-AMS

Matlab
DMT demodulation

FIR
FFT
Constellation DEC

MTPR TEST (DMT Carrier hole)

Q
I
f

Controller for automated simulation

Simulation controller enables fast and automated simulation steps
Global development management
SoC needs several technology layers from system and software to device.
Narrow development time slot

The development time slot is very narrow. So “Just in time” develop is required.
Scaled CMOS

Current Scaled Si technology is very artistic.
How to control it and how to increase the production yield quickly!

Matsushita’s 0.13um CMOS

Transistor

Interconnection

Gate
SiO₂
Si

100nm

Seven lattices

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Choice of transistor

A variety of transistors has increased.
Choose the proper transistor depending on the systems

Operating Voltage (V)

Delay time (Arbitrary)

- Low leak (3pA/um)
- Middle leak (1nA/um)
- Constant VT
- Scaled VT

Operating Voltage:
- 1V
- 1.2V
- 1.5V
- 1.8V
- 2.5V
- 3V
- 5V

Design rule (um):
- 0.1
- 0.2
- 0.3
- 0.5
- 1.0

A variety of transistors has increased.
Choose the proper transistor depending on the systems
System target driven development

System target driven can reduce unconformities and shorten the TAT.


Conventional

Unconformity Spec. Cost and Time

Advanced

Collaboration to solve boundary problems

Shorten dev. TAT
Bidirectional design flow; feed forward flow, as well as feedback flow can pass early targets to different groups. This shorten the TAT and reduce the conflicts.

Feed back (Conventional)
- Speed
- Delay

Verification Flow
- Cell Lib.
- Device
- Process
- Product

Feed forward (Advanced)
- System
- SoC Design

Target flow
Making roadmap makes a good communication and a corroboration between different groups.

**Future issues and tradeoffs**

**Future demand**

**Making roadmap and meetings**

- **Cell Lib.**
  - Cell height
  - HP Analog
  - HP I/O

- **Device**
  - Reliability
  - High Idd
  - Low Ioff

- **Process**
  - Low-k
  - Cu
  - STI
  - Analog

- **Fab**
  - High yield
  - Quick ramp-up
  - Analog control

- **Package**
  - POE
  - Low inductance

- **Test**
  - Iddq test
  - Wafer burn-in

- **System**
  - Mixed signal
  - Clocking
  - Power routing
  - Large system’s verification

- **EDA**
  - EMI sim
  - Cross-talk sim
  - Mixed signal sim

- **Making roadmap**

- **Solutions**

Summary

- Digital consumer electronics based on multimedia technology has emerged and become big market.

- SoC also has become a dominant along with this technology.

- Architecture of SoC should be optimized for the application system.

- The mixed signal technology is vital for SoC. Increase the design quality and development speed.

- SoC development needs a variety of technology layers from a system to a device and needs several optimization for the applications.

- A global development managing system is another key to success. Make collaboration and unification over different technology groups to shorten the development time and increase customer satisfaction.