Mixed signal systems and integrated circuits

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1. Introduction

• Mixed signal systems
  – Software defined radio
  – Digital read channel
  – Mixed Signal SoC

• Progress of ADC and DAC
  – Power and area
  – Embedding
Basic mixed signal system

Mixed signal systems basically consist of DSP, ADC, DAC, and pre/post filters. The signals are converted between continuous time and discrete time.
Software defined radio

Future wireless systems need powerful ADC and DAC for software defined radio.

Future cellular phone needs 11 wireless standards!!

Multi-standards and multi chips

Current

Multi-bands and Multi-standards on a single chip

Future

2006.10.19
A. Matsuzawa, Tokyo Tech.
Power and area reduction of video-rate 10b ADCs

Power and area of ADC have been reducing continuously. Currently, ADC can be embedded on a chip.

Power reduction

Area reduction

Power and area of ADC have been reducing continuously. Currently, ADC can be embedded on a chip.
Power and area reduction of video-rate 10b ADCs

M. Hotta et al. IEICE 2006. June
2. Characterization of data converters

• Basic functions of ADC and DAC
• Static performance
  – INL, DNL, monotonicity
  – Quantization noise
• Dynamic performance
  – SNR, SFDR, THD, SNDR, ENOB
  – Sampling Jitter
  – ERB
  – Glitch
• Figure Of Merit
• Performances and applications
  – Needed performances for wireless systems
Basic functions of ADC

Sampling: Sampling the analog signal with accurate timing.
Quantization: Express the converted data with certain accuracy.

Sampling

Quantization

Coding

Analog

Digital

ADC

CLK
Static performance

INL and DNL are the major static performance indicators of ADC and DAC.

**DNL: Differential Non-Linearity**

\[
DNL_j = \frac{\text{Width}_{\text{ACTUAL},j} - \text{Width}_{\text{IDEAL}}}{\text{Width}_{\text{IDEAL}}}
\]

**INL: Integrated Non-Linearity**

\[
INL_j = \sum_{k=0}^{k=j} DNL_k
\]

\[
DNL_j = INL_{j+1} - INL_j
\]
DNL and INL
Binary coded DAC often degrades monotonicity.

The monotonicity stands for the qualitative characteristics of data converters of which transfer function keep the monotonic increase or decrease.

At the change of MSB bit

If the converter can not guarantee the monotonicity, The feedback loop doesn’t work properly and results in backrush.
Quantization noise

Quantization causes noise

Higher SNR needs higher resolution

Transfer characteristics

\[ P_n = \int_{-\Delta/2}^{\Delta/2} e^2 P(e) \, de = \int_{-\Delta/2}^{\Delta/2} e^2 \frac{1}{\Delta} \, de = \frac{\Delta^2}{12} \]

\[ \therefore P(e) = \begin{cases} \frac{1}{\Delta}, & |e| < \frac{\Delta}{2} \\ 0, & \text{all other } e \end{cases} \]

Quantization noise

\[ P_s = \frac{(\Delta \cdot 2^{N-1})^2}{2} \]

\[ SNR = \frac{P_s}{P_n} = \frac{(\Delta \cdot 2^{N-1})^2}{2} \cdot \frac{12}{\Delta^2} = 1.5 \cdot 2^{2N} \]

\[ SNR_{dB} = 10 \log \left( \frac{P_s}{P_n} \right) = 6.02 \cdot N + 1.76 \]
Dynamic performance indicates the ratio between signal and noise or distortion. We should use the suitable terms depending upon the type of application.

\[
\begin{align*}
SNR &= 10 \log \frac{\text{Signal power}}{\text{Total noise floor power}} \\
SFDR &= 10 \log \frac{\text{Signal power}}{\text{Largest spurious power}} \\
THD &= 10 \log \frac{\text{Total harmonic distortion power}}{\text{Signal power}} \\
SNDR &= 10 \log \frac{\text{Signal power}}{\text{Noise and distortion power}} \\
\text{ENOB} &= \frac{\text{SNDR} - 1.76}{6.02}
\end{align*}
\]

\[F_c = 40\text{MHz}, \; f_{in} = 4\text{MHz}\]
\[SFDR = 49.8\text{dB}\]
\[\text{SNDR} = 44.9\text{dB}, \; \text{ENOB} = 7.17\text{-bit}\]
\[2\text{ndHD} = -49.8\text{dB}, \; 3\text{rdHD} = -56.7\text{dB}\]
Sampling jitter effect

Sampling jitter is converted to noise.
When the input frequency becomes higher, the SNR becomes lower.

\[ SNDR(dB) = -10 \log \left( \frac{1}{(2\pi f_{in}\sigma_t)^2} \right) \]

\[ \Delta V = \frac{dV_{sig}}{dt} \sigma_t \]

\[ V_{sig} \]

Input signal

\[ \sigma_t \]

Time

\[ \Delta V \]

\[ 1 \times 10^{-13} \]

\[ 1 \times 10^{-12} \]

\[ 1 \times 10^{-11} \]

\[ \sigma_t \]

SNDR\((10 \cdot 10^6, \sigma_t)\)
SNDR\((20 \cdot 10^6, \sigma_t)\)
SNDR\((50 \cdot 10^6, \sigma_t)\)
SNDR\((100 \cdot 10^6, \sigma_t)\)
SNDR\((200 \cdot 10^6, \sigma_t)\)

A. Matsuzawa, Tokyo Tech.
Effective Resolution Bandwidth

ERB is the input frequency where the SNDR has dropped 3dB (or ENOB 0.5 bit)
Glitch is the spiky signal at code transition.

State 1: [1000]=8

State 2: [0111]=7

Intermediate: [1111]=15

Caused by overlapping of signals
This appears within a few psec,
However, energy is not negligible.
Glitch causes the distortion of signal

\[ P_{g,max} = 2^{2N-2} \cdot \Delta^2 \cdot \frac{T_g}{T_s} \]

\[ P_{g,max} < P_{QN} = \frac{\Delta^2}{12} \]

\[ T_g < \frac{T_s}{3 \cdot 2^{2N}} \]
Figure Of Merit

Figure of merit shows energy efficiency for data conversion.

\[ FOM = \frac{\text{Energy}}{\text{Conversion step}} \]

\[ = \frac{\text{Power}}{2^{\text{ENOB}} \times f_s} \]

or \[ = \frac{\text{Power}}{2^{\text{ENOB}} \times 2BW} \]

High Speed ADC
[Sampling Freq. VS Power]

JSSC, ISSCC, VLSI, CICC, ESSCC & Products
(\geq 10\text{Bit}, \geq 1995-2006)

12\text{Bit} (Paper)
10\text{Bit} (Paper)
12\text{Bit} Products
10\text{Bit} Products.
Needed resolution and conversion rate depending upon the application.

![Graph showing resolution and conversion rate for various applications.](image-url)
Needed SNR for certain BER in wireless system

Lower Bit Error Rate in the digital modulation needs higher SNR.

\[
\text{BER} \approx \text{erfc} \left( \sqrt{\text{SNR}} \sin \frac{\pi}{n} \right)
\]

\[
\text{BER} \approx 2 \left( 1 - \frac{1}{\sqrt{n}} \right) \text{erfc} \left( \frac{\sqrt{2 \cdot \text{SNR}}}{2 \left( \sqrt{n} - 1 \right)} \right)
\]
Signal intensity in wireless system

Wireless system has strong unwanted signals. Also, electric circuits generate distortion and noise.

Due to aliasing
Due to distortion of ADC

> Needed dynamic range to the blocker
> Needed SNR

Thermal Noise + Quantization noise
Needed ADC dynamic range

Existence of strong blockers results in the need for high dynamic range ADC.

ADC dynamic range = 86dB (14b)

Wanted signal
-97dBm

Blocker signal
-26dBm

ADC dynamic range = 36dB (6b)

WCDMA

Adjacent channel
-52dBm

DCS1800

Wanted signal
-33dB

Filter attenuation
-85dB

Thermal noise
20dB

Quantization noise
15dB

Quantization noise
15dB

DCS1800

WCDMA
3. Overview of high-speed A/D converters

- Performance and ADC architecture
- Integrating ADC
- Successive approximation ADC
- Flash ADC
- Sub-ranging ADC
- Interpolating ADC
- Folding ADC
- Pipelined ADC
There are many conversion architectures with varying performance parameters.
Integrating ADC achieves high resolution, but at low speed. Recently it has been used as column-ADC in CMOS imager.

- High resolution (20bit and more)
- Very low speed (DC measurement)
- Small DNL
- Can realize zero offset voltage
- Small analog elements and area

Going to 0 -> 1, when V_x becomes negative.

\[ v_x(T) = -\int_0^T \frac{(-v_{in})}{RC} d\tau = \frac{v_{in}}{RC} T \]
Successive-approximation ADC

Successive-approximation method is based on a binary search.

\[ V_{\text{in}} \rightarrow \text{S/H} \rightarrow + \rightarrow \text{Comparator} \rightarrow \text{Successive-approximation resistor and control logic} \rightarrow \text{DAC} \rightarrow V_{\text{ref}} \]

- Binary search
- Comparator
- Successive-approximation resistor and control logic
- DAC

Balance

- S/HVin
- Comparator
- Successive-approximation resistor and control logic
- DAC
- Vref

\[ V_{\text{DAC}} = \frac{1}{2} V_{\text{FS}} \]

- \( b_1 = 1 \)
- \( b_1 = 1, b_2 = 1 \)
- \( b_1 = 0, b_2 = 1, b_3 = 0 \)
- \( b_1 = 0, b_2 = 1, b_3 = 1 \)
- \( b_1 = 0, b_2 = 1, b_3 = 0, b_4 = 1 \)

VFS MSB LSB

2006.10.19 A. Matsuzawa, Tokyo Tech.
Charge-redistribution ADC

Charge-redistribution ADC draws attention as a suitable ADC in the nano-meter CMOS era. Because it needs no OP-Amp, but just needs capacitors and comparator.

1) Sampling

![Binary weighted Capacitor array](image)

\[ V_x = 0 \]
\[ Q = -2C V_{in} \]

2) Hold

![Binary weighted Capacitor array](image)

\[ V_x = -V_{in} \]
\[ Q = -2C V_{in} \]
Charge-redistribution ADC

3) Charge redistribution

\[ V_x = -V_{in} + \frac{V_{ref}}{2} \]

\[ Q = -2CV_{in} \]

Determine from MSB

Resistor ladder for higher resolution

If needed

Higher resolution  Easy calibration
Ultra low power  No OP amp
Low conversion rate  Needs multi clock
Successive-Approximation ADC

Charge-Redistribution ADC

Virtual ground

\( v_x = 0 \)

Sampling mode

Comparator

Sampled input signal

Reference voltage

Charge-Redistribution ADC

\( v_{in} \)

\( v_{ref} \)
Successive-Approximation ADC

Charge-Redistribution ADC

\[ v_x = -v_{in} \]

Hold mode

Sampled input signal

Reference voltage

\[ v_{in} \]

\[ v_{ref} \]
Successive-Approximation ADC

Charge-Redistribution ADC

Determine the output bits from MSB to LSB

\[ v_x = -v_{in} + \frac{v_{ref}}{2} \]

Bit cycling mode

Sampling input signal

Reference voltage

\[ v_{in}, v_{ref}, v_{out} \]
Flash ADC is very fast, but area and power increase exponentially with resolution.

- Ultra fast operation: Several GHz
- No sample and hold
- Low resolution: <8 bit
- Large input capacitance → difficult to drive

Flash ADC diagram:
- Input voltage $V_{\text{in}}$
- Comparator
- Encoder
- Digital output $V_{\text{ref}}/2^N$
- Input voltage
- Scale
- $V_{\text{ref}}$
- $D_1 D_2 D_3 D_4 D_5$
Sub-ranging ADC

Multi-step conversion can reduce the # of comparators. However, it needs high precision comparators. As a result, small power and area.

10bits: Flash; $2^N - 1 = 1023$

two step; $2 \left( \frac{N}{2} - 1 \right) = 62$

Slide gauge

Upper conversion

Lower conversion

Input voltage
Two step parallel ADC

One of the basic architectures for video-rate ADCs
Chopper inverter comparator

Pros: Simple, low power, small area, low voltage, and sample and hold action
Cons: large absolute offset, suffer the power supply noise, sensitive to Vdd.

S1, S2:ON, S3:OFF; Signal sampling
S1, S2:OFF, S3:ON; Offset cancel and amplify

Vin=Vr: No change
Vin>Vr: Vout goes down
Two step parallel ADC

Realizing simultaneous signal sampling
2 channel lower conversion units realize two times higher operation
Overlap scheme relaxes needed offset voltage for comparators
Interpolation method

Interpolation can generate accurate intermediate references which are between two references. Thus step sizes are almost equal, even though mismatch voltages are large.

K. Kusumoto and A. Matsuzawa
Virtual reference voltages can be generated by the interpolation method.
**Feature of the interpolating ADC**

Small DNL error and very smooth connection between the upper and the lower conversions.

The effect of mismatch of the differential amplifiers on the DNL can be reduced to $1/m$, where $m$ is the number of the interpolation.

Also, the effect of mismatch of the lower bit comparators on the DNL can be reduced to $1/G$, where $G$ is the voltage gain of the differential amplifiers.

No need to adjust the voltage gain.

$$\sigma_{off}^2 = \left( \frac{\sigma_{diff}}{m} \right)^2 + \left( \frac{\sigma_{cmp}}{G} \right)^2$$
Capacitive interpolation CMOS ADC

World lowest power dissipation video rate 10b ADC in 1992.

10bit, 20MHz, 30mW @0.8umCMOS ADC

Capacitive interpolation

Interpolation, offset cancel, amplification, in a pipeline manner.
Folding ADC

Input signal is folded to the compressed signals of which phases are different. Lower bits are obtained by comparing between these folded signals.

Low power and small size, yet still high speed. However, not suitable for higher resolution. <10bit
Folding circuits

Composing the folding characteristics by the summation of currents from differential transistor pairs.
Pipelined ADC

Pipelined ADC is the centerpiece of embedded ADCs for many applications, such as digital cameras, digital TVs, ADSLs, VDSLs, and wireless LANs.

Suitable for CMOS
Switched capacitor operation

High resolution (<15bit)
Moderate speed (<200MHz)
Low power consumption

Conventional M is 1 or 1.5

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1.5-bit/stage Pipeline ADC

Amplification at each stage reduces the input referred thermal noise. 1.5b/stage architecture reduces the requirement for the comparator offset drastically.

Unit conversion stage for 1.5-bit/stage pipeline ADC

\[
V_o = \begin{cases} 
(1 + \frac{C_s}{C_f}) V_i + \frac{C_i}{C_f} V_{\text{ref}} & \text{if } V_i < -\frac{V_{\text{ref}}}{4} \\
(1 + \frac{C_s}{C_f}) V_i & \text{if } -\frac{V_{\text{ref}}}{4} \leq V_i \leq \frac{V_{\text{ref}}}{4} \\
(1 + \frac{C_s}{C_f}) V_i - \frac{C_i}{C_f} V_{\text{ref}} & \text{if } V_i > \frac{V_{\text{ref}}}{4} 
\end{cases}
\]
Pipelining

Pipeline action relaxes settling time requirement.

Sample & Hold

1st stage

2nd stage

Sample and Hold

Op amp

Cf

Cs

Sample

Op amp

Cf

Cs

Amplify

Sample

Amp.

Sample

Amp.
4. Overview of high-speed D/A converters

- Basic two concepts of DAC
  - Binary method
    - R-2R based DAC
    - Capacitor array DAC
  - Decoder method
    - Resistor string DAC
    - Current steering DAC
Basic two concepts of DAC

1. Binary method

Not small DNL
Large glitch
Small area

$$V_{\text{analog}} = V_{\text{ref}} \sum_{i=1}^{N} \frac{1}{2^i} \cdot D_i$$

2. Decoder method

Small DNL
Small glitch
Large area

$$V_{\text{analog}} = V_q \sum_{i=0}^{N-1} 2^i \cdot D_i$$
Binary method

R-2R based DAC

R-2R resistor ladder can generate binary weighted current easily.

Resolution: 12b
Large DNL
Small area at high resolution
Moderate speed
Large power consumption

\[ v_{out} = R_F \left( I_r \cdot A_0 + \frac{I_r}{2} \cdot A_1 + \frac{I_r}{2^2} \cdot A_1 + \frac{I_r}{2^3} \cdot A_1 \right) \]

\[ I_r = \frac{v_{ref}}{2R} \]
Binary method

Capacitor array DAC

Capacitor array DAC is widely used in CMOS technology.

Low power and no sample & Hold

\[ Q = v_{ref} \left[ C \cdot A_0 + 2C \cdot A_1 + 4C \cdot A_2 + 8C \cdot A_3 \right] \]

\[ v_{out} = -\frac{Q}{16C} \]

\( A_i = 0 \) or \( 1 \)

Reset

Enable
Decoder method can realize small DNL, however needs large area at high resolution.

Resolution limit: 10b
Good DNL
Low speed
Small glitch

Digital value

large parasitic capacitance: $2^N$
Current steering DAC

Widely used for high speed DAC. Graphics, communications, etc.

High speed, -- 1 GHz
Resolution – 14 b
Small DNL
Small glitch

Conventionally large area

Current source

Current cell with switch
6. Basic design considerations

- **Accuracy**
  - Current mismatch and DAC accuracy
  - $V_T$ mismatch
  - Capacitor mismatch
- **Comparator**
  - Offset compensation
- **Op-Amp**
  - Gain and GBW
  - kT/C noise
Current mismatch and DAC accuracy

Larger resolution requires smaller mismatch.

\[ \frac{\sigma(I)}{I} \approx \frac{1}{2C\sqrt{2^N}} \]

N: resolution

C: constant determined by INL yield

INL yield

Van den Bosch,.. Kluwer 2004
Larger gate area is needed for smaller $V_T$ mismatch. Technology scaling reduces $V_T$ mismatch if the gate area is equal.
Mismatch current and transistor size

Smaller mismatch requires larger L and W.

\[ I_{ds} = K' \frac{W}{L} (V_{gs} - V_T)^2 \]

\[
\Delta I_{ds} = \frac{\partial I_{ds}}{\partial V_T} \Delta V_T + \frac{\partial I_{ds}}{\partial K'} \Delta K' + \frac{\partial I_{ds}}{\partial \left( \frac{W}{L} \right)} \Delta \left( \frac{W}{L} \right)
\]

\[
\frac{\Delta I_{ds}}{I_{ds}} = -2 \frac{\Delta V_T}{V_{gs} - V_T} + \frac{\Delta K'}{K'} + \frac{\Delta \left( \frac{W}{L} \right)}{\left( \frac{W}{L} \right)}
\]

\[ \left( \frac{\Delta I_{ds}}{I_{ds}} \right)^2 = \frac{4K' A_{VT}^2}{L^2 I_{ds}} + \frac{A_K^2}{WL} + A_{WL}^2 \left( \frac{1}{W^2} + \frac{1}{L^2} \right)^2 \]

Mismatch

\[ \Delta V_T \approx \frac{A_{VT}}{\sqrt{LW}} \]

\[ \frac{\Delta K'}{K'} \approx \frac{A_K'}{\sqrt{LW}} \]

\[ \Delta \left( \frac{W}{L} \right) = A_{WL} \sqrt{\frac{1}{W^2} + \frac{1}{L^2}} \]

\[ V_{gs} - V_T = \sqrt{\frac{I_{ds}}{K' \left( \frac{W}{L} \right)}} \]
Capacitor mismatch

Smaller capacitor mismatch requires larger capacitance

\[ \frac{\Delta C}{C} (3\sigma) = \frac{6 \times 10^{-4}}{\sqrt{C_{(pF)}}} \]

Coefficient depends on the Fab.

Typical MIM capacitor

- 10bit: 0.4pF
- 12bit: 4pF
- 14bit: 40pF

Capacitance (pF)

10bit, ¼ LSB
12bit, ¼ LSB
14bit, ¼ LSB
kT/C noise

Larger SNR requires larger capacitance and larger signal swing. Low signal swing increases required capacitance.

\[
\langle v_n^2 \rangle = 4kTR \int_0^\infty \frac{1}{1 + (\omega CR)^2} d\omega = kT/C
\]

\[
v_n^2 = \frac{n kT}{C} \quad n: \text{configuration coefficient}
\]

\[
\text{SNR (dB)} = 10 \log \left( \frac{CV_{FS}^2}{8nkT} \right)
\]

\[
v_n^2 = \frac{n kT}{C} \quad n: \text{configuration coefficient}
\]

\[
\text{SNR (dB)} = 10 \log \left( \frac{CV_{FS}^2}{8nkT} \right)
\]
CMOS comparators

There are many types of comparator circuits

(a) [Diagram]

(b) [Diagram]

(c) [Diagram]

(d) [Diagram]
Low power CMOS comparator

A CMOS comparator is low power because of no need of static current.

No static current
Differential comparison
Interpolation action
High speed

Interpolation action

\[ G_1 = K_p \left[ \frac{W_1}{L} (V_{in1+} - V_{th}) + \frac{W_2}{L} (V_{in2+} - V_{th}) \right] \]

\[ G_2 = K_p \left[ \frac{W_1}{L} (V_{in1-} - V_{th}) + \frac{W_2}{L} (V_{in2-} - V_{th}) \right] \]

if \( W_1 : W_2 = \frac{m-n}{m} : \frac{n}{m} \)

then, \( (m-n)V_{in1+} + nV_{in2+} = (m-n)V_{in1-} + nV_{in2-} \)

Gain bandwidth (=Speed) is inversely proportional to the $L^2$ (channel length). Technology scaling is still effective to increase the comparator speed, if we don’t take care of the signal dynamic range.

\[
GBW = \frac{g_m}{2\pi \left(WC_j + \frac{2}{3} C_{ox} LW\right)} = \frac{I_{sink}}{2\pi \left(WC_j + \frac{2}{3} C_{ox} LW\right) V_{eff}}
\]

\[
I_{sink} = \frac{\mu C_{ox}}{2} \frac{W}{L} V_{eff}^2 \quad C_{ox} = \frac{\kappa}{L}
\]

\[
GBW = \frac{\mu V_{eff}}{2\pi L^2 \left(\frac{2}{3} + \frac{C_j}{k}\right)}
\]
Offset compensation

Two ways for suppressing offset voltage.

Store the offset voltage in capacitors and subtract it from the signal.

\( (V_a - V_{osA})(-A) = V_o = V_a \)

\[ V_o = V_a = \frac{A}{1 + A} V_{osA} \]

\( V_{osA} \): Offset of the amplifier
\( V_{osl} \): Offset of the latch

a) Offset cancel at input nodes

b) Offset cancel at output nodes

Feedback = High gain type

Feed forward = Low gain type
Higher resolution requires higher open loop gain.
Higher conversion frequency requires higher closed loop GBW.

DC gain

\[
G_{\text{error}} \approx -\frac{1}{G} \left(2 + \frac{C_p}{C_f}\right) \approx -\frac{1}{G\beta} \\
\beta \equiv \frac{1}{2 + \frac{C_p}{C_f}}
\]

\[
\frac{1}{G} \leq \frac{\beta}{2^{N-M+1}}
\]

N: ADC resolution
M: Stage resolution

\[
G(dB) > 6N + 10
\]

for 1.5b pipeline ADC

Closed loop gain-bandwidth

\[
\text{GBW}_{\text{close}} = \frac{g_m\beta}{2\pi C_L} > \frac{N \cdot f_c}{3}
\]

\[
\square = \frac{C_f}{C_f + C_s + C_{pi}}
\]

\[
C_L = C_{po} + C_{ol} + \frac{C_f(C_s + C_{pi})}{C_f + C_s + C_{pi}}
\]
Cascode circuits is used to increase voltage gain.

Cascode

High BGW
Medium DC gain

Medium BGW
Medium DC gain
Low voltage operation

Operational amplifier

Folded cascode
Operational amplifier

Super cascode realizes extremely high gain with wide GBW.

Extremely high DC gain
Wide GBW

\[ r_{out} = G \cdot g_{m2} \cdot r_{ds2} \cdot r_{ds1} \]

Super cascode ckt.
(Regulated cascode)

Super cascode amp.

Actual ckt.
Basic design consideration

Very tough tradeoffs, so let’s keep up the design effort.

Small mismatch

\[
\frac{\Delta C}{C} \text{ or } \frac{\Delta V_{\text{off}}}{V_{FS}} \propto \frac{1}{2^N}
\]

Increase Capacitance

\[
\frac{\Delta C}{C} \propto \frac{1}{\sqrt{C}} \text{ or } \frac{\Delta V_{\text{off}}}{\sqrt{LW}} \propto \frac{1}{\sqrt{C_g}}
\]

\[
C \propto 2^{2N}
\]

Results in

Decrease speed and Increase Power

\[
f_s \propto GBW \propto \frac{g_m}{C} \propto \frac{g_m}{2^{2N}} \quad GBW \propto \frac{I_d}{C} \propto \frac{I_d}{2^{2N}}
\]

\[
P_d \propto V_d I_d \propto f_s \cdot C \propto f_s \cdot 2^{2N}
\]

\[
f_s \propto \frac{I_d}{2^{2N}} \quad P_d \propto f_s \cdot 2^{2N}
\]

Solutions

1) Architecture
   Pipeline, Parallel
2) Redundancy
3) Error compensation
4) Circuit design

However, kT/C issue remains

\[
SNR \propto CV_{\text{sig}}^2 \propto 2^{2N}
\]

\[
C \propto \left( \frac{2^N}{V_{\text{sig}}} \right)^2
\]

Solutions

1) Increase signal swing
2) Increase OSR

\[
SNR \propto OSR
\]
Study-aid books