Mixed signal systems and integrated circuits

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Contents

• Mixed signal systems
• High speed A/D converters
• High speed D/A converters
• Sigma delta A/D and D/A converters
• Wireless systems and RF CMOS circuits
• PLL and related systems
Aim of this lecture

• Understanding basic current mixed signal systems
  – Wireless transceiver

• Understanding basic mixed signal circuit building blocks:
  basic operation method and basic design method
  – A/D and D/A converter
  – Sigma-delta modulation
  – Phase Lock Loop and Delay Lock Loop
  – Low Noise Amplifier
  – Frequency Mixer
  – Voltage Controlled Oscillator and Frequency Synthesizer
1. Mixed signal systems
Current electronics and mixed signal technology
Exciting digital consumer electronics world

New consumer electronics era has been emerged. Key technologies are digital multimedia and System on a Chip.

- Exciting Multimdia with System LSI Solutions
- Anywhere
- Audio and Video
- Better Look
- Better Sound
- Higher Quality
- Anytime
- Semiconductor Technology
- System and Software Technologies
- Broadcasting Communication Network
- Storage Media
LCD Driver

LCD driver is a simple example of mixed signal LSI
LCD Driver

LCD driver is an array of DA converters

Controller

6 bit * R, G, B * 2 = 36 bit

Shift Register 64

384 * 6 bits Latch

384 * 6 bits Latch

384 * 6 bits level shifter

384 * Voltage Scalling DA Converter

384 output

XGA: 1024 * RGB (=3072) \( \rightarrow \frac{3072}{384} = 8 \text{LSIs} \)
Digital consumer electronics and networking drive current electronics.
Mixed signal technology enables high speed digital networking.

- **Data conversion**
- **Equalization**
- **Encryption**
- **Data and clock recovery**
- **Noise cancellation**
- **Error correction**

**Analog circuit**
- Line I/F
- ADC
- 250Mbaud (PAM-5)
- DAC
- 6b, 125MHz ADC, DAC
- Pulse Shaping
- FFE
- Clock Recovery

**Digital circuit**
- Slicer
- DFE
- 3-NEXT Canceller
- Side-stream Descrambler & Trellis, Viterbi decoder
- Side-stream Scrambler & Trellis, Viterbi Symbol Encoder
x-DSL

ADSL and VDSL use the mixed signal technology

- ADSL-service, 0.5–8Mbps(Dwn)/1Mbps (Up) for 5~6Km
- VDSL-service, 13–52Mbps(Dwn) for 0.3–1.5Km.

- ADSL: 0.1MHz–1.1MHz
- VDSL: 2.0MHz–3.5MHz

- Anti-aliasing Filter
- ADC
- Decimation Filter
- Adaptive DFE
- Error Correction FEC
- Interpolation Filter
- Error Correction FEC

- RX-in
- TX-out

- 4~256-QAM modulation
  - 60MHz 10-bit ADC and DAC for VDSL
  - 5MS/s 14-bit ADC and DAC for ADSL

- 96-tap Decision Feedback Equalizer (DFE)

- T=8 Read-Solomon Forward Error Correction (FEC)
Mixed signal tech. ; Digital read channel

Digital storage also needs high speed mixed signal technologies.

Variable Gain Amp. → Analog Filter → A to D Converter → Digital FIR Filter → Viterbi Error Correction

Data In (Erroneous) → Voltage Controlled Oscillator → Clock Recovery

Data Out (No error)

Analog circuit
Digital circuit
Mixed signal SoC for DVD RAM system

This enables high readability for weak signal from DVD RAM pickup.

World fastest and highly integrated mixed signal CMOS SoC

0.18um- eDRAM
24M Tr
16Mb DRAM
500MHz Mixed Signal

Goto, et al., ISSCC 2001
Mixed signal SoC can realize full system integration for DVD application. Embedded analog is the key.

0.13um, Cu 6Layer, 24MTr
Recent developed mixed signal CMOS LSIs

5G RF LAN

12b 50MHz ADC 2ch
12b 50MHz DAC 2ch

AFE (Analog Front End)

Digital network

1394b (1GHz)

AFE for Digital Camera

12b 20MHz ADC+AGC

AFE for ADLS

12b 20MHz ADC+DAC

2GHz RF CMOS

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Application area in mixed signal CMOS tech.

Almost all the products need mixed signal CMOS LSI tech.

Wireless
- Cellular phone: PDC, W-CDMA
- RR-Net: Bluetooth, IEEE802.11
- Broadcast: STB, DTV, DAB

Wired
- Optical: FTTH, OC-xx
- Metal: ADSL, VDSL, Power line modem
  - Serial: IEEE1394, USB, Ethernet
  - Parallel: DVI, LVDS

Recording
- DVD, VDC, HDD

Output
- LCD, PDP, EL, Audio drive

Input
- Camera, Others

Power supply
- Switching supply, Every LSIs (On-chip)
Digital technology in real world

Digital signal suffers heavy damage in real world. But, digital can address this issue by own advantages, but needs the help of analog tech.

Advantages of Digital Tech.

- High robustness
- Programmability
- Time shift (memory)
- Error correction
- High Scalability

Pure digital

Mixed signal technology (Analog+Digital)

Real world

Damaged digital

Reconstruction

Recovered digital

Not only digital, but also analog; ADC, DAC, Filter, and PLL are needed
Role of current analog technology

The role of current analog technology is an interface between digital technology and outer physical world. Analog supports digital.
Basic technology for digital network and storage

Analog and data converter technologies are needed for digital network and digital storage

Network

Storage media

Analog technology
- RF
- Optical I/F
- Cable drive
- Signal Generation

Data Converter
- A/D Converter
- D/A Converter

Communication processing
- Mod/ Demod
- Channel select
- Error correction
- Protocol
- Encryption

Data compression
- MPEG2, 4
- DSP
- Codec

Digital technology

Analog technology

NetworkStorage media

Analog and data converter technologies are needed for digital network and digital storage

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Development of ADCs has contributed to the progress of digital consumer electronics.

- Bip / BiCMOS
- CMOS
- Applied System
- DVD
- Digital Camera 8b, 100MHz
- Digital OSC
- HDTV
- Camera
- Video Camera
- Wide-TV
- MUSE Receiver
- Perfec TV
- Video Switcher
- 6b, 80MHz
- 6b, 1GHz
- 6b, 800MHz
- 8b, 20MHz
- 10b, 20MHz, 30mW
- 10b, 300MHz
- 8b, 20MHz
- 10b, 30MHz
- 8b, 120MHz
- 10b, 20MHz
- '85
- '90
- '95

Development of ADCs for digital consumer products

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Progress in A/D converter; video-rate 10b ADC

<table>
<thead>
<tr>
<th>Year</th>
<th>Type</th>
<th>Power</th>
<th>Cost</th>
<th>Power Reduction</th>
<th>Cost Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>1980</td>
<td>Conventional product</td>
<td>20W</td>
<td>$8,000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1982</td>
<td>World 1st Monolithic Bipolar (3um)</td>
<td>2W</td>
<td>$800</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1993</td>
<td>World lowest power CMOS (1.2um)</td>
<td>30mW</td>
<td>$2.00</td>
<td>1/200,000</td>
<td>1/2,000</td>
</tr>
<tr>
<td>2009</td>
<td>SoC Core CMOS (0.15um)</td>
<td>10mW</td>
<td>$0.04</td>
<td>1/2,000</td>
<td>1/200,000</td>
</tr>
</tbody>
</table>

ADC is a key for mixed signal technology. We have reduced the cost and power of ADC drastically; 1/2,000 in Power and 1/200,000 in cost! CMOS technology attained it. dulling past 20 years

Analog Devices Inc.
Power and area reduction of video-rate 10b ADCs

Power and area of ADC have been reducing continuously. Currently, ADC can be embedded on a chip.

Power reduction

Area reduction
Power and area reduction of video-rate 10b ADCs

M. Hotta et al. IEICE 2006. June
Early stage mixed signal CMOS LSI for CE

Success of CMOS ADC and DAC enabled low cost mixed signal CMOS LSI. This also enabled low cost and low power digital portable AV products.

1993 Model: Portable VCR with digital image stabilizing

System block diagram
Mixed signal system: Digital Camera

Current camera system uses digital technology.
Ultra-high speed ADCs have been developed.

- **8b, 120MHz, (1984)**
  - World fastest 8b ADC

- **8b, 600MHz ADC (1991)**
  - World fastest 8b ADC

- **6b, 1GHz ADC (1991)**
  - World fastest in production
    - (Dual Parallel method)
Ultra-high speed ADCs have realized Digital Oscilloscopes.

松下通信工業: 10b 100MHz OSC (1986年)

横河電機: 8b 1GHz (1994年)
Progress in high-speed ADC

High speed ADC has reduced its power and area down to be embedded.

**World fastest 6b ADC**
- 6b, 1GHz ADC
- ISSCC 1991
- 2W
- 1.5um Bipolar

**ISSCC 2000 World fastest CMOS ADC**
- 6b, 800MHz ADC
- 400mW, 2mm²
- 0.25umCMOS

**ISSCC 2002 World lowest Pd HS ADC**
- 7b, 400MHz ADC
- 50mW, 0.3mm²
- 0.18umCMOS

![Graph showing Reported Pd of CMOS ADCs](image)

- **This Work**
- **1 order down**

- **Conversion rate [x100Msps]**
- **Pd/2^N[mW]**

- **10mW/Gsps**
- **1mW/Gsps**

System: DVD player

Current electrical system is complicated and needs analog and memory.

Optical Disc Optical Head

Memory

32bit MCU DRAM Embedded

Media Core Processor

MPEG Algorithm

Video Output

AC-3 Output

Stereo Output

Console Panel

Driver

Head Amp

Red Laser

Photo-receptive Compound

Red Laser Unit

Pre Amp

Read Channel

ODC

Demodulation ECC

Copy Protection

AV Decoder

MPEG 2 Video

AC-3 Audio

System Controller MCU

Servo DSP

Servo DSP

System Controller MCU

Servo DSP

System Controller MCU

: First-Gen.

: Third-Gen.

: Second-Gen.

: Fourth-Gen.

OS API

High-speed Analog-Digital

Current electrical system is complicated and needs analog and memory.
Full DVD system integration in 0.13um tech.

Advanced mixed signal SoC has been successfully developed.

Okamoto, et al., ISSCC 2003

0.13um, Cu 6Layer, 24MTr

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Cost reduction in DVD Recorder

One-chip integration for hole DVD system has been realized. This makes circuit board simpler and contribute to the cost down, as well as performance up.

’2000 Model

’2003 Model
Current Scaled CMOS technology is very artistic.

Matsushita’s 0.13um CMOS technology
CMOS as analog device

CMOS has many issues as analog device, but also has a variety of circuit techniques

<table>
<thead>
<tr>
<th></th>
<th>CMOS</th>
<th>Bipolar</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch action</td>
<td>++</td>
<td>--</td>
<td>Only CMOS can realize switched capacitor circuits</td>
</tr>
<tr>
<td>Low Input current</td>
<td>++</td>
<td>--</td>
<td>CMOS is ¼ of Bip.</td>
</tr>
<tr>
<td>High gm</td>
<td>-</td>
<td>+</td>
<td>CMOS is 10x of Bip.</td>
</tr>
<tr>
<td>Low Capacitance</td>
<td>+</td>
<td>-</td>
<td>This results in Cp issue</td>
</tr>
<tr>
<td>$f_T$</td>
<td>+</td>
<td>+</td>
<td>Almost same</td>
</tr>
<tr>
<td>Voltage mismatch</td>
<td>--</td>
<td>++</td>
<td>CMOS is 10x of Bip.</td>
</tr>
<tr>
<td>$1/f$ noise</td>
<td>--</td>
<td>++</td>
<td>CMOS is 10x to 100x of Bip.</td>
</tr>
<tr>
<td>Low Sub. effect</td>
<td>-</td>
<td>+</td>
<td></td>
</tr>
<tr>
<td>Offset cancel</td>
<td>++</td>
<td>--</td>
<td>CMOS has a variety of techniques to address the self issues</td>
</tr>
<tr>
<td>Analog calibration</td>
<td>++</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>Digital calibration</td>
<td>++</td>
<td>--</td>
<td></td>
</tr>
<tr>
<td>Embed in CMOS</td>
<td>++</td>
<td>--</td>
<td></td>
</tr>
</tbody>
</table>
GHz operation by CMOS

Cutoff frequency of MOS becomes higher than that of Bipolar. Over several GHz operations have attained in CMOS technology.

\[ f_T = \frac{gm}{2\pi C_{in}} \]

\[ f_{Tpeak} \approx \frac{v_{sat}}{2\pi L_{eff}} \]
CMOS technology for over GHz networking

Digital consumer needs over GHz wire line networking. CMOS has attained 5Gbps data transfer.

World first 1394b transceiver
For 1Gbps networking
0.25um 3AL_CMOS

Test chip for 5Gbps wire line
0.18um 4AL_CMOS

5Gbps Eye pattern
Scaling can realize higher integration and higher speed yet low power for digital circuits. In contrast, analog performance is used to be degraded with scaling.

Architectural and circuit technology development has been needed.
Wireless systems

The number of wireless standards are increasing

- 4G
- PDC
- W-CDMA
  - (384k)
- GSM
- PRS
- EDGE
- cdma2000
- 1X
- (144K)
- IEEE802.20
  - (4M)
- cdma2000-1X
- EV-DO
  - (2.4M)
- IEEE802.11b
  - (11M)
- IEEE802.11a/g
  - (54M)
- IEEE802.11n
  - (100M)
- IEEE802.15
- ZigBee
- Bluetooth
- IEEE802.15 WB

Data rate
Technology edge RF CMOS LSI

Many RF CMOS LSIs have been developed for many standards

**Wireless LAN, 802.11 a/b/g**
0.25um, 2.5V, 23mm$^2$, 5GHz

**Discrete-time Bluetooth**
0.13um, 1.5V, 2.4GHz

M. Zargari (Atheros), et al., ISSCC 2004, pp.96
K. Muhammad (TI), et al., ISSCC2004, pp.268
Current status of RF CMOS chip

RF CMOS was a university research theme, however currently becomes major technology in wireless world.

• Current products
  – Bluetooth: 2.4GHz, CSR etc., major
  – Wireless LAN: 5GHz, Atheros etc., major
  – CDMA: 0.9GHz-1.9GHz, Qualcomm, becomes major
  – Zigbee: 2.4GHz, not yet, however must use CMOS
  – TAG: 2.4GHz, Hitachi etc., major

Major Cellular phone standard, GSM uses SiGe-BiCMOS technology
Why CMOS?

- **Low cost**
  - Must be biggest motivation
  - CMOS is 30-40% lower than Bi-CMOS

- **High level system integration**
  - CMOS is one or two generation advanced
  - CMOS can realize full system integration

- **Stable supplyment and multi-foundries**
  - Fabs for SiGe-BiCMOS are very limited.
    - Slow price decrease and limited product capability

- **Easy to use**
  - Universities and start-up companies can use CMOS with low usage fee, but SiGe is difficult to use such programs.
Multi-standard issue

Reconfigurable RF circuit is strongly needed for solving multi-standard issue.

Future cellular phone needs 11 wireless standard!!

Yrjo Neuvo, ISSCC 2004, pp.32

Multi-standards and multi chips

Current

Current

Future

Unified wireless system

Reconfigurable RF

DSP

Unified wireless system

Reconfigurable RF

Yrjo Neuvo, ISSCC 2004, pp.32
Scalable circuit design for wireless systems

Scalable and reconfigurable design is needed for addressing the multi-standard wireless systems

Changeable: ADC/DAC resolution and bandwidth
Basics of analog to digital and digital to analog conversion
Basic mixed signal system

Mixed signal systems have DSP, ADC, DAC, and pre/post filter basically. The signals are converted between time continuous and time discrete.
Sampling theory

The signal has bandwidth of \( fm \). Periodical sampling pulse has a period of \( T \).

\[
v(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT)
\]

\[
v(t) = \sum_{n=-\infty}^{\infty} V_n e^{\frac{j2\pi nt}{T}}
\]

\[
V_n = \frac{1}{T} \int_{-T/2}^{T/2} v(t)e^{-\frac{j2\pi nt}{T}} dt
\]

\[
v(t) = \frac{1}{T} \sum_{n=-\infty}^{\infty} e^{\frac{j2\pi nt}{T}}
\]
Sampling process can be treated as the product of the signal and the sampling pulse.

Sampled signals have multi-sidebands at Nfc.

\[ x(t) \cdot v(t) = \sum_{n=-\infty}^{\infty} x(nT) \delta(t - nT) \]

\[ F(x(t) \cdot v(t)) = X(f) \sum_{n=1}^{\infty} \left( X(nf_c + f) + X(nf_c - f) \right) \]
Frequency spectrum in sampled data.

\[ x(t) \cdot v(t) = \sum_{n=-\infty}^{\infty} x(nT)\delta(t-nT) \quad v(t) = \frac{1}{T} \sum_{n=-\infty}^{\infty} e^{\frac{2\pi inT}{T}} = \frac{1}{T} \left( 1 + 2 \sum_{n=1}^{\infty} \cos \left( \frac{2\pi nt}{T} \right) \right) \quad \Theta \cos x = \frac{e^{ix} + e^{-ix}}{2} \]

\[ v(t) = \frac{1}{T} \left( 1 + 2 \cos(2\pi f_c t) + 2 \cos(2 \cdot 2\pi f_c t) + 2 \cos(3 \cdot 2\pi f_c t) + \ldots \right) \]

\[ x(t) \cdot v(t) = \frac{1}{T} \left( x(t) + 2x(t) \cos(2\pi f_c t) + 2x(t) \cos(2 \cdot 2\pi f_c t) + 2x(t) \cos(3 \cdot 2\pi f_c t) + \ldots \right) \]

Thus \( x(t)v(t) \) can be regarded as a AM modulated signal that the carrier signal of which frequency is \( nfc \) and the modulated signal is \( x(t) \)

If simply assuming \( x(t) \) is single tone: \( x_o \cos (2 \pi f_a t) \)

Sampled signal has a sideband of +/- \( f_a \) at around \( nf_c \)

\[ x(t) \cdot v(t) = \frac{x_o}{T} \left\{ \cos(2\pi f_a t) + 2 \sum_{n=1}^{\infty} \cos(2\pi f_a t) \cos(2\pi f_c t) \right\} \quad \Theta \cos A \cos B = \frac{1}{2} (\cos(A + B) + \cos(A - B)) \]

\[ = \frac{x_o}{T} \left\{ \cos(2\pi f_a t) + \sum_{n=1}^{\infty} \left( \cos(2\pi (nf_c + f_a) t) + \cos(2\pi (nf_c - f_a) t) \right) \right\} \]
Signal reconstruction from sampled data

If signal bandwidth is less than fc/2, signal can be reconstructed perfectly.

\[ F(x(t) \cdot v(t)) = X(f) + \sum_{n=1}^{\infty} \left\{ X(nf_c + f) + X(nf_c - f) \right\} \]

- **F(x(t)v(t))**: Fourier transform of x(t)v(t)
- **X(f)**: Fourier transform of the analog signal

Low pass filter

Nyquist condition

\[ f_m < \frac{f_c}{2} \]

Signal non-overlap

Signal can be separated to reconstruct

\[ f_m \geq \frac{f_c}{2} \]

Signal overlap

Signal can not be separated
Reconstruction from sampled signals

Sampled signal can be reconstructed to be continuous signal through low pass filter.

\[ x(t) \cdot v(t) = \sum_{n=-\infty}^{\infty} x(nT) \delta(t-nT) \]

Ideal Low pass filter:

\[ G(\omega) = \begin{cases} 
1 & |\omega| \leq \frac{\omega_c}{2} \\
0 & |\omega| > \frac{\omega_c}{2} 
\end{cases} \]

\[ y(t) = \sum_{n=-\infty}^{\infty} x(nT) \cdot v(t-nT) \]

\[ v(t) = \frac{\sin(\pi f_c t)}{\pi f_c t} \]

For the unit impulse signal
Reconstruction by sampling function

Signal can be reconstructed by the convolution between sampling signal and sampling function.

\[ S(t) = \frac{\sin(\pi f_c t)}{\pi f_c t} \]

\[ y(t) = \sum_{n=-\infty}^{\infty} x(nT) \cdot S(t-nT) \]

\[ y(t) = \sum_{n=-\infty}^{\infty} x(nT) \frac{\sin(\pi f_c (t-nT))}{\pi f_c (t-nT)} \]
Signals of which frequencies are higher than fc/2 are folded to the lower frequencies L.T. fc/2. Nose which spreads wide frequency is also folded to lower frequency and accumulated.

\[ f_{\text{alias}} = f_{\text{sig}} - nf_c \quad : \quad nf_c \leq f_{\text{sig}} < \frac{(2n+1)f_c}{2} \]

\[ f_{\text{alias}} = (n+1)f - f_{\text{sig}} \quad : \quad \frac{(2n+1)f_c}{2} \leq f_{\text{sig}} < (n+1)f_c \]
By using under sampling technique, we can obtain modulated signal from very high carrier frequency. However, very low SNR due to noise accumulation.
Reconstruction process

Reconstructed signals has also folding frequency components. Thus DAC need post low pass filter. The interpolation technique can relax the required LPF spec.
Aperture effect in DAC

Due to the aperture effect, the higher frequency component of the output signal from DAC is decreased. Sometimes some technique is needed.

Ideal impulse train

Actual Step pulse train in DAC output

Frequency characteristics of DAC

High frequency signal of DAC is decreased

Use aperture correction filter that has inverse frequency characteristics.

Reduce the pulse width by using small duty pulse

Increase the conversion frequency using over sampling technique
Frequency spectrums in ADC and DAC

Input signal to ADC

Folding

Signal in ADC and DSP

Re-folding

Signal from DAC without the aperture effect

Aperture effect

Signal from DAC with the aperture effect
ADC has a finite resolution number and the signal is quantized. This causes error called “quantization error”.

Quantized signal = Input signal + Quantization noise

Ideal quantization error

0 to $2^N$-1

0 to $2^N$

LSB (Least Significant Bit)
Quantization causes noise and this noise power reduces with increase of resolution number. Principal signal to noise ratio (dB) of N bit ADC is about 6N+2.

The higher resolution of ADC realizes the higher SNR for signal processing.

**Quantization causes noise and this noise power reduces with increase of resolution number.**

**Principal signal to noise ratio (dB) of N bit ADC is about 6N+2.**

**The higher resolution of ADC realizes the higher SNR for signal processing.**

**Probability density of quantization error**

\[
    p(x) = \begin{cases} 
        \frac{1}{q}, & |x| \leq 0.5q \\
        0, & |x| > 0.5q 
    \end{cases}
\]

**Noise power**

\[
    N_q = \int_{-0.5q}^{0.5q} x^2 p(x) dx = \frac{1}{3} \left( \frac{q}{2} \right)^2
\]

**Signal power**

\[
    S = \frac{1}{2} \left( \frac{2^N q}{2} \right)^2
\]

**Signal to Noise Ratio**

\[
    SNR_{rms} = 10 \log \left( \frac{S}{N_q} \right) = 20 \log 2^N + 10 \log(1.5)
\]

\[
    = 6.02N + 1.76(dB)
\]
SNR increase by increasing fsc

We can increase SNR by increasing of conversion frequency with low pass filter.

\[ SNR_{rms/rms} = 6.02N + 1.76 + 10\log\left(\frac{f_c}{2f_b}\right) \]

fc: Conversion frequency
fb: Bandwidth of LPF